FPGA-BASED DESIGN AND IMPLEMENTATION OF THREE-PRIORITY PERSISTENT CSMA PROTOCOL

Xu ZHI[1], Ding HONGWEI[2], Liu LONGJUN[3], Bao LIYONG[4], He MIN[5]

Carrier Sense Multiple Access (CSMA) is one of the key protocols to ensure the efficient operation of communication network. According to the characteristics of each node of the wireless sensor network, the field programmable gate array (FPGA) is used to provide a three-priority data transmission for the communication system of the persistent CSMA protocol. The design of the circuit not only contains the source module to meet the requirements of the agreement, while dividing a number of priorities, and in accordance with the principle of protocol to transfer data. Finally, through the circuit system test, the throughput and the average power of the node simulation results consistent with the theoretical value, confirmed the correctness of the circuit design.

Keywords: Carrier Sense Multiple Access; Wireless Sensor Network; Application of Field Programmable Gate Array; Source Module; Priority; Throughput ; Average Power of the Node

1. Introduction

With the development of communication technology, we are moving towards deeper areas of communication systems. The Wireless sensor network [1] is widely used with the features of reliability and flexibility. But the channel is an external shared state, the state of link is unstable, so how to allocate the limited resource is extremely important. The Wireless sensor network system is composed of a large number of stations, and the communication service of each station is intermittently working, and the channel resources are used irregularly, which will reduce its utilization rate. If the Carrier Sense Multiple Access (CSMA) [2] protocol is used in WSN, the station will listen to the channel state before transmitting the data, and then decide whether to send the information according to the state of channel. This strategy greatly reduces the number of conflicting states in the information transmission process, and improves the utilization of channel resources. The persistence CSMA protocol will send information immediately when the channel is idle, and will continue to listen on

[1] School of Information, Yunnan University, Kunming, China, e-mail: dhw19640@126.com
[2] School of Information, Yunnan University, Kunming, China
[3] School of Information, Yunnan University, Kunming, China
[4] School of Information, Yunnan University, Kunming, China
[5] School of Information, Yunnan University, Kunming, China

the channel state when it is detected that the channel is busy. This way greatly reduces the idle rate, effectively improving the channel utilization.

At present, the research method of MAC layer communication protocol is relatively simple [3, 4], and the theoretical equation of the protocols are simulated by mathematical simulation tool (Matlab). FPGA as a hardware performance, through its implementation of the communication protocol algorithm, the reality of the node transmission process in the hardware parallel circuit to achieve, which is a process from the theory to the practice, and through this experimental way can improve the theoretical understanding.

This paper first proposed implementation of three-priority CSMA protocol based on FPGA. Firstly, Matlab and Quartus II are used to design the priority modules which meet the principle of the three-priority persistence CSMA protocol. Then, a stable circuit is established by combining the hardware circuit description language Verilog and the logic circuit design. The control strategy of the three-priority persistence CSMA protocol algorithm is analyzed. Finally, the test results are consistent with the theoretical values, the throughput of the system is better than other MAC layer protocols, and the average power of the nodes is low. The hardware implementation in the communication protocol design provides a new way for the research of communication protocols, and provides a useful reference for improving the understanding of the network communication protocol and can be applied to the research of wireless sensor network.

2. Analysis of Protocol

2.1 Protocol model

The principle of persistence CSMA protocol: the site will send information immediately when the channel is idle, and will continue to listen on the channel state when it is detected that the channel is busy.

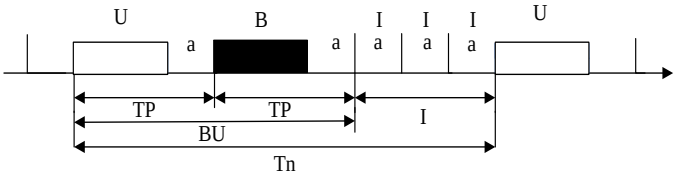

Fig. 1. Persistent CSMA protocol model

Fig. 1 is the persistent CSMA protocol model. UBI represent the three states of the channel: the information packet is sent successfully, the information packet is collided, and the channel is idle. TP indicates the sending time of an information packet, BU represents the success of the message packet transmission and the collision event; Tn represents a cycle of the busy time period and the idle

time period. In the wireless communication system, there are N channels for all users to random access, and the provisions of the terminal using multi-channel persistence CSMA technology. In the actual communication system, there are a variety of services such as voice service and video service, and different priorities are set according to the different characteristics of these services, and different users are required to occupy multi-channel rules.

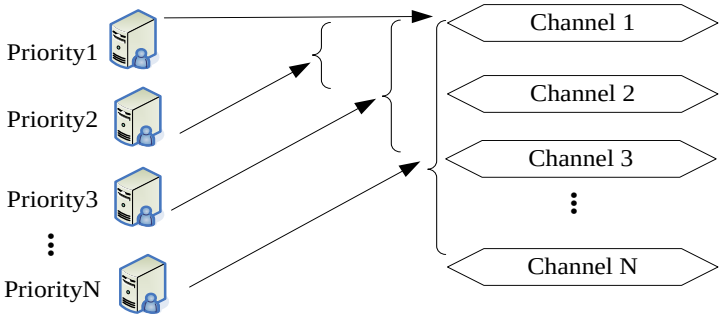

Fig. 2. Load balancing system model

Fig. 2 is the load balancing system model, the number of channels in the system is N, and there are N priorities. The order of priority is from priority to priority 1, priority 2... priority N and the number of users in each priority is unlimited. If a user is at priority x, its traffic is fixed to channel 1 to channel x. And the arrival rate of the priority y on channel x is $\lambda_y = \frac{G_x}{N-x+1}$ (y≤x). Since the system load is balanced, the utilization of each channel is $G_x = G \ \ (x = 1,2, \dots, N)$.

The throughput is the number of successful transmission of data per unit time in the network. The average power of the nodes is the criterion of system energy consumption. In order to give the theoretical value of the circuit simulation, the following describes the throughput and the average power of the node.

2.2 Analysis of system throughput

Before analyzing the protocol, the system is defined as follows:

Table 1.

Description of Symbol

Symbols	Description
x	The number of channels in the system
y	The number of priorities in the system
a	Length of idle slot
λ_x	The packet arrival rate on channel x
$E(I_x)$	Average length of idle events on channel x

$E(U_x)$	Average length of information packets sent on channel x
$E(BU_x)$	The average length of the information packet collision or successful transmission on channel x
S_{Py}	The throughput of Priority y

(1) The access mode of each channel is persistence CSMA, and the information packet arrival process on channel x satisfies the Poisson distribution [5] (x = 1, 2, 3 ... N) with independent parameterλ_x;
(2) The slot length of the channel idle is a, the slot length of the packet transmission is the unit length 1, which is an integer multiple of a;
(3) System load balance, the arrival rates of each channel are $\lambda_x = \lambda(x = 1,2, \dots, N)$.
(4) Assuming that the channel is ideal, no noise in the channel interference;
(5) Collision or abandonment of the transmitted message packet will be retransmitted at a later time, and the retransmitted packet has no effect on the arrival of the channel.
First, the average length $E(U)$ of the success of sending the event U in the x channel is solved, which consists of the following two parts:

(1) If an information packet arrives in the last slot of the idle period and it is only sent in the next slot, it will send successfully. this event is denoted as U_{x2} and its average length is $E(U_{x1})$:

$$\mathrm{E}(U_{x1}) = \left[\sum_{i=1}^{\infty}\left(1 - e^{-(1+a)\lambda_x}\right)^{i-1}\right]\left[\sum_{j=1}^{\infty}\left(e^{-a\lambda_x}\right)^{j-1}\right] e^{-(1+a)\lambda_x} a\lambda_x e^{-a\lambda_x} \quad (1)$$

(2) If the packet arrives in a busy cycle and the packet is the only packet that is to be sent in the current transmission cycle, this event is denoted as U_{x2} and its average length is $E(U_{x2})$:

$$\mathrm{E}(U_{x2}) = (1 + \mathrm{a})\lambda_x \quad (2)$$

Then the $E(U)$ is:

$$\mathrm{E}(U_x) = \mathrm{E}(U_{x1}) + \mathrm{E}(U_{x2}) \quad (3)$$

Next, the average length $\mathrm{E}(BU_x)$ of the busy period in the x-channel is solved:

$$\mathrm{E}(BU_x) = (1 + \mathrm{a})\sum_{i=1}^{\infty}\sum_{j=1}^{\infty} i\left(1 - e^{-a\lambda_x}\right)\left(1 - e^{-(1+a)\lambda_x}\right)^{i-1} e^{-(1+a)\lambda_x}\left(e^{-a\lambda_x}\right)^{j-1} \quad (4)$$

Finally, the average length of the idle period I_x of the x-th channel is solved $E(I_x)$:

$$E(I_x) = a\sum_{i=1}^{\infty}\sum_{j=1}^{\infty} j(1 - e^{-aG})\left(1 - e^{-(1+a)G}\right)^{i-1} e^{-(1+a)G}(e^{-aG})^{j-1} \quad (5)$$

In the system, because the channel load is balanced, there are $\lambda_x = \lambda\ (x = 1,2,\dots,N)$, according to the above analysis and throughput calculation, we can get the throughput of priority y:

$$S_{Py} = \left(\sum_{y=1}^{x} \frac{1}{N-y+1}\right) \frac{a\lambda_x e^{-(1+2a)\lambda_x} + (1+a)\lambda_x\left(1-e^{-a\lambda_x}\right)e^{-(1+a)\lambda_x}}{(1+a)(1-e^{-a\lambda_x}) + ae^{-(1+a)\lambda_x}} \quad (6)$$

2.3 Analysis of energy consumption

In order to obtain the mathematical expression of the power consumption of the system, the powers of three different states are set as:

(1) The power of sending isP_s;

(2) The power of listening isP_l;

(3) The power of receiving isP_r;

System power is divided into the following situations:

(1) Suppose that there are M nodes in the system, and only one terminal is ready to send data in idle slot. Then the power of the system is: $P_s + (M-1)P_r$
So in an average transmission cycle, the power of data is successfully transmitted as:

$$P_U = \frac{E(U)}{E(T)} * [P_s + (M-1)P_r] \quad (7)$$

(2) When there is no terminal decide to send packets in the idle slot, all terminals are listening to the channel. At this moment, the system power is MP_l.

$$P_I = \frac{E(I)}{E(T)} * MP_l \quad (8)$$

(3) Based on the above analysis, the time axis is divided by the average cycle time(I, BU, T), the system power of the channel collision as:

$$P_B = \left[E(B)P_s + \left(M - \frac{1}{E(B)}\right)P_r\right]\frac{1}{E(T)} \quad (9)$$

Therefore, in an average transmission cycle, the average power of the system is：

$$P_A = \frac{E(U)}{E(T)} * [P_s + (M-1)P_r] + \frac{E(I)}{E(T)} * MP_l + \left[E(B)P_s + \left(M - \frac{1}{E(B)}\right)P_r\right]\frac{1}{E(T)} \quad (10)$$

3. The design of system circuit

According to the characteristics of FPGA [6, 7], the implementation of multi-channel CSMA protocol needs to be modular design, the three-priority circuit system is analyzed as an example.

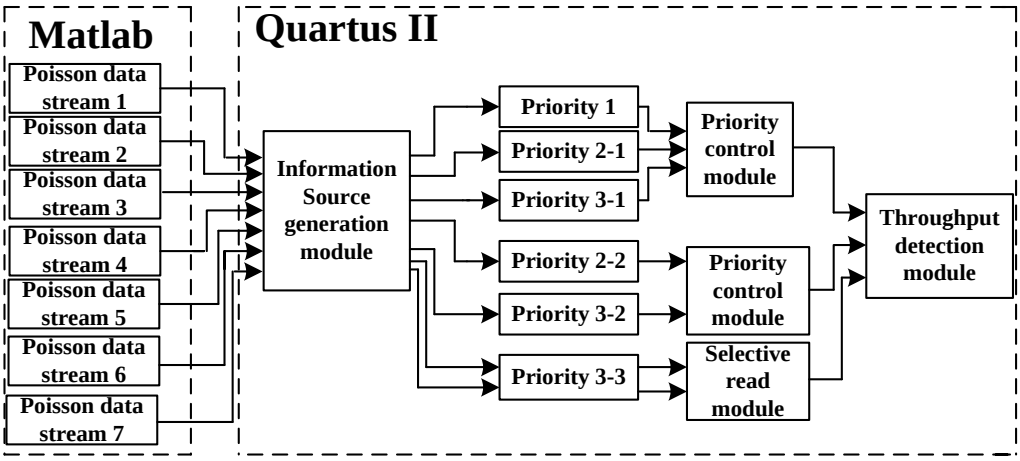

Fig. 3. Circuit diagram

Fig. 3 is the system circuit architecture. According to the principle of three-priority persistence CSMA protocol, the circuit consists of the Information Source generation module, the Selective read module, the Priority control module and the throughput detection module.

3.1 Information Source generation module

The design of the source is a difficult point in the hardware implementation of the MAC layer communication protocol. The key is that the circuit module cannot produce Poisson data stream. In order to solve this problem, combined with Matlab and Quartus II to build experimental platform, and according to the three-priority persistence CSMA protocol principle, when the number of channels is three, then priority 1, priority 2, priority 3 will be transmitted on channel 1; and Priority 2, priority 3 will be transmitted on channel 2, and priority 3 will be transmitted on channel 3. Therefore, as shown in Fig. 1, in the Matlab need to generate multiple Poisson data flow to represent the priority data. The following is a process for a priority data generation.

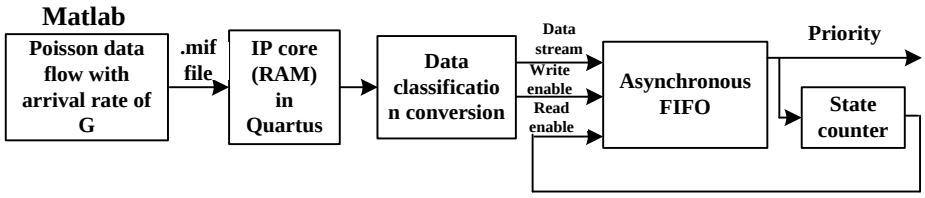

Fig. 4. Information Source generation module

Fig. 4 is the information source generation module; we can see that Poisson data stream is generated in Matlab, and then save the data stream as. Mif file format, through the Quartus IP core (RAM) to read, so the Poisson data stream is successfully introduced into the circuit. But this data does not meet the requirements of the agreement, so the data need classification conversion and time slot control.

According to the arrival rate of Poisson function in Matlab, the data information will fluctuate between different values, and according to the principle of the protocol, 0 represents no data, 1 represents a single data arrives, and other represents multi-data arrives, so these three information states are represented by multi-bit bit width data. The design uses 8-bit wide for data classification conversion. For example: 0000_0000, 0000_1000, 0000_1001 represent the above three states.

In the 1.2 analysis of protocol throughput, the slot length of the idle has been defined as a, the slot length of the packet transmission is the unit length 1, which is the integer multiple of a. But the data length of each data state through data classification is equal, and does not meet this multiple relationship, so these data need to be time slot length control.

The asynchronous FIFO [8] operation has a characteristic that when the write enable remains active, the read enable is changed from valid to invalid, and the soutput information will remain the last unique data. According to this feature, when the counter detects that the data state is no data, the read enable of the asynchronous FIFO is enabled; when the other data status is detected, the read enable is disabled and the read enable recovery is controlled by counting. The time slot of this count is the length of the success and collision state, so the priority is generated.

3.2 Priority control module

There are multiple data stream contention channels on channel 1 and channel 2. Aiming at this problem, the Priority control module is designed according to the principle of persistence CSMA. Taking channel 2 as an example, priority 2 and priority 3 will compete for the channel to transit the respective data, so first use different values to represent the two priorities of the respective data.

Therefore, it is necessary to use different values to represent the respective data status of the two priorities.

Table 2.

Priority data status on channel 2

Status / Priority	no data	Single data	Multiple data
2	0000_0000	0000_0110	0000_0111
3	0000_0001	0000_1000	0000_1001

As shown in Table 1, (0, 6, 7) and (1, 8, 9) respectively represent the three data states of priority 2 and priority 3. When the two priorities have no data, then channel 2 is idle; when one of the two priorities is the status of single data and other is no data, the channel 2 is the state of successful transmission; the rest is the state of information conflict, which reflects the multiplexing channel based on the persistence CSMA protocol control strategy.

3.3 Select the read module

The highest priority 3 is singly transmitted on channel 3. There are two states in the channel: channel idle, channel busy (joint event of success and collision); therefore, in order to realize the information packet competition in the single channel, to reflect the two events, an information site is divided into an idle site and a busy site.

These Poisson data streams are derived from two Poisson data streams in Matlab. The arrival rates areλ_1, λ_2, and $\lambda_1 + \lambda_2 = \lambda_o$. So, a Poisson data station with a reaching rate of λ_o is generated. And the selective reading module selectively reads the information data of the idle or busy station according to the real-time data (I, U, B) on the channel, so that the circuit not only completes the function of the listening channel, but also realizes the persistence CSMA Protocol control mechanism on single-channel.

3.4 Throughput detection module

This module consists of three self-incrementing counters, which are used to count the number of successful data slots on the three channels.

$$S = \frac{N_U * T_{BU}}{T} * \frac{1}{1+a} \qquad (11)$$

Equation (11) is a statistical method of throughput experiment results. The T is the total length of the simulation, N_U is the number of successful data transmission time slot in circuit simulation, T_{BU} is the channel busy time slot length, the length of time slot is to send a packet length in the algorithm in the

protocol (TP), the theoretical value is 1+a, and successful slot length is 1. Therefore, in the calculation of state long success should be multiplied by $\frac{1}{1+a}$ ratio.

3.5 The advantages of circuit design

The advantage of design is shown in the Table 3:

Table3.

Advantages of circuit design

key point	Details of the key points
Arrival rate value	Based on MATLAB and Quartus II, this design solves the problem of Poisson source generation and does not generate the approximate Poisson by pseudo-randomness, which improves the accuracy of the system. In the process of experiment simulation, the value λ can be adjusted in the poissrnd function of the Matlab software, the convenience of the experiment is greatly improved.
Control mode of Time slot length	Combined with the FIFO kernel and counter module (Verilog), can be controlled in accordance with the integer multiple relationship between the length of idle state a and the length of busy state 1, and this multiple relationship can be arbitrarily adjusted in the counter module program;
The ability to reshape	The whole design of the circuit adopts the modular design. The design takes the three-channel data transmission as an example, can realize the protocol control mechanism, the structure is simple, the remodeling is strong, and the data transmission system with any number of priority can be shaped quickly.

4. System testing and analysis

The simulation experiment of this design is used to test the throughput of multi-channel persistence CSMA. In the first section, the test of the throughput theory has been obtained. The arrival rate of all priorities in the experiment is set in the Poisson function in Matlab. The relationship between the timeslot lengths in the different states of the information can be adjusted in the counter program of the information source generation module.

Table 4.

Simulation parameters

Parameter Description		Value
System minimum clock cycle	T_m	10ns
System simulation time	T	500us
Idle slot	a	0.1
Length of Idle time slot	T_I	80ns

Length of Busy time slot	T_{BU}	800ns
Priority 1 arrival rate	λ_1	1/6
Priority 2_1 arrival rate	$\lambda_{2\ 1}$	1/2
Priority 3_1 arrival rate	$\lambda_{3\ 1}$	1/3
Priority 2_2 arrival rate	$\lambda_{2\ 2}$	1/2
Priority 3_2 arrival rate	$\lambda_{3\ 2}$	1/2
Priority 3_3 arrival rate	$\lambda_{3\ 3}$	1

Table 4 is the parameters of system simulation, the minimum inherent length of Quartus II software simulation is 10ns, if the idle time slot is 0.1, then the busy time slot length is 1, so there is a 10-times relationship between the two states, and this relationship is convenient for design and final statistics. In the source generation module, the Poisson sequence in Matlab is introduced into the circuit through the eight-bit conversion, so the data is 80ns, and the busy data is processed by the priority module slot, the time slot is expanded by 10 times, so the busy slot length is 800ns. The simulation time(500us) can reflect fifty thousand minimum simulation emulation clock cycle,which is enough to test the design. When the multi-priority system is equalized, the total packet arrival rate on each channel should be the same, and the arrival rate of the high priority on the low channel is assigned according to the formula $\lambda_y = \frac{G_x}{N-x+1}$, so $\lambda_1 = 1/6$, $\lambda_{2\_1} = 1/2$, $\lambda_{3\_1} = 1/3$, λ_{2_2}=1/2, λ_{3_2}=1/2, and $\lambda_1 + \lambda_{2\_1} + \lambda_{3\_1} = 1$, $\lambda_{2\_2} + \lambda_{3\_2} = 1$, the priority 3 transmits information on channel 3 alone, so $\lambda_{3-3} = 1$.

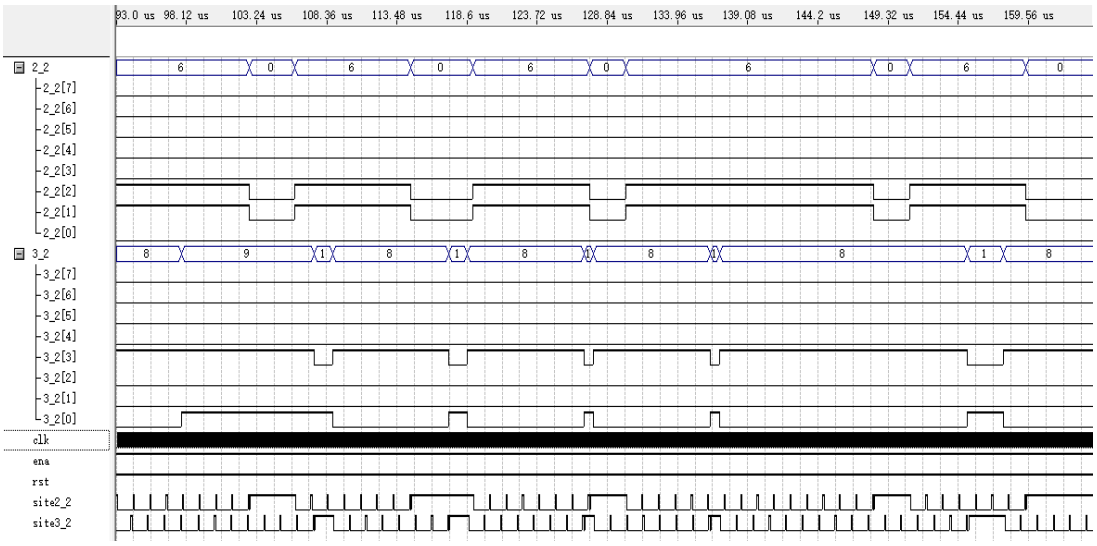

Fig. 5. Data state simulation

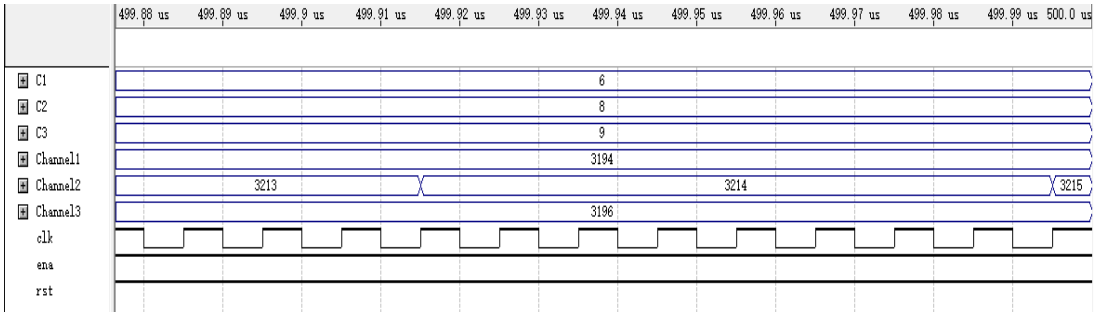

Fig. 6. Circuit simulation results

When the arrival rate is 1, the throughput theoretical value of the system is optimal, which is an important test point in the design, so the total arrival rate in each channel is set to 1.

Table 2 has set (0,6,7) and (1, 8, 9) to represent the three data arrival states (I,U,B) of priority 2 and priority 3 on channel 2. Fig. 5 is the data processed by the source processing module, 2_2 and 3_2 show the priority 2 and priority 3 real-time transmissions of data, which the slot length of idle data and non-idle data has an integer multiple of relationships, which is consistent with the original intention of the design. As shown in Fig. 6, Channel 1, Channel 2, Channel 3 is the number of data transmission success status on the three channels.

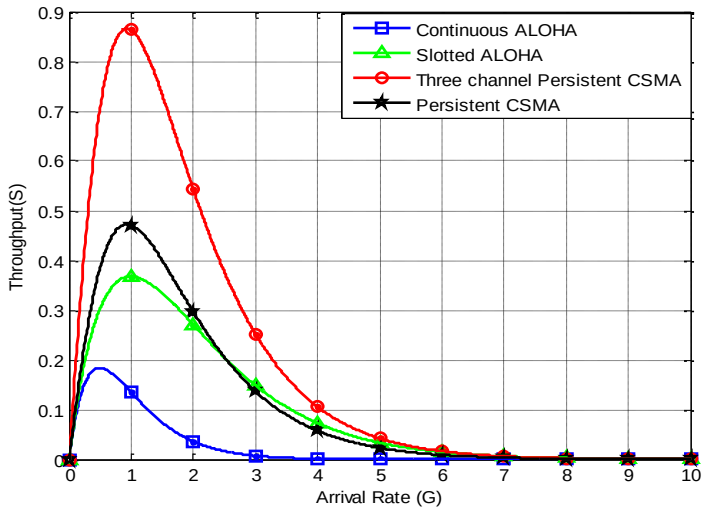

Fig. 7. The throughput of the protocol and other protocols

The Table 4 is the hardware simulation parameters, the final system channel 1, channel 2, channel 3 throughput statistics number is 3194,3215,3196; the simulation calculation of the throughput values was 0.4645, 0.4676, 0.4648,

and which is consistent with the theoretical value 0.4709, proved that the protocol design is correct. Fig. 7 is the comparison of the theoretical and statistical values of the throughput of the three channels CSMA and other protocol systems, and the statistical values of the throughput of each MAC layer protocol are all on the theoretical values. It can be seen from the diagram that the throughput of the protocol is much higher than that of other protocols.

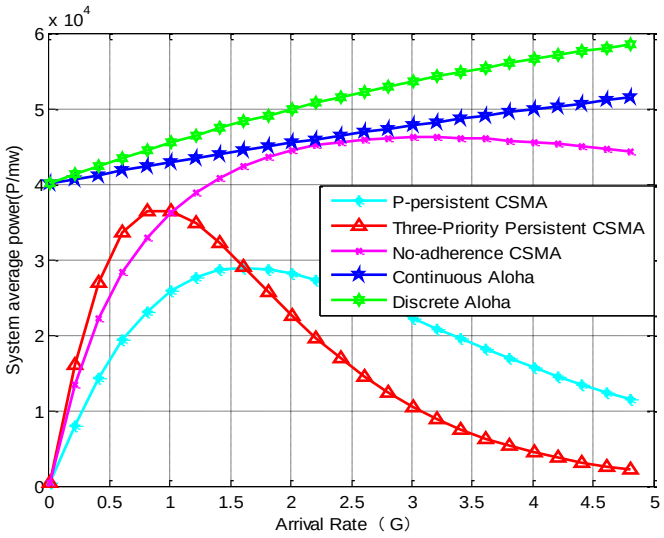

Fig. 8. Comparison of average power of multiple MAC protocol

Fig. 8 is a comparison of the average power of the three-priority persistence CSMA and other protocol system. It can be observed that the average power statistics of the system are in the theoretical curve in the range of the system arrival rate, and the three-priority persistence CSMA protocol system has lower average power than the other MAC protocols, which proves that the protocol can effectively reduce the communication System energy consumption.

5. Conclusions

In this paper, according to the working characteristics of wireless sensor networks, FPGA is used to design the three-priority CSMA protocol access system. The design not only combines Matlab and Quartus II software to introduce the Poisson data stream into the circuit, but also its working principle is mapped to the circuit system according to the characteristics of the communication protocol algorithm. The simulation results show that the simulation value of the system throughput and average power are consistent with the theoretical value, which verifies the accuracy and stability of the design.

FPGA as a form of hardware, through its implementation of the communication protocol algorithm, the reality of the node transmission process is realized in the hardware parallel circuit, which is a process from the theory to the practice, and have very great help to improve the understanding of the theory of communication protocol.

Acknowledgments

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