SOFTWARE IMPLEMENTATION OF FIVE LEVEL INVERTER

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În această lucrare se prezintă structura de invertor cu cinci niveluri de tensiune 5L-ANPC-CI. Este propusă o metodă de simulare care ulterior este verificată prin intermediul unei implementări experimentale utilizând un microcontroler industrial. Rezultate obținute prin simulare şi prin modelare experimentală sunt prezentate şi comparate pentru a valida metoda folosită.

In this paper the inverter with five voltage levels 5L-ANPC-CI is presented. It also proposes a simulation method that verifies a digital implementation using an industrial microcontroller. Results obtained by simulation and by experiment are presented and compared in order to validate the method used.

Keywords: coupled inductor, microcontroller, multilevel inverter

1. Introduction

MULTILEVEL conversion structures represent a solution to improve the performances given by the classical structures with two voltage levels. Semiconductor devices with a high voltage rating have an increased price. Multilevel structures offer a reduction of the voltage stress that compensates the increased number of devices. Also these structures offer the advantage of reducing the size of the output filter by reducing the total harmonic content [1]-[3].

An important structure is the Active Neutral Point Clamped Converter (ANPC) developed in 2001. It presents the advantage of an increased number of degrees of freedom [4]-[6]. Also it allows the combination with other concepts in order to create structures with higher number of voltage levels and output parameters. Another class of multilevel converters introduces the coupled inductor concept [7]-[9]. This type of converters offer an increased number of voltage levels, lower current stress in the semiconductor devices and better output voltage properties. In order to combine the advantages given by the structures that do not use the coupled inductor concept and those that do, a hybrid structure was developed [10].

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In order to create a valid prototype, very accurate simulations are necessary. This paper presents a simulated implementation of the control of the Five-Level-Active-Neutral-Point-Clamped-Coupled-Inductor (5L-ANPC-CI) converter that gives the same results as the practical implementation using the microcontroller dsPIC30F6010 from Microchip and the digital environment Mplab [11]. Simulated and experimental results are given in order to prove the advantages of the control method used.

2. Structure presentation

This structure is made from the three level bidirectional cell (3L-B) and two parallel basic commutation cells (2L-B) connected with a coupled inductor that form the 3L-CI cell [10]. From the combination between the 3L-B cell and the 3L-CI cell results a structure with five voltage levels, made from eight switches and one coupled inductor (Fig.1).

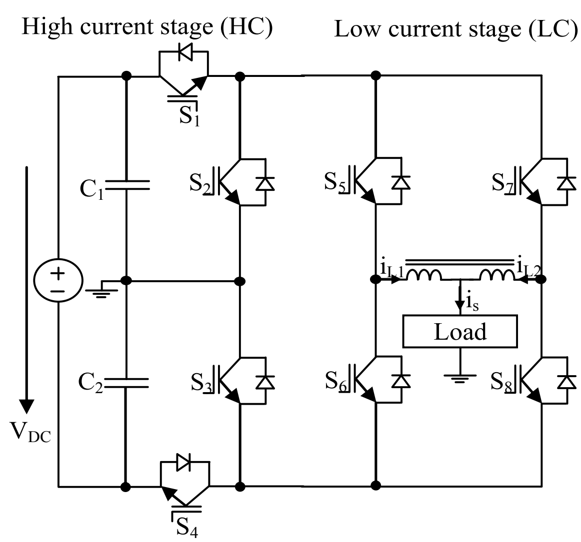


Fig.1. Five-level ANPC-CI inverter.

The eight transistors are complementary controlled: S_1-S_2, S_3-S_4, S_5-S_6 and S_7-S_8. The devices from the 3L-B cell, S_1-S_2 and S_3-S_4 switch with the frequency of the reference wave and form the high current stage (HC). The devices from the 3L-CI cell, S_5-S_6 and S_7-S_8 switch with the frequency of the carrier wave and form the low current stage (LC).

The PWM control for the HC stage is obtained from the direct comparison of the reference wave (S_r) and zero, while the control of the LC stage is obtained from the comparison of the reference voltage modulus (S) with two carrier waves

(C_1 and C_2) phase-shifted with half of the switching period (Fig.2).

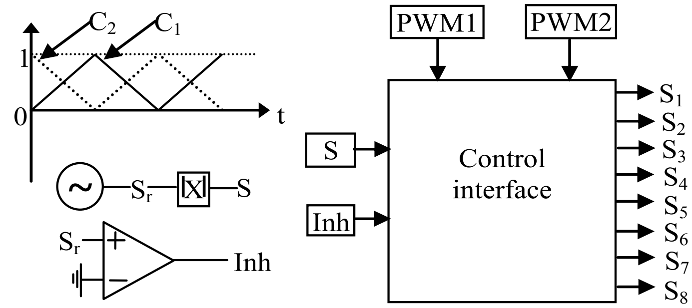


Fig.2. PWM control of the 5L-ANPC-CI converter.

The coupled inductor from the 3L-CI cell is used to create the five voltage levels and to divide the load current through the LC stage (1). As a result the current in each device from the 3L-CI cell is half of the load current, a fact that leads to the reduction of the conduction and switching losses.

$$I_{L1} = I_{L2} = \frac{I_s}{2} \tag{1}$$

In (1), IL1 and IL2 are the current through the coupled inductor, while Is is the load current.

The apparent switching frequency (f_{ap}) of the output voltage is two times larger than the switching frequency (f_{sw}) (2), a property that leads to the reduction of the total harmonic distortion (THD) and of the output filter required.

$$f_{ap} = 2 * f_{sw} \tag{2}$$

3. Simulation setup

In order to create an experimental control using an industrial microcontroller it was necessary to make firstly a simulation that contains all the elements needed for the software implementation: counter, carrier wave, reference wave, PWM control logic.

In Fig.3 it is presented a circuit that creates a counter (Cnt) and a sampling signal (Spl). The Spl signal is made in order to sample the two reference waves on each moment the counter has the value zero. It is used an up/down counter of 16 bits with the frequency of the internal clock of 29.4 MHz. When the U/D input has the value zero the counter decrease. The reset input (R) brings the counter to zero when it is active. Because the system can not start immediately it was used a step signal that keeps the counter blocked for 10 µs. Also it sets a D flip-flop so that the Spl signal will start after the first 10 µs at the exit port of the monostable

(Mon). Regarding of the required frequency for the carrier wave, the counter change the count direction when it reaches the minimum value zero or one of the following maximum values: 1474 for 10 kHz, 2949 for 5 kHz, 5899 for 2.5 kHz or 11799 for 1.25 kHz.

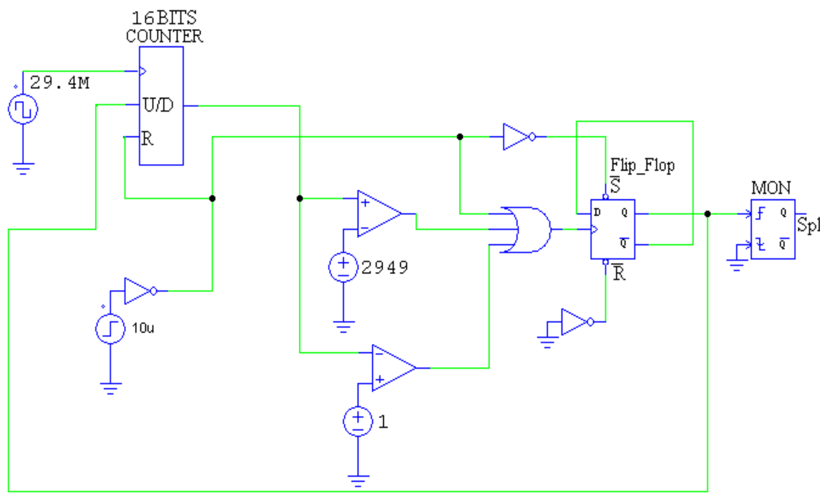


Fig.3. Carrier wave realization.

After the realizations of the carrier wave it was necessary to simulate the control of the S_1-S_4 devices with a dead time margin, the reference wave R and the two resulted modulus waves RA and RA1 (Fig.4). The dead time is made by using two monostables and it was set to 1 µs. The two reference waves are sampled using a sample and hold block controlled with the frequency of 50*1024 Hz. The resulted reference waves are compared with the previous obtained carrier wave in order to create the PWM signals: PWM1 and PWM2 (Fig.4). The carrier wave is delayed with 1 µs in order to better simulate the working mode of the microcontroller used in the real application.

By combining the circuits from Fig.3, Fig.4 and by using PWM1 and PWM2 it results the discrete control of the 5L-ANPC-CI converter. Simulation results are presented in Fig.5 and Fig.6. In Fig.5 the five level output voltage (V_0) and the sinusoidal load current (i_{load}) are presented.

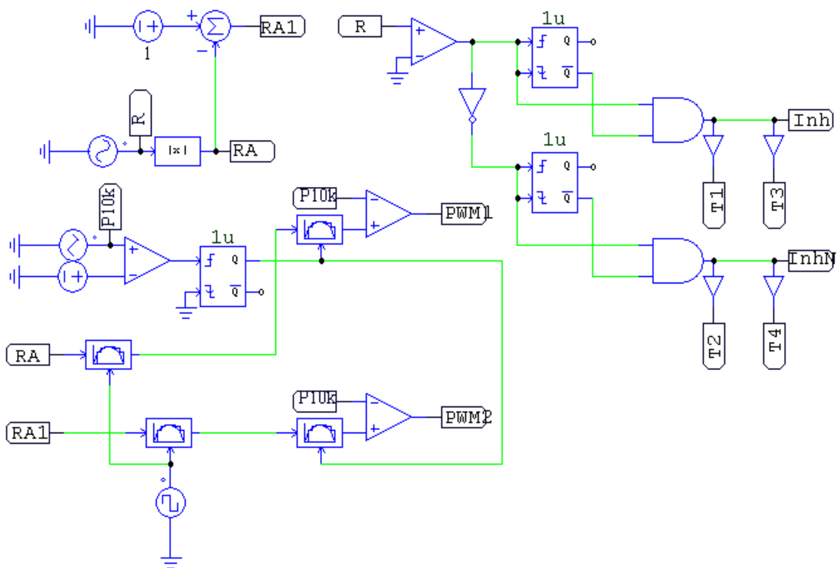


Fig.4. Realization of the reference waves, the PWM1 and PWM2 signals and the control of the T_1-T_4 devices.

The output voltage has a total harmonic distortion factor (THD) of 0.32%.

Fig.6 presents a zoom in order to show the ripple of the currents through the coupled inductor. The resulted ripple has the value of 2.5%.

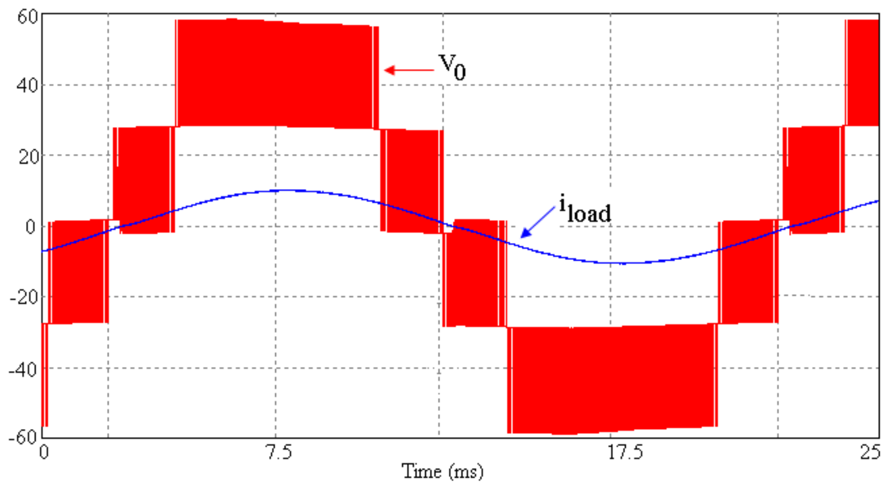


Fig.5. Simulated output voltage (V_0) and current (i_{load}).

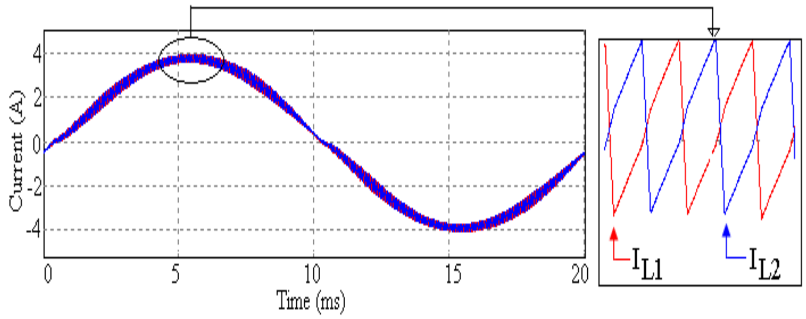


Fig.6. Simulated currents through the coupled inductor: I_{L1} and I_{L2}.

4. Software implementation

The microcontroller used is the dsPIC30F6010 from Microchip [11]. Its PWM module is able to generate eight PWM outputs, PWM1H/PWM1L to PWM4H/PWM4L with different modulation indexes, a maximum resolution of 16 bits and saw tooth or triangle carrier waves. It has the following registers that have to be defined by the user: PTCON (PWM Timerbase Control Register), PTMR (PWM Timebase Count Register), PTPER (PWM Timebase Period Register), PWMCON1 (PWM Control Register 1), DTCON 1 (PWM Dead Time Control Register 1) and PDC1 (PWM Duty Cycle Register 1).

Choosing the parameters for the MPLAB implementation

The PTCON register must be initialized, so Bit5 must take the value 1. The up-down counting mode was chosen, so according to the datasheet the PTMOD register must take the value two, which means that Bit1=1 and Bit0=0 of the PTCON register. Also the prescale value of 1:1 was chosen so the prescale register PTCKPS must take value zero. From these considerations results the value of the PTCON register: 1000|0000|0000|0010 in binary or 8002 in hexadecimal.

The PWM frequency (f_{sw}) depends on the value of the PTPER register, the oscillator internal clock (T_{CY}) and the prescale value (PTCKPS) (3).

$$f_{sw} = \frac{PTCKPS}{T_{CY} * (PTPER + 1)} \quad (3)$$

Four frequencies were implemented in the experimental model: 1.25 kHz, 2.5 kHz, 5 kHz and 10 kHz. The internal clock has the period of 33.9 ns. The maximum value of the modulation index must be limited to 0.995, which leads to the following values for the PTPER and PDC1 registers:

f_{sw} = 1.25 kHz: PTPER = 11799, PDC1 = 23500
f_{sw} = 2.5 kHz: PTPER = 5899, PDC1 = 11700
f_{sw} = 5 kHz: PTPER = 2949, PDC1 = 5800
f_{sw} = 10 kHz: PTPER = 1474, PDC1 = 2940

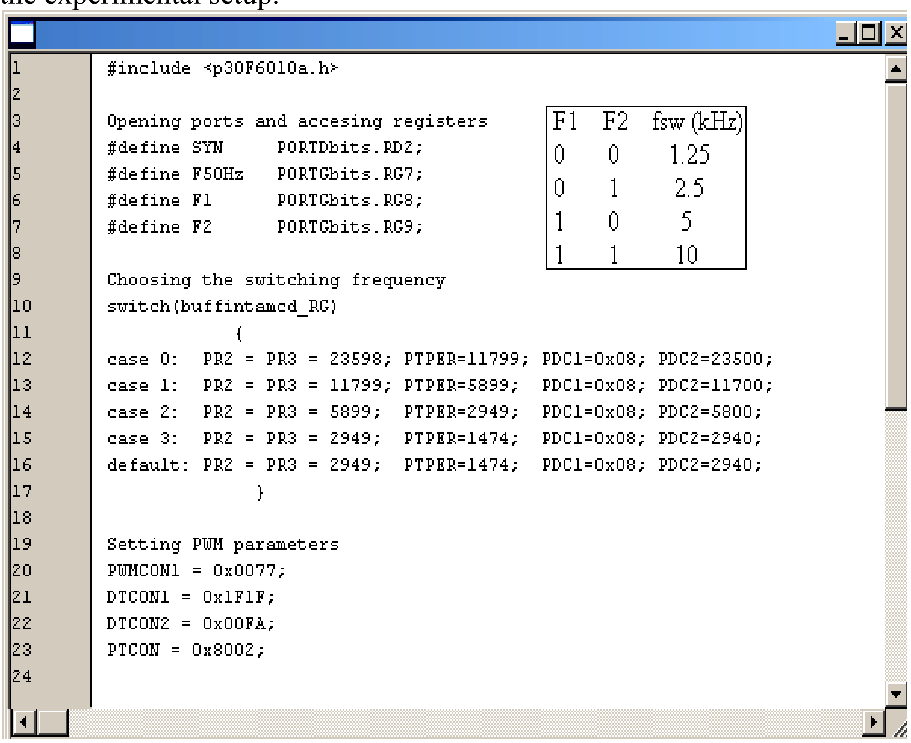
Because three PWM outputs are used, the bits zero to six of the register PWMCON1 must have the value one, while the others are zero: 0000|0000|0111|0111 in binary or 0077 in hexadecimal.

The dead time value (DT) depends on the prescale value (T_{CY}), the value of the dead time register (DTCON) and the internal clock T_{CY} (4).

$$DT = DTCON1 * T_{CY} * PTCKPS \quad (4)$$

Taking into consideration a normal dead time value of 1 μs results the hexadecimal value of 31 that must be written in the DTCON1 register for all the PWM outputs.

By entering these values into an Mplab program (Fig. 7) results the control for the experimental setup.



```
#include <p30F6010a.h>

Opening ports and accesing registers
#define SYN     PORTDbits.RD2;
#define F50Hz   PORTGbits.RG7;
#define F1      PORTGbits.RG8;
#define F2      PORTGbits.RG9;

Choosing the switching frequency
switch(buffintamcd_RG)
            {
case 0:  PR2 = PR3 = 23598; PTPER=11799; PDC1=0x08; PDC2=23500;
case 1:  PR2 = PR3 = 11799; PTPER=5899;  PDC1=0x08; PDC2=11700;
case 2:  PR2 = PR3 = 5899;  PTPER=2949;  PDC1=0x08; PDC2=5800;
case 3:  PR2 = PR3 = 2949;  PTPER=1474;  PDC1=0x08; PDC2=2940;
default: PR2 = PR3 = 2949;  PTPER=1474;  PDC1=0x08; PDC2=2940;
             }

Setting PWM parameters
PWMCON1 = 0x0077;
DTCON1 = 0x1F1F;
DTCON2 = 0x00FA;
PTCON = 0x8002;
```

F1	F2	fsw (kHz)
0	0	1.25
0	1	2.5
1	0	5
1	1	10

Fig.7. Sample of the software implementation in Mplab.

In this sample program, F1 and F2 are two bits that allow the user to choose the switching frequency, SYN is one of the sinusoidal waves that are compared with the carrier wave and is generated by using a numerical table, while F50Hz is an input that sets the normal frequency for the reference wave.

5. Experimental setup

A test low-voltage experiment has been made in order to validate the operation mode of the single-phase 5L-ANPC-CI converter with a RL load (R = 6 Ω, L = 2 mH). The power semiconductors IGBT SKM75GB124D from SEMIKRON are rated for 1200 V and 75 A. The supply voltage Vdc has been limited to 136 V and the dead time has been set to 1 μs. In order to create the connection between the dsPIC30F6010 microcontroller and the Mplab environment an experimental board was made (Fig.8).

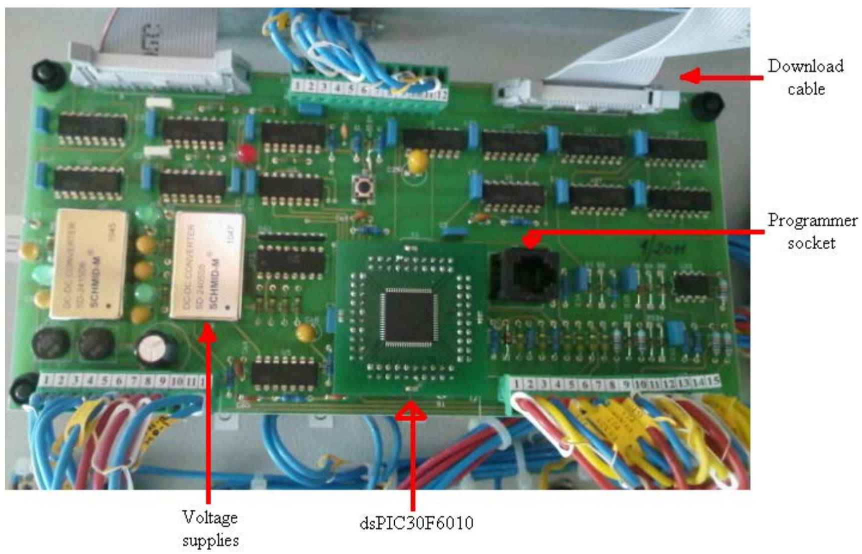


Fig.8. Experimental microcontroller board.

Experimental results are given in Fig.9 and Fig.10 in order to compare with the simulated results from Fig.5 and Fig.6. The experimental waveforms were acquired by using the TDS 2014B four channel digital storage oscilloscope from Tektronix.

In Fig. 9 the output voltage (V_0) and the load current (i_{load}) are presented. Because of the increased number of levels, the output voltage has a low harmonic content that translate into a low output filter. Also the two waves are similar to the results presented from the simulation setup.

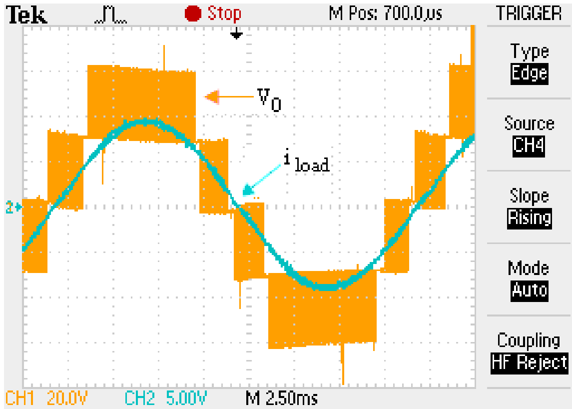


Fig.9. Experimental waveforms: output voltage V_0 and load current i_{load}.

In Fig.10 the load current and the two coupled inductor currents, i_{L1} and i_{L2} are presented. The two currents that pass through the coupled inductor are half of the load current as it was shown in (1). Also they have the same ripple and are in a perfect balance as it was also showed in Fig.6 from the simulation model.

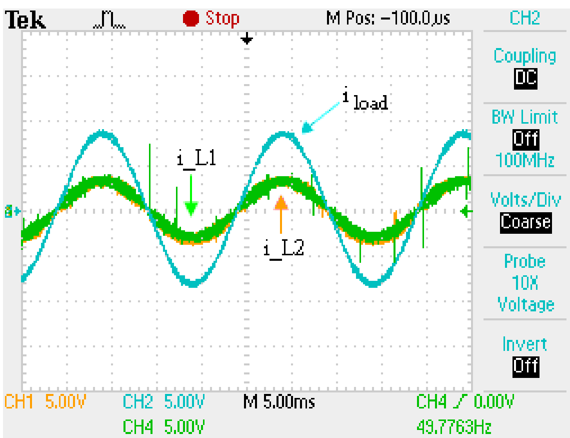


Fig.10. Experimental waveform: load current i_{load} and coupled inductor currents i_{L1}, i_{L2}.

6. Conclusions

In this paper a software implementation of a five level coupled inductor converter was presented. It has the advantage of simplicity and a low price cost required for the microcontroller. First a simulated control model is presented in order to better understand how the microcontroller dsPIC30F6010 from Microchip used in the experimental setup works.

Simulated and experimental waveforms were presented and compared in order to validate the proposed software implementation control method.

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R E F E R E N C E S

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