A NEW GENERATION OF SPEED GOVERNORS FOR KAPLAN TURBINES

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The paper presents the prototype of a new generation of speed governors for KAPLAN turbines created by the authors with the new FPGA technology and the real time operation system LabVIEW. The control software was implemented on the new industrial computer family CompactRIO developed by the NATIONAL INSTRUMENTS corporation. This embeded and reconfigurable controller can be widely used in different SCADA systems. The new hardware and software configuration was validated on an industrial KAPLAN turbine controlled by a speed governor designed in the Fluid Power Laboratory of the University POLITEHNICA of Bucharest.

Keywords: hydraulic turbine, speed governor, SCADA system, FPGA technology

1. Introduction

The modern speed governors for hydropower units must respond to ever increasing requirements regarding performance, reliability and safe operation in the frame of the *Union for the Co-ordination of Transmission of Electricity* [1]. In Romania a great progress in this matter was achieved in 2003 by the research team of the Fluid Power Laboratory of U.P.B. which installed a modern patented electrohydraulic speed governor in the Râmnicu Vâlcea Hydropower Station [2], [3]. The main features of this speed governors is the promotion of a new generation of high speed, high flow, two stages electrohydraulic proportional servovalves [4], and a new generation of high speed digital controllers based on Sharc Digital Signal Processor [5] .

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In this paper, the authors present the architecture and performances of a new digital speed governor, built around a National Instruments CompactRIO industrial computer [6], taking the advantage of the FPGA technology [7].

2. General assessment of the FPGA and NI cRIO technology

Field-programmable gate arrays (FPGAs) are reprogrammable silicon chips [8]. This allows them to have the same flexibility of software running on a processor-based system, but not be limited by the number of processing cores available. Unlike processors, FPGAs are truly parallel in nature, so different processing operations do not have to compete for the same resources. Each independent processing task is assigned to a dedicated section of the chip, and can function autonomously without any influence from other logic blocks. As a result, the performance of one part of the application is not affected when you add more processing. It also means that the application logic operates at a much lower level (directly in hardware circuits), as opposed to a traditional processor system, where an application usually runs on top of an operating system and various device driver (fig.1). This translates directly into a much shorter response time and increased processing speed.

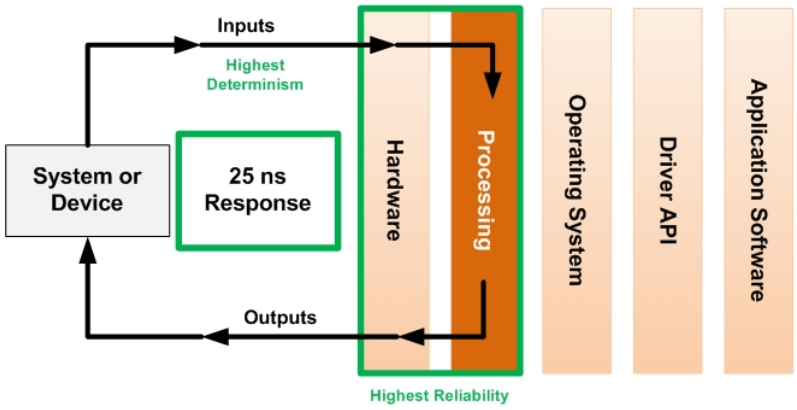

Fig. 1. FPGA circuit operation [6]

Additionally, the fact that the application is written directly in a FPGA circuit (which can not be erased or reprogrammed without specific external tools and commands) makes it a lot less susceptible to possible bugs and errors that inevitably occur when running traditional software.

The main trade-offs when using FPGA technolgy revolve around I/O connectivity and programming difficulties. It is impossible to install generic device drivers on an FPGA chip, as the drivers need to be ‘wired’ into the

hardware structure of the chip, which makes programming application I/O interfaces a tedious process. This is further complicated by the difficulty of using traditional low-level FPGA programming tools, like VHDL. This code is usually lengthy, and writing, understanding or testing it requires advanced chip architecture knowledge, which not many engineers from the various fields where FPGA implementation would be beneficial possess.

In order to eliminate these downsides, the authors have chosen to use a National Instruments CompactRIO architecture together with LabVIEW software. The NI RIO platform is a hybrid, also called *heterogeneous architecture* in literature, which combines an x86 processor with an FPGA chip, connected by a PCI data bus. The x86 system handles routine tasks (system clock, read/write operations to disk etc.) and most I/O connections with network or peripherals, but it's also fully capable of running any needed software. Therefore, the whole the FPGA chip is free to run application logic.

The LabVIEW programming environment is distinctly suited for FPGA programming because it clearly represents parallelism and data flow, so users who are both experienced and inexperienced in traditional FPGA design processes can leverage FPGA technology. Additionally, it allows all tasks (design, deployment to FPGA chip and testing) to be performed directly from the graphical interface. If needed, integration of existing VHDL code is also supported.

3. Speed governor structure

In order to assess the performance of using FPGA technolgy in the speed governors for hydropower units, the authors, working in the Fluid Power Systems laboratory of the Hydraulics, Hydraulic Machinery and Environmental Engineering Department of University POLITEHNICA of Bucharest have developed an original (patentable) solution. The software, named RAV-cRIO, has the following structure. The modular architecture of the cRIO platform allowed an effective distribution of tasks between the x86 processor and the FPGA chip. The critical part of the system, which consists of 3 digital controllers (PI RAV for the speed governor, PID AD for the wicket gate servomechanism and PID PR for the rotor blades servomechanism) has been implemented on the FPGA chip, for maximum reliability and speed in execution, while the x86 processor handles parameter monitoring, network communication and generic plant automation tasks. The I/O modules receive the following parameters: position of the wicket gate servomotor, position of the rotor blades servomotor, achieved turbine speed, desired turbine speed, and head. This information is 'read' by the FPGA module and either used in modules on the chip, or redirected toward the x86 system, as shown in fig. 2. The cRIO then outputs the command signals for the wicket gate and rotor blade servomechanisms.

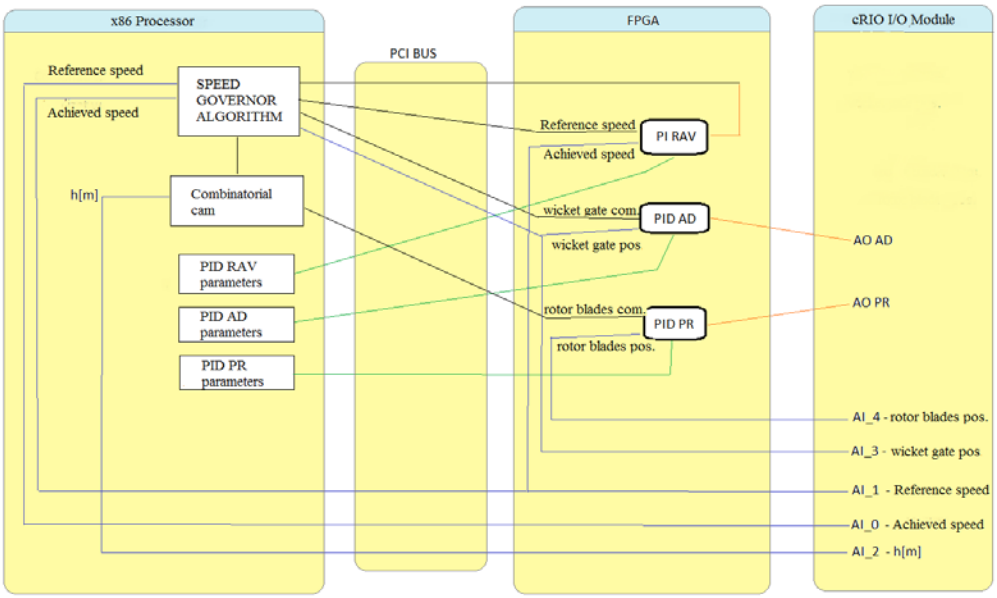

Fig. 2. RAV-cRIO software structure

The parameters for the 3 controllers are defined by the x86 unit. They are initialized with a default set of values but can be altered locally or via a TCP/IP connection by a remote monitoring system, referred to as Host in the software.

The software consists of 3 interdependent programs, running on the Host, on the x86 processor, and on the FPGA chip.

To insure better integration between them, they were developed using a single project in the LabVIEW environment (fig. 3) and the communication between them has been implemented using *shared variables* (specific type of data available in LabVIEW). Each application consists of a block diagram and a front panel. Fig. 4 and 5 show the front panel of the x86 processor software, while figures 6 and 7 show the same for the FPGA software.

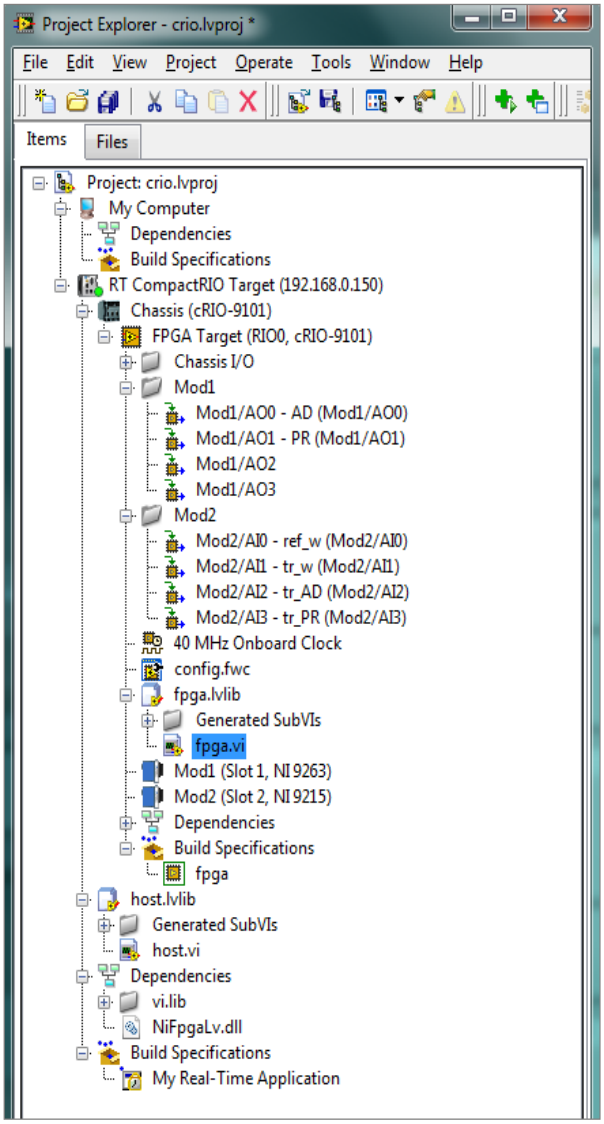

Fig. 3. RAV-cRIO project in LabVIEW

The authors have also developed a test software that allowed to verify that the response of the speed governor algorithm meets the desired design goals.

The testing routine was the following: ramp signals in the 0…100% have been used as the required position of the wicket gate servomechanism. Then the head has been set to 2.5, 4.0, 6.0 and 8.0 m according to Table 1.

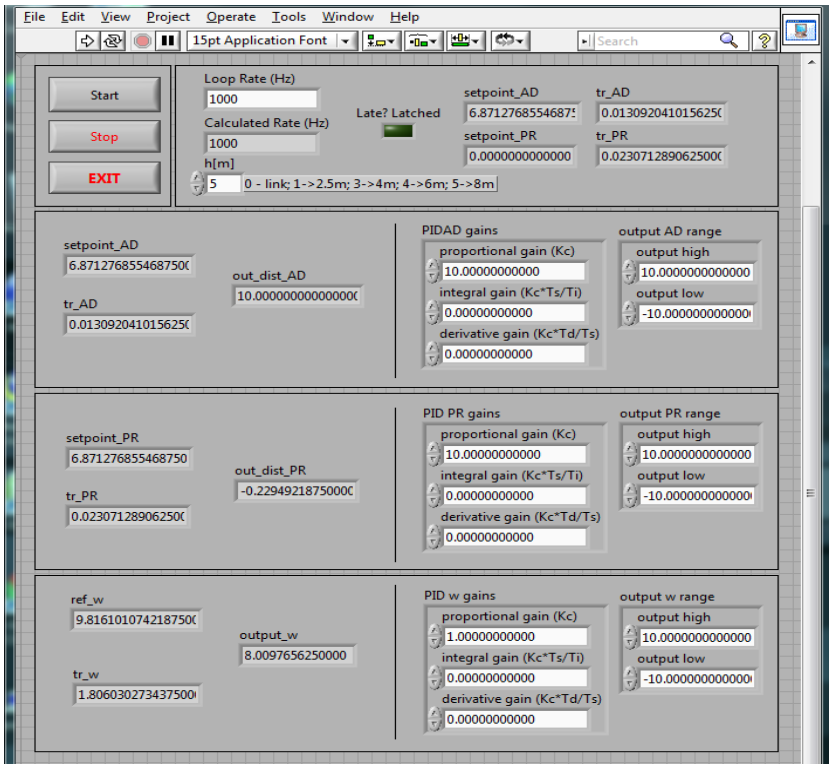

Fig. 4. x86 software front panel

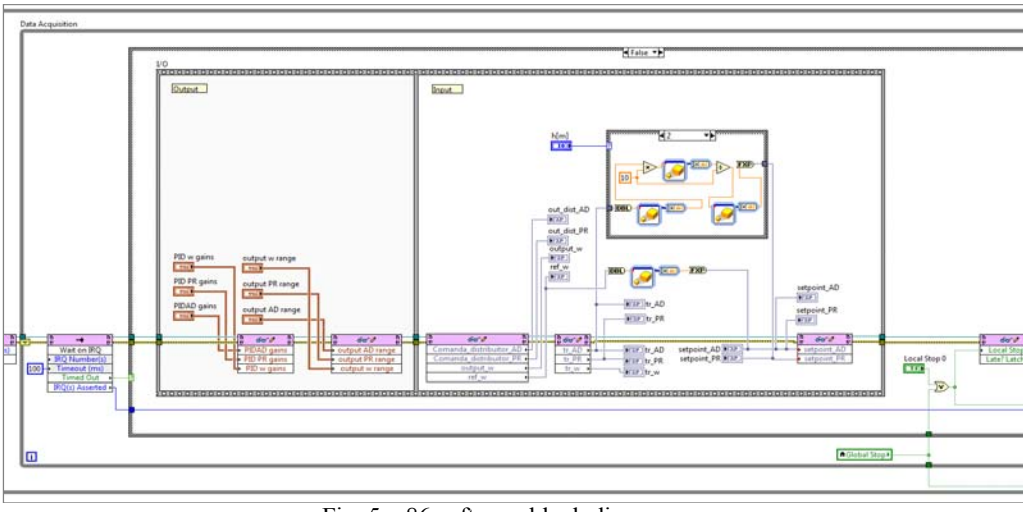

Fig. 5. x86 software block diagram

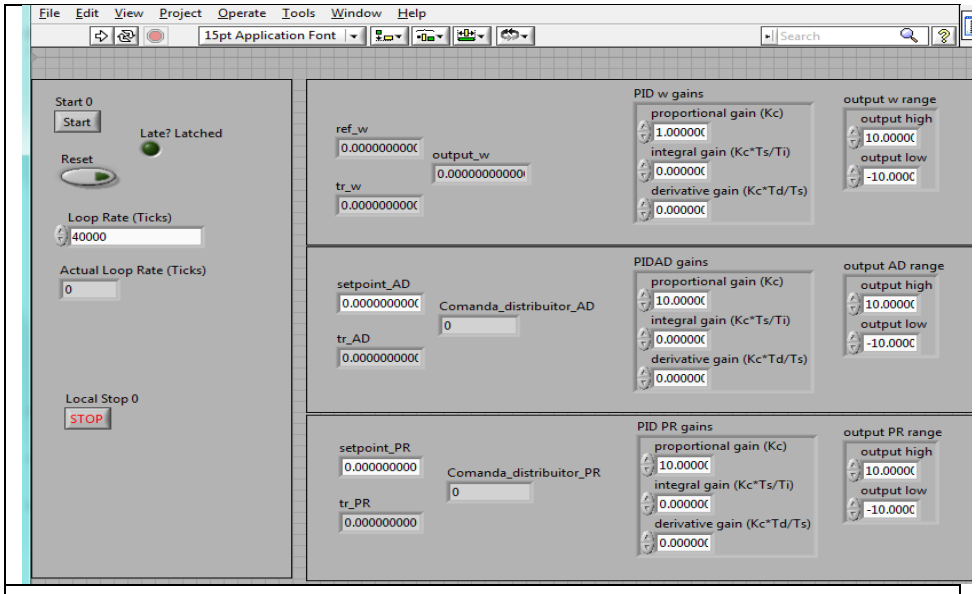

Fig. 6. FPGA software front panel

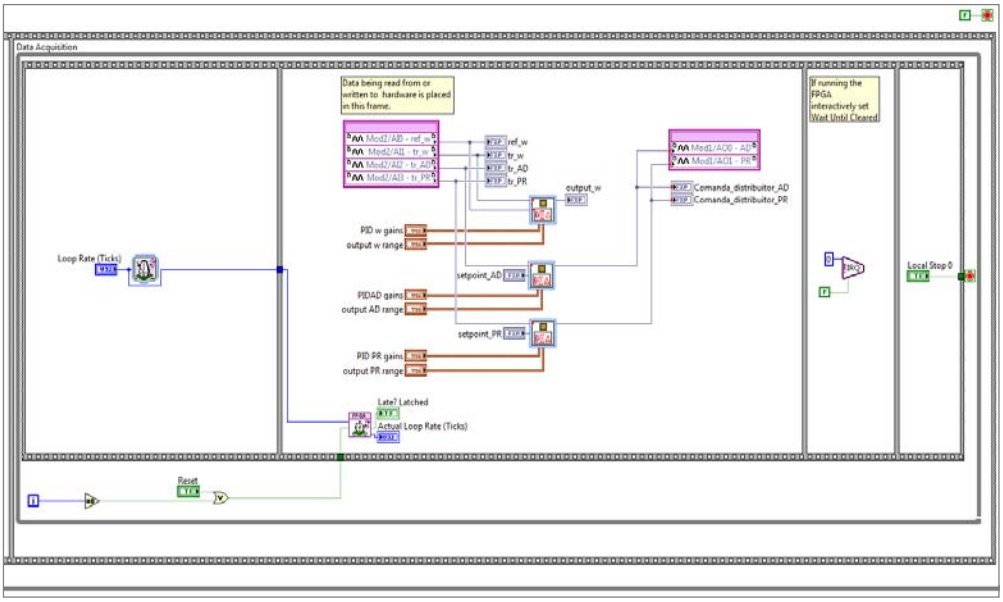

Fig. 7. FPGA software block diagram

Table 1

Data for optimal relation between the net turbine head,
the position of the rotor blades and the position of the wicket gate

H [m]	AD [%]	PR [%]
2,5	68…100	0-48
4	60…100	0…73
6	53…100	0…95
8	48…90	0…100

Knowing that the optimal relation between the position of the rotor blades and the position of the wicket gate is a function of head, the motion of the rotor blades servomechanism has been simulated based on the opening of the wicket gate servomechanism (fig. 8).

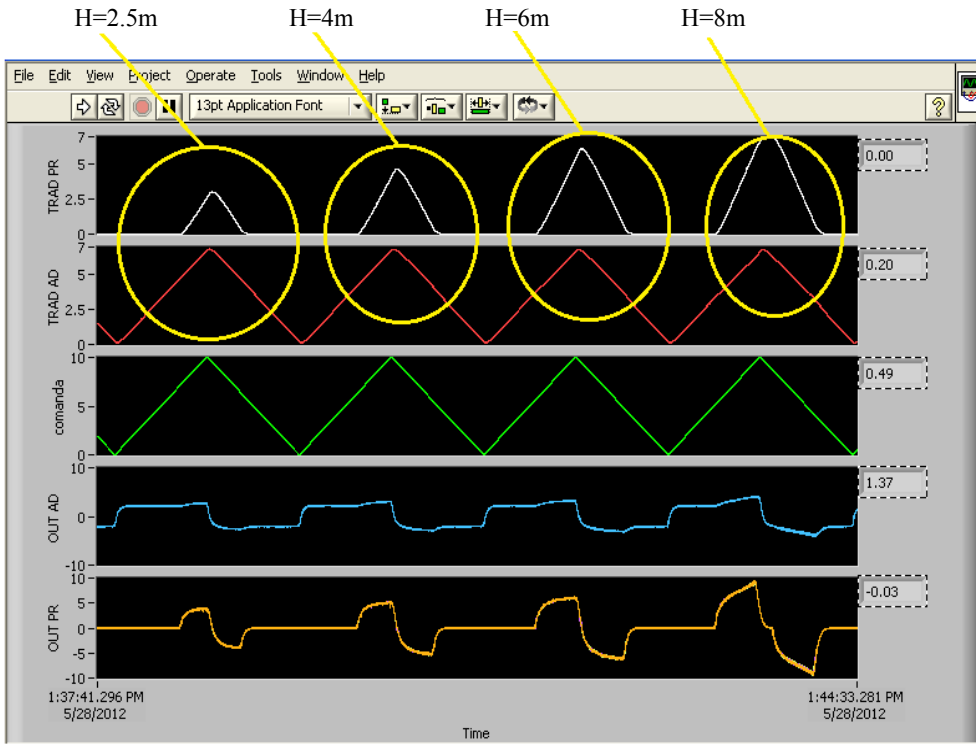

Fig. 8. Simulation results

4. Results of the experimental research

In order to test the behavior of the speed governor, the system presented in fig. 9 has been used. The generated input signal has been a square wave with 5V amplitude, corresponding to a 50 Hz reference frequency.

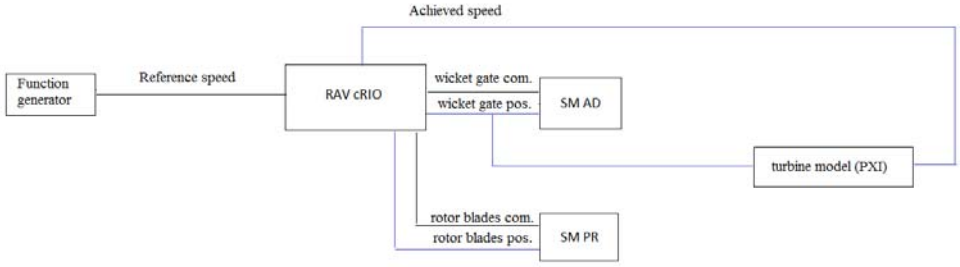

Fig. 9. Speed governor test system

The tuning of the speed governor controller has been done directly, by watching the process variables (reference speed and achieved speed). The system monitoring interface (fig. 10) shows a sequence of the testing procedure.

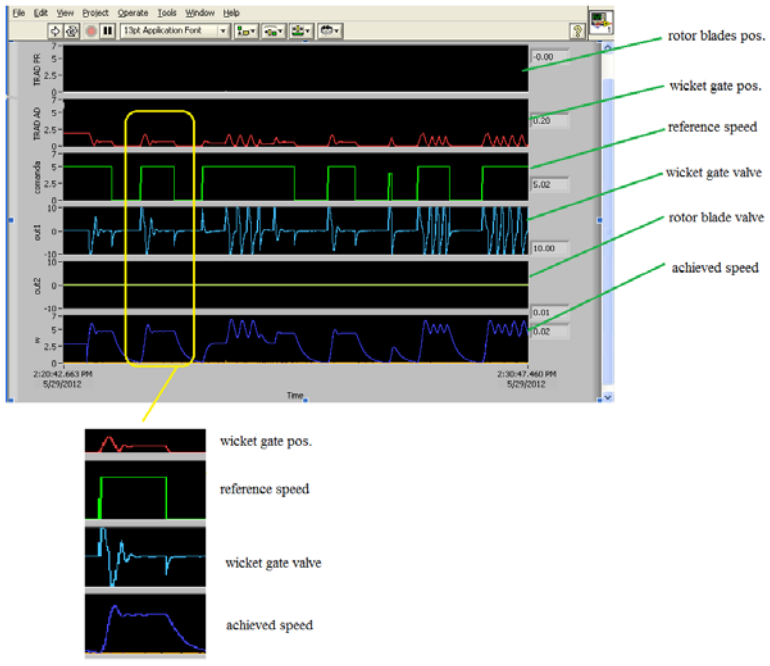

Fig. 10. System monitoring interface

The interface offers the possibility of tracking the effect of controller parameter changes in real time and visually comparing the results with previous iterations. This has allowed an easy identification of the optimal controller parameters.

After determining the optimal parameter values (Kp=10, Ki= 0.00781 for the speed governor PI controller), the authors have performed detailed experiments in order to assess the quality of the system's response during the startup sequence until the desired frequency (50 Hz) is achieved. Fig. 11 shows the evolution of the system from figure 12 with the following collors: green-reference speed, blue-acheved speed, red-wicket gate position, cyan-wicket gate valve command signal.

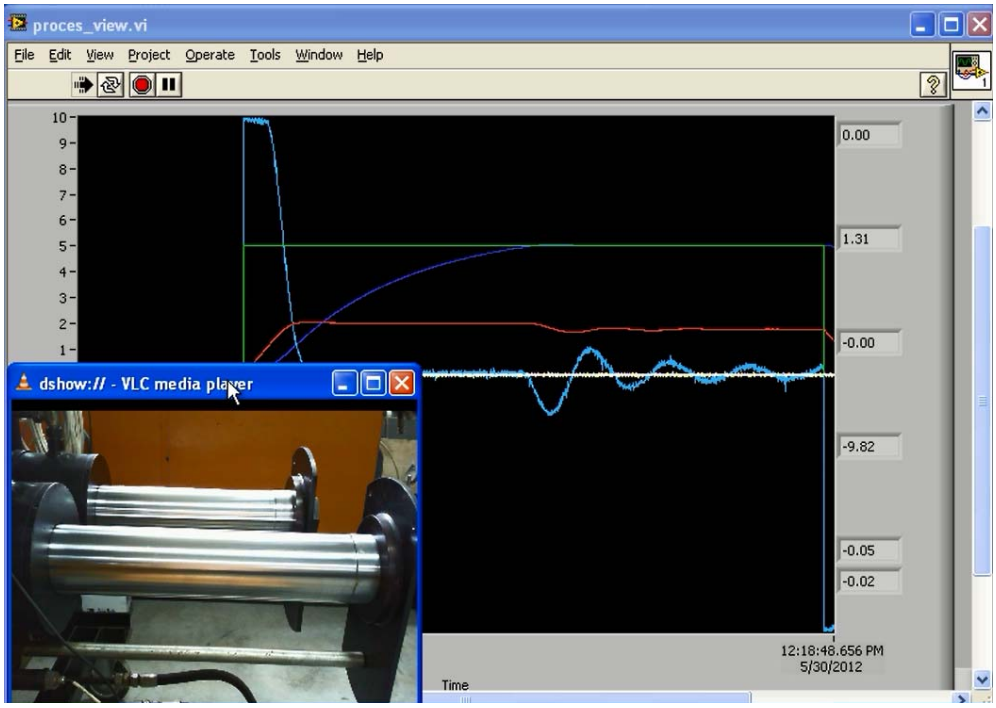

Fig. 11. System response and test bench servomechanisms

5. Conclusion

The application developed by the authors has allowed the validation of the new digital speed governor concept for Kaplan turbines. The use of a hybrid x86-FPGA system (like CompactRIO) allows significant improvements in terms of operating speed and reliability, while also offering a reduction in costs. As such, it

can be stated that FPGA based solutions represent the next generation of numerical systems for process control in the field of the hydropower units. At the same time, the overall price of the hardware and software system developed for a hydropower unit is lower than other equivalent solution.

Fig. 12. Functional speed governor model using NI cRIO technology

6. Acknowledgments

The authors are grateful for the help offered by LMS International BV from Belgium, and National Instruments Corporation from U.S.A. for their continuous support through academic programs. Trying to solve complex industrial problems by the aid of high level numerical simulation environments like AMESIM and LabVIEW, the authors received always facilities and fruitful advices from the above mentioned companies.

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