ADVANCED ELECTRO-THERMAL MODELING FOR SURFACE MOUNT RESISTORS

Cătălin NEGREA[1], Paul SVASTA[2]

Exceeding component maximum ratings due to transient events like current spikes can lead to premature failure of surface mount resistors due to thermal and electrical overstress. In order to accurately evaluate device parameters and their impact on the circuit behavior a coupled electro-thermal simulation method must be applied under the influence of packaging. This article presents an analysis method for electro-thermal transient interaction for resistors, based on thermal impedance modeling using RC network synthesis and SPICE circuit solver simulation. The described approach enables the simultaneous analysis of film temperature and resistance variations, presenting interest for applications in which the thermal behavior of fixed resistors can have important consequences on the functional parameters of the circuit.

Keywords: Electro-thermal simulation, thermal impedance, SMD resistor

1. Introduction

Due to their high count in electronic assemblies, fixed resistors and especially chip type resistors have an important influence on the overall reliability of a product. Transient events such as current spikes or lighting surges that are often neglected during design stages can have destructive effects. The ability to withstand such events is translated in to the pulse handling capability of the device, but often such data is not presented in the manufacturer datasheets [1]. Operating at high, but nondestructive, temperatures for extended periods of time leads to a permanent drift in the resistance value which can cause functional parameter change outside the specified limits. It is well known that all resistors types present some degree of change in resistance with the resistive element operating temperature. All the above mentioned temperature related effects are strongly dependent on the thermal environment of the device, which implies PCB (Printed Circuit Board) design, air flow, heat generated by other components, so in other words it is application specific. Evaluating transient electrical effects under the thermal influence of packaging is rarely considered due to the high number of variables involved in the modeling process. Previous studies

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concerning chip resistor thermal management present results only for steady state conditions [2, 3, 4] but as mentioned before, in many applications pulsed mode is highly important.

This paper presents a method of simulating electrical and thermal variables of linear fixed resistors in the time domain, using an ordinary SPICE circuit solver. The modeling technique is based on transient electro-thermal analogies, using finite element thermal simulations as a starting point for model definition. In [5] a similar approach was used for modeling electro-thermal interactions for LEDs with good agreement to experimental results.

This approach enables the application designer to simultaneously analyze resistive film temperature and electrical parameters, while also offering the benefits of SPICE simulations such as parameter sweep and worst case analysis.

2. Temperature effects on linear resistors

During normal operation passive components are subjected to temperature variations due to several factors: selfheating due to the Joule effect, heating of the printed circuit board (PCB) and surrounding air caused by other components and variations in ambient conditions.

Thermal behavior of resistors is dictated by the resistivity variation of the resistive film or foil. This variation is defined be the thermal coefficient of resistance (TCR) expressed as:

$$TCR(T) = \frac{1}{R(T)} \frac{dR(T)}{dT} \left[\frac{ppm}{^oC} \right] \tag{1}$$

Using TCR as a function of temperature eq. (1) becomes:

$$R(T) = R(T_{nom})[1 + TCR(\Delta T)] \left[\Omega\right] \tag{2}$$

where $R(T)$ is the resistance at temperature T, $R(T_{nom})$ is the reference resistance at the nominal temperature T_{nom} and $\Delta T = T - T_{nom}$ is the temperature difference.

As mentioned in [6] the TCR value specified in resistor datasheets is a linear approximation of the actual $R(T)$ curve, defined by the tangent lines of the cold and hot chords. The temperature range used for the cold and hot chords by the manufacturer to define the TCR value might be different from the actual temperature in the application. Also the trend of the TCR variation might be significantly different from one manufacturer to another for the same film type. This difference in behavior should be taken in to account especially when TCR tracking between two or more resistors is required in order to maintain a stable ratio of their values. The actual $R(T)$ curve's shape of NiCr alloys closely

matches a graph of a quadratic polynomial equation [6]. The presented modeling approach permits complex polynomial variation modeling up to a 5th degree function.

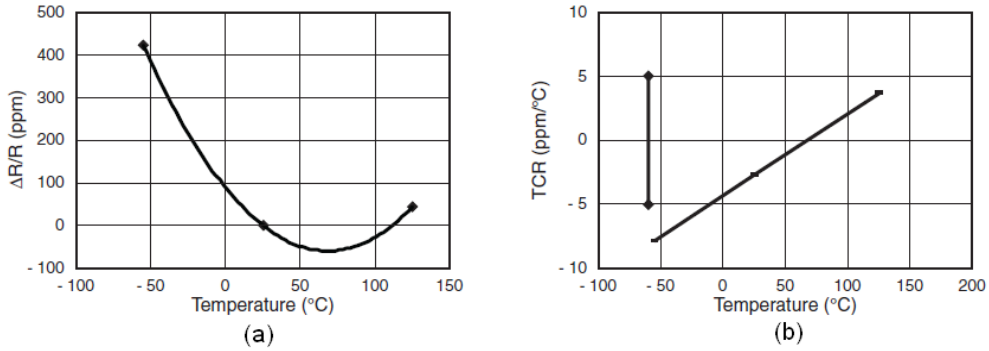

Fig. 1. Normalized resistance vs. temperature variation (a) and TCR variation for cold and hot chords (b) for NiCr thin film resistor from vendor 1 [6].

Modeling resistance variations for NTC (Negative Thermal Coefficient) and PTC (Positive Thermal Coefficient) thermistors also requires high order polynomial and exponential approximations, as shown in [7].

Fig.1 and 2 presents the normalized resistance variation for two NiCr thin film precision resistors provided by different manufacturers and their corresponding TCR linear approximations obtained for the cold and hot chords.

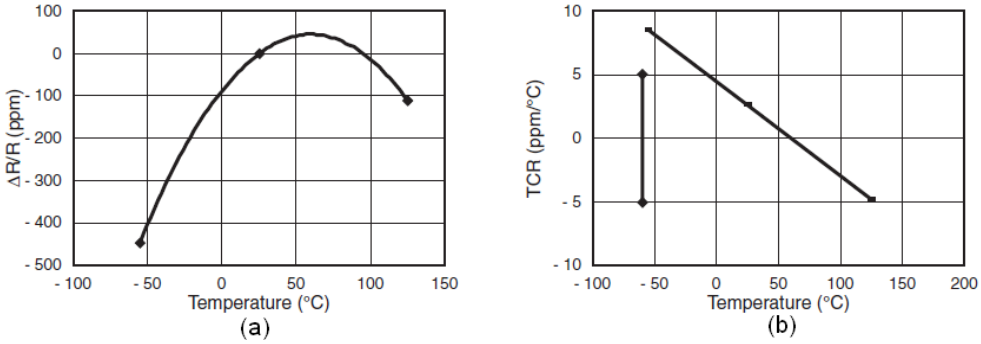

Fig. 2. Normalized resistance vs. temperature variation (a) and TCR variation for cold and hot chords (b) for NiCr thin film resistor from vendor 2 [6].

From the figures above it can be observed that by considering only the limit values of the TCR for modeling of temperature induced variations, as it is

commonly assumed, the errors can become highly significant for some temperature ranges due to the actual TCR nonlinearities.

3. Electro-thermal Modeling

Usually electrical circuit simulations are done considering all components at the same temperature, but in practice this is rarely the case. Modeling of the resistance variation by a first order approximation is commonly used in simulations but never correlated with the actual selfheating of the component.

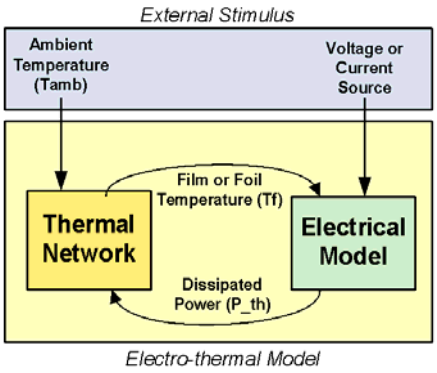

Fig. 3. Block interactions of the electro-thermal model

By considering the thermal effects on the actual 3D virtual model of the assembly, a more realistic modeling approach can be defined, and of course this will represent a significant improvement in the accuracy of the simulation results, as stated in [8].

Figure 3 presents the parameter basic interactions between electrical and thermal fields. The resistor dissipated power defined by Joule effect is used as an input for the thermal network. The result of the RC Cauer network circuit solving is the instantaneous film temperature which is then used to refresh the resistance and power values. Fig.4 illustrates the proposed electro-thermal model based on SPICE circuit element definition. Block 1 is the electrical part of the model composed of the temperature dependent resistor *R(TF)*, the parasitic equivalent series inductance *ESL* and the parasitic package capacitance *Cpar*. Since the film temperature is modeled as the potential *TF*, a voltage controlled current source is used to model the actual resistor because a voltage controlled resistor is not currently implemented in SPICE. The variation of the resistance with film temperature can be defined based on a polynomial function with the general form:

$$I(V_{12}, T_F) = (V_1 - V_2) / R(T_{nom}) \cdot \sum_{i=1}^{n} a_i T_F^{\ i} \tag{3}$$

,or by using the first order TCR as described by eq. 2. A voltage controlled voltage source is used to obtain the instantaneous dissipated power value based on

the expression depicted in the fig. 4. Block 2 of Fig.4 presents the structure of the RC network in Cauer form.

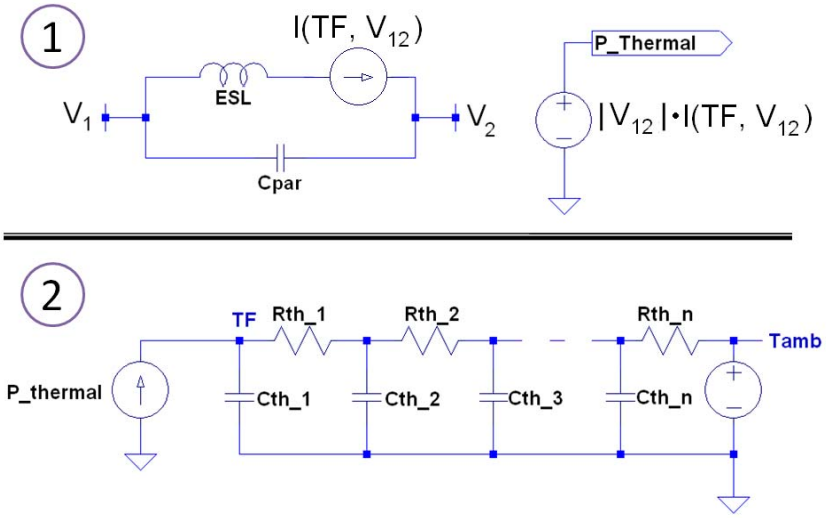

Fig. 4. Proposed electro-thermal model building blocks for SPICE solver.

4. Thermal Modeling

The method for dynamic electro-thermal modeling is to extract the transient thermal information from the thermal impedance response of the PCB assembly, including resistor package and board. FEM (Finite Element Method) software offers the possibility of transient thermal simulations based on detailed geometry and material properties of the resistor package and the assembly.

The thermal impedance curve is obtained by subtracting the ambient temperature T_{amb} from junction temperature T_j and dividing the obtained value by the instantaneous power P:

$$Zth(t) = (T_j(t) - T_{amb}(t)) / P(t) \tag{4}$$

For the case when *Zth* is obtained using FEM simulation the power and ambient temperature values are constant over time.

The representation of thermal behavior of a resistive film as an RC network is basically a form of model order reduction. As stated in [9], when boundary condition independence is not required and there is a single film-to-ambient heat-flow path, a Cauer type RC is a viable solution for junction temperature calculation. Modeling of resistive element transient thermal behavior in correlation with the electrical model, using RC networks, was successfully used

in [8] for thick film embedded resistors and shows good agreement with experimental measurements.

For identification of RC parameter values from the transient thermal response there are two methodologies mentioned in literature: (1) the NID (network identification by deconvolution) method, first introduced in [10] and extensively used [9, 11]; (2) curve-fitting to an exponential target equation which describes a Foster type network [12].

For the presented implementation a nonlinear least square curve-fitting technique to a Foster type network equation of *n*-th order is used:

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th,i}(1 - \exp(-t / R_{th,i}C_{th,i})) \tag{5}$$

Fig.5 illustrates the Foster network used as a thermal transient model. The dissipated power P_d is modeled as a current source and the ambient temperature T_{amb} is modeled as a voltage source.

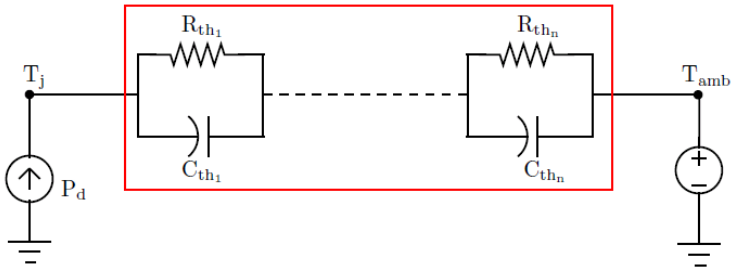

Fig 5. Foster type RC network.

The order of the target function must be defined by the user based on the required level of accuracy. In most practical cases the thermal impedance profiles can be modeled by 3rd to a maximum of 8th order networks with satisfactory results.

A Foster type model has no physical meaning and is also counterintuitive, so it is used only for the convenience of mathematical modeling [11]. By using the transformation method presented in [11] the RC parameters for a Cauer type network are obtained, with the topology presented in Fig.6.

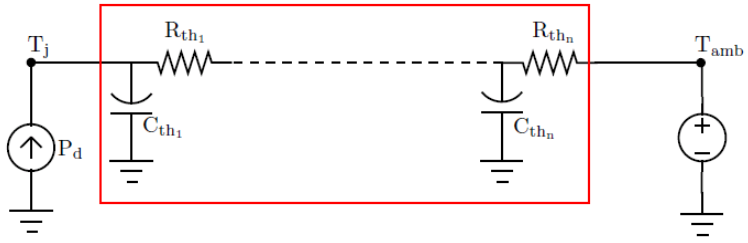

Fig 6. Cauer type RC network.

Briefly, the transformation method uses the identification of Cauer RC elements based on the recursive decomposition on the Laplace-transform Cauer function:

$$Z_{th\_Cauer\_n}(s) = sc_n + 1/(r_n + Z_{th\_Cauer\_n-1}(s)) \quad (6)$$

Equating the Foster impedance written as a rational function $Z_{th\_Foster\_n}(s) = p_n(s)/q_n(s)$ with the Cauer $Z_{th\_Cauer\_n}(s)$, the rational function $1/Z_{th\_Cauer\_n}(s) = q_n(s)/p_n(s)$ is decomposed by standard Euklid's algorithm into a polynomial linear rational function and a reminder, to the form:

$$1/Z_{th\_Cauer\_n}(s) = q_n(n)/p_n(n) = sc'_n + k_n + rem_n(s)/p_n(s) \quad (7)$$

By comparing this expression with eq. 6 the *n*-th order thermal capacitance Cth_n and thermal resistance Rth_n can be identified. The remainder will be further decomposed to obtain the *n-1* order elements. The algorithm is repeated until all Cauer elements are computed and is terminated when $p_0(s) = 0$ [11]. The indentified element values define a Cauer network with the same order as the Foster network, without any accuracy loss. The reverse transformation is also possible.

Fig.7 presents the model geometry for a 1206 package type resistor used to extract the thermal impedance profile. The board used is a standard 1s type 100x100 mm JEDEC board, with a dielectric thickness of 1.6mm and a copper thickness of 35 µm. The computational domain is assumed as 300x300x300 [mm] as mentioned in JEDEC 51-2 [13] standard for natural convection measurements. A transient simulation is carried out for a power step of 1W.

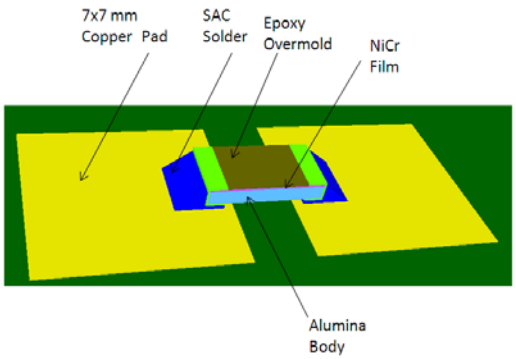

Fig. 7. Geometry of 3D model for 1206 film resistor used in CFD Simulation

Fig.8 presents the temperature distribution for the 1206 resistor mounted using 2x2 mm pads after 1.2 s from applying the power step.

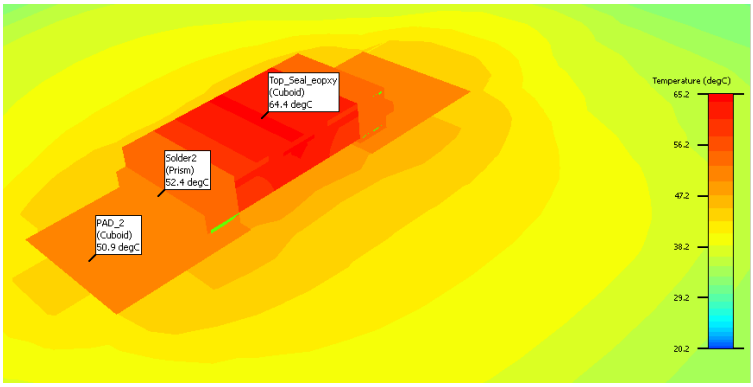

Fig. 8. Temperature distribution at resistor package and board level, on 2x2 mm solder pads, for 1[W] power dissipation, at 1.2s after startup

Steady state is reached after approximately 40s. The temperature map at this stage is presented in Fig.9. The steady state results for film-to-solder and film-to-ambient thermal resistances show good agreement with the measured values presented in [14]. Fig.10 presents the thermal impedance curve obtained using FEM simulation and the 6th order fitted function response. Using the Matlab tool, developed by the author the computing time was 4.31 seconds and the mean fitting error 0.155%. The Fig.also includes the RC element values in the rectangle.

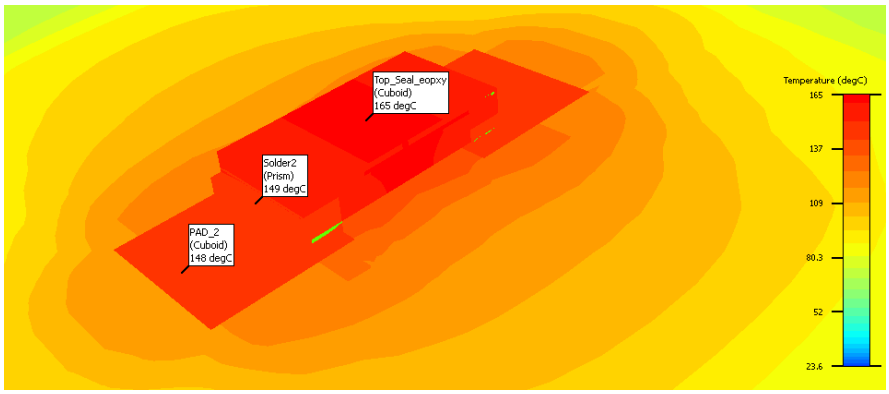

Fig. 9. Temperature distribution at resistor package and board level, on 2x2 mm solder pads, for 1[W] power dissipation, at 40 s after startup (steady-state)

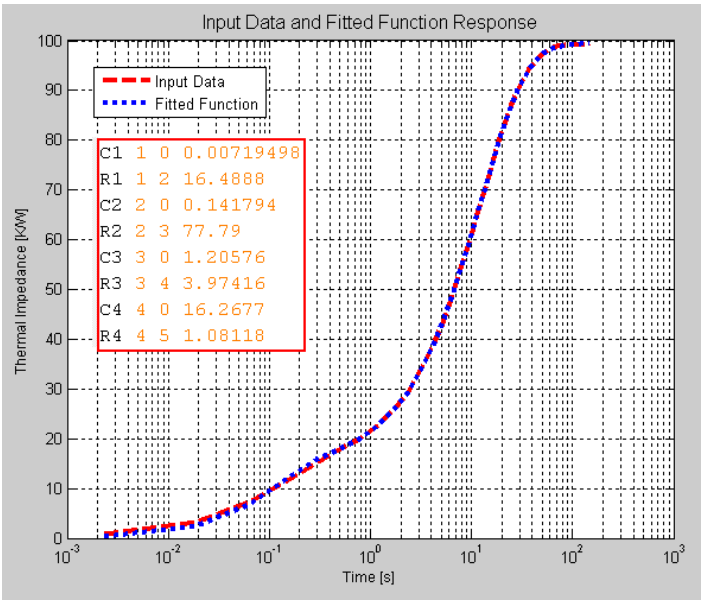

Fig 10. Comparison of the thermal impedance profile from simulation (red) and the fitted function response (blue); RC elements values of the Cauer network (and also connection nodes) are depicted in the red rectangle.

5. Matlab Tool for Model Development

In order to facilitate the code definition for the electro-thermal SPICE model a Matlab program was designed and implemented by the authors. The graphical user interface (GUI) of the program is presented in Fig.11.

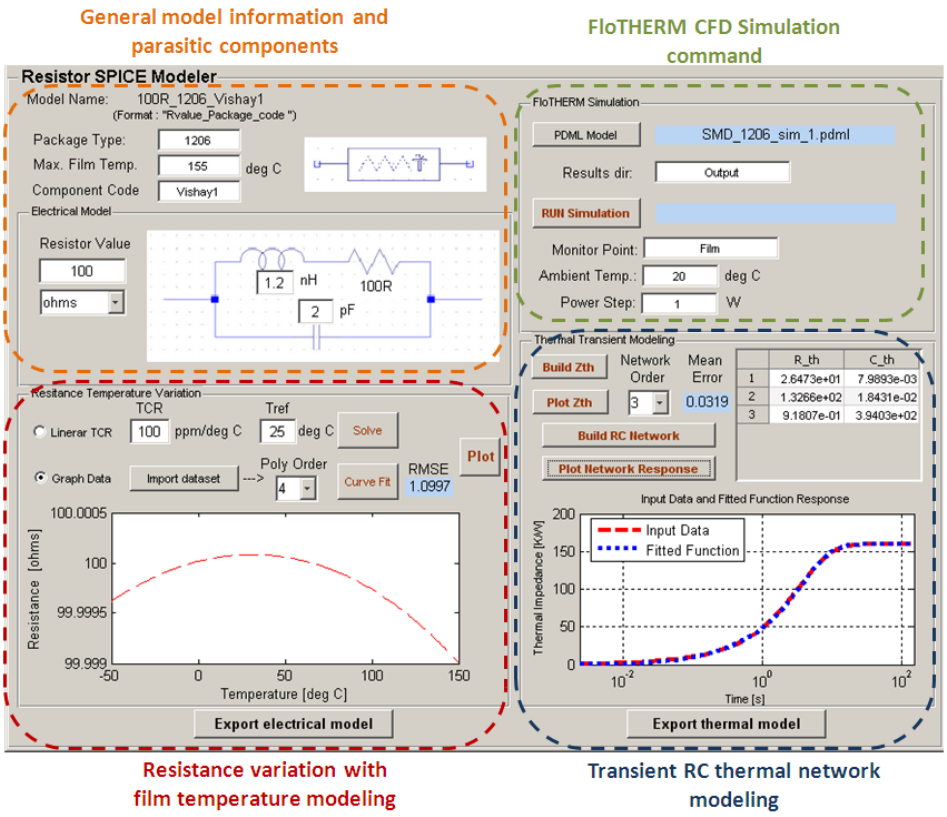

Fig. 11. Matlab Interface of the developed application for assisted electro-thermal SPICE model generation for resistors

The GUI has four main sections with specific functions:

- *General information and electrical model* – contains inputs for resistor value, ESL and Cpar parasitic elements, model name, package type;
- *Resistance Temperature Variation Modeling* - the resistance temperature variation is modeled based on a linear slope defined by a TCR value or by a dataset in Excel Spreadsheet format approximated using a polynomial function; the root mean square error is displayed as a figure.of merit for the approximation quality;
- *FloTHERM Simulation Command* - the FloTherm simulation is initialized based on a previously defined PDML file containing the detailed geometry and thermal simulation settings, using the command list described in [15];
- *RC Thermal Network Modeling* – used for building the thermal impedance curve based on data collected from the FloTherm simulation results; based on the thermal impedance curve the RC Cauer type network

is synthesized; the resulting RC element values and Cauer network response are displayed for investigation.

The result of the modeling procedure is the generation of the SPICE code lines separated in two distinct files. One file contains the electrical behavior including resistance variation with temperature and is modeling block 1 from Fig.4. The other file contains the RC Cauer network and the current source based on the model presented in block 2 from Fig.4. The language for code generation is based on SPICE 3 standard syntax [16].

6. SPICE Simulation

To analyze the functionality of the composed SPICE electro-thermal model a simple voltage divider circuit will be considered, with a high side resistor R1 of 91 Ω nominal value and a low side resistor R2 of 10 Ω nominal value. The simulation schematic built in LTSpice [17] is illustrated in Fig.12.

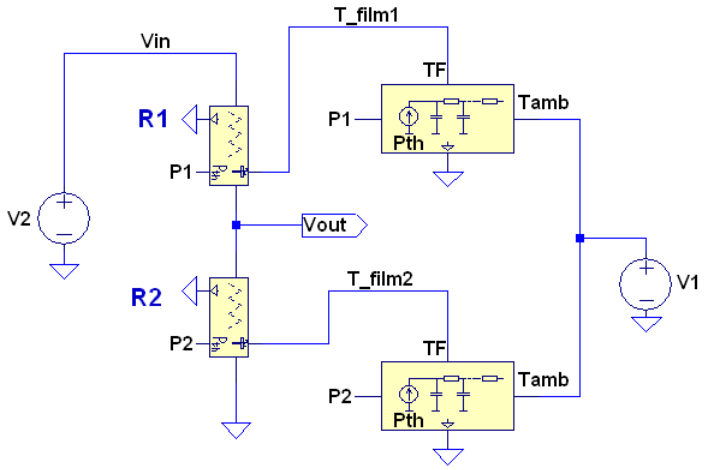

Fig. 12.Schematic of the resistor divider circuit used in electro-thermal simulation

Both resistors are in 1206 package but are from different vendors and mounted on different size solder pads. R1 resistance variation is modeled based on the graph from Fig.1 and is mounted on 5x5 mm pads. R2 resistance variation is modeled based on the graph from Fig.2 and is mounted on 2x2 mm pads. A 10V voltage step is applied by source V2 at t=10ms. V1 is used to set the ambient temperature for the Cauer networks at 20 ^{o}C. The resulting film temperature variations due to selfheating and the effect on the resistance value of R1 and R2 are presented in Fig.13.

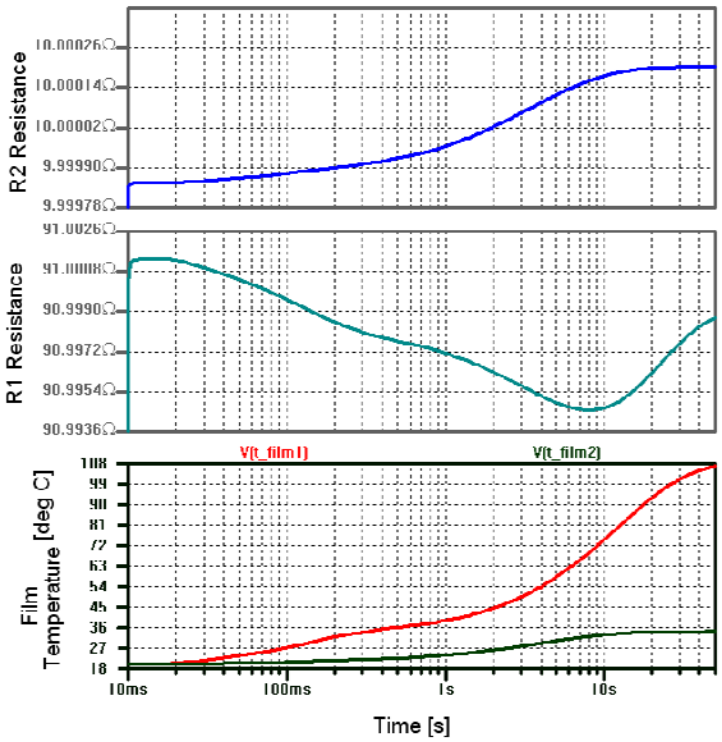

Fig. 13.R1 and R2 film temperature and resistance variations over time based on simulation scenario defined by the schematic in fig. 12

The different behavior of the two resistors with film temperature leads to a voltage ratio variation which could not have been accurately determined without the use of a fully coupled electro-thermal simulation approach. The resulting voltage ratio defined by the division of node voltages *Vout* to *Vin* as specified in the schematic from Fig.12 is presented in Fig.14.

The above simulation example proves that a correlated electro-thermal analysis can reveal functional parameter variations that are easily overlooked in typical electrical simulations but can have important consequences in precision applications. The results illustrated in Fig.14 present a voltage ratio deviation from -20.2 ppm to 70.8ppm. In most cases such small deviations are not important but for high precision applications, where functional parameters must have variations below ±5 ppm over a large ambient temperature range, such results indicate the need for thermal management redesign or selection of resistors with closely marched TCR variations .

The analysis presented in the above example can prove useful in applications that are highly sensitive to resistance variations such as precision voltage or current sources that use resistive the feedback networks, precision

amplifiers and active filters that use resistors for gain control, drivers circuits that use current sense resistors and measurement resistive bridges.

It should be stated that while this article is focused on thin film chip resistor modeling, the presented approach can successfully be used for any type of linear fixed resistor. It is also possible, with minor modifications to presented algorithm, to model electro-thermal behavior of NTC (Negative Temperature Coefficient) and PTC (Positive Temperature Coefficient) nonlinear resistors.

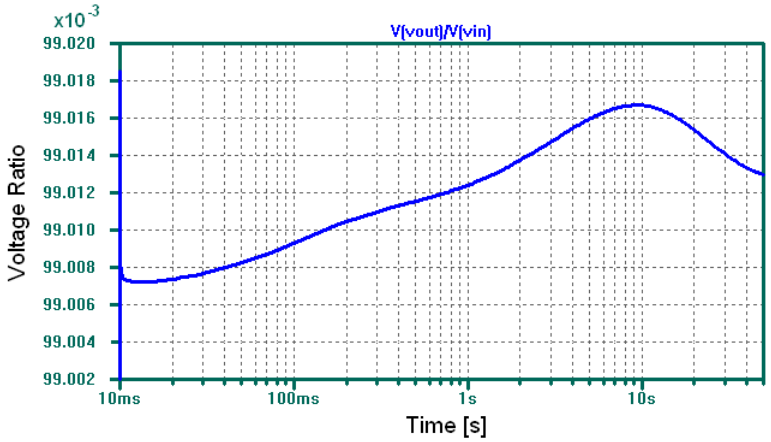

Fig. 14.Voltage ratio variation over time due to selfheating of the dividing resistors.

7. Conclusions

A modeling and simulation method for fully coupled electro-thermal behavior of chip resistors was described and illustrated for thin film 1206 chip resistors. The method uses time domain electro-thermal analogies to model the resistive film temperature variation based on detailed 3D CFD simulation results of the component, under the influence of packaging and thermal environment.

To facilitate the definition of the composed electro-thermal models, the authors developed a software application, using Matlab language, which includes all the necessary algorithms for SPICE code generation.

This method enables engineers to analyze the transient variations of functional parameters during selfheating. This approach also offers flexibility in terms of parameter observability, since practically any known parameter variation with film temperature and resistor current or voltage can be modeled using the techniques presented in sections 3.

The presented design approach describes a practical way of closing the loop between thermal an electrical simulations for applications where resistor parameters have important consequences on the circuit's performance.

R E F E R E N C E S

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