FPGA CONTROL FOR THREE-LEVEL STATIC POWER CONVERTERS

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Acest articol descrie o aplicție generică FPGA (Field Programmable Gate Array) pentru comanda convertoarelor de putere multinivel. Aplicația FPGA este configurată de către utilizator printr-un set de parametri. Strategia PWM specifică unui convertor poate fi implementată rapid de către utilizator cu ajutorul porților logice. Astfel, timpul dintre elaborarea strategiei PWM şi testarea sa experimentală este micşorat. Sunt prezentate rezultate experimentale pentru aplicația FPGA şi convertorul de putere 3L-ASNPC (Active Stacked Neutral Point Clamped).

This paper describes an FPGA (Field Programmable Gate Array) generic application for controlling multilevel power converters. The FPGA application is configured by the user with a set of parameters. The PWM strategy for a specific converter can be rapidly implemented by the user with the help of logic gates. In this way, the time between the PWM strategy elaboration and experimental testing is diminished. Experimental results are presented for the FPGA application and the 3L-ASNPC (Active Stacked Neutral Point Clamped) power converter.

Keywords: multilevel converters, FPGA control

1. Introduction

Modern applications need static power converters that are able to operate at high power rates. Multilevel topologies are providing solutions for over 30 years by series connecting power semiconductors [1]. These structures distribute only a fraction of the input voltage to the semiconductor devices, while improving the waveform quality at the output.

The first multilevel topology consisted in a serial connection of single-phase inverters with DC separate sources [2]. This structure was followed by the 3L-SC (Stacked Cells) conversion concept [3], [4]. The pioneering 3L-NPC (Neutral Point Clamped) converter (Fig. 1.a) was introduced in the early 1980s [5]. This is the most popular multilevel conversion structure in the industry. Later, another invention introduced the concept of the 3L-FC (Flying Capacitor) converter with flying capacitors [6].

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The 3L-NPC structure performances were improved by the 3L-ANPC (Active NPC) converter [7]-[9] and the 3L-SNPC (Stacked NPC) converter [10], [11]. The 3L-ANPC converter (Fig. 1.b) and the 3L-SNPC converter (Fig. 1.c) have more zero switching states than the 3L-NPC converter that are used to double the apparent switching frequency and to better balance the power losses of the switches. Recently, the 3L-ASNPC (Active SNPC) converter was proposed by [12]. The 3L-ASNPC converter (Fig. 1.d) has more degrees of freedom than the 3L-ANPC and the 3L-SNPC converters that are used to improve the static conversion.

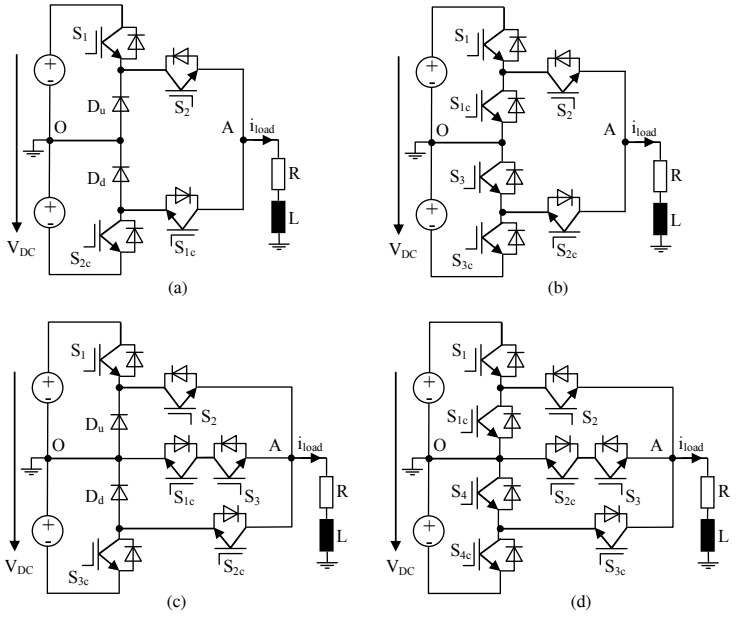


Fig. 1. Three-level power converters: (a) The 3L-NPC converter, (b) The 3L-ANPC converter, (c) The 3L-SNPC converter, (d) The 3L-ASNPC converter

Since their introduction in 1985, the FPGA (Field Programmable Gate Arrays) circuits are widely used for the digital control of power converters [13]-[18]. In these works, the FPGAs are chosen as the control solution for power converters because their advantages over their analog and digital counterparts: fast time-to-market, shorter design cycle, embedding processor, low power consumption and higher density for implementing digital control system.

Compared to the DSP (Digital Signal Processor) solution, the main advantage of the FPGA is that all the logic is executed continuously and simultaneously (concurrent operation) [18].

The FPGA circuits are designed to be configured or reconfigured by the user with a HDL (Hardware Description Language) programming language. Reconfiguring allows for incremental optimization and improvement of the control function by using software development techniques. This FPGA feature is interesting in terms of fast prototyping of PWM control.

In this paper, a generic FPGA control application for multilevel power inverters is described. The FPGA application allows the user to configure and test various PWM strategies for multilevel power converters. Experimental results for the 3L-ASNPC converter are obtained with the FPGA application.

2. Three-Level NPC Converter

The 3L-NPC converter (Fig. 1.a) is composed of two commutation cells (S_1-S_{1c} and S_2-S_{2c}) and two clamp diodes (D_u and D_d). The commutation cells are controlled by the α_1 and α_2 duty cycles (Fig. 2). The two commutation cells are switching half of the input voltage ($V_{DC}/2$) in only half period of the sinusoidal reference. All semiconductor devices are switching with the frequency (f_s) of the carrier signal. The α_1 and α_2 duty cycles are obtained with a CRPWM (Carrier Redistribution Pulse Width Modulation) control strategy (Fig. 3). The CRPWM strategy is based on the vertical distribution of two carrier signals. The α_1 duty cycle is obtained by comparing the upper carrier (Carrier1) with the reference on the positive period of the reference. The α_2 duty cycle is obtained by comparing the negative half period of the reference with the lower carrier (Carrier2).

The 3L-NPC topology has three commutation states: P, O and N (Table 1). The state P ($V_{DC}/2$) is obtained when the switches S_1 and S_2 are in conduction. The state N ($-V_{DC}/2$) is obtained when the lower branch (S_{1c} and S_{2c}) is in conduction. During the N and the P states, the two clamp diodes are blocked. The state O is obtained through one of the clamp diodes, depending on the inductive load current path. If the inductive load current is positive the upper branch is in conduction (S_2 and D_u). The lower branch (S_{1c} and D_d) is in conduction when the inductive load current is negative.

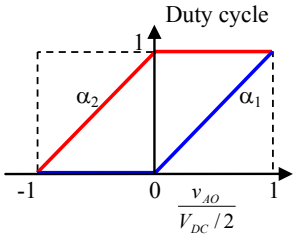


Fig. 2. The 3L-NPC duty cycles

Table 1

Switching sequences of the 3L-NPC converter

Output voltage (V_{AO})	Switching state	Switching sequence			
		S_1	S_{1c}	S_2	S_{2c}
$-V_{DC}/2$	N	0	1	0	1
0	O	0	1	1	0
$V_{DC}/2$	P	1	0	1	0

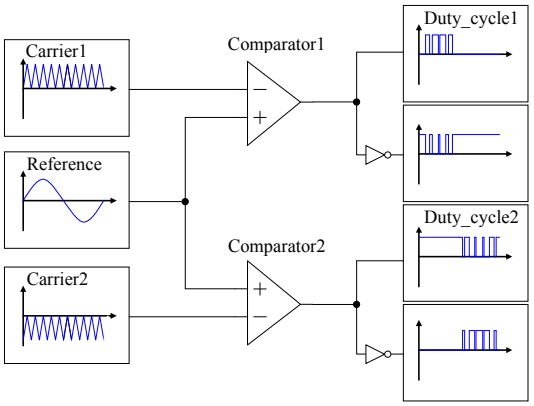


Fig. 3. CRPWM control strategy

3. Three-Level ANPC Converter

In addition to the 3L-NPC converter, the 3L-ANPC converter (Fig 1.b) has two active switches that are antiparallel connected to the clamp diodes. The converter is made up of six switches that form three basic commutation cells (S_1-S_{1c}, S_2-S_{2c} and S_3-S_{3c}). The three commutation cells are controlled by the α_1, α_2 and α_3 duty cycles (Fig. 4). The switches S_1 and S_{1c} are controlled only half a cycle by the α_1 duty cycle. Also, the α_3 duty cycle is applied to the S_3 and S_{3c} switches for half of commutation cycle. The S_2 and S_{2c} switches are controlled on the entire commutation cycle by the α_2 duty cycle.

The PWM strategy for the 3L-ANPC converter uses the PSCPWM (Phase-Shifted Carrier Pulse Width Modulation) principle. In the PSCPWM strategy, the Carrier2 signal is phase-shifted with half of switching period from the Carrier1 signal (Fig. 5).

The 3L-ANPC converter has six commutation sequences: P, N, O_1^-, O_2^-, O_3^+, O_4^+ (Table 2). The switching state P ($V_{DC}/2$) is obtained by turning on switches S_1, S_2 and S_3. The switching state N ($-V_{DC}/2$) is obtained when the switches S_{1c}, S_{2c} and S_{3c} are in conduction.

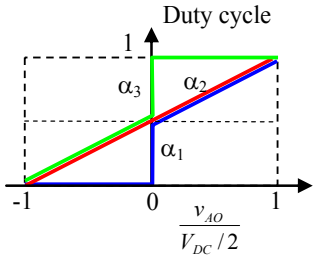


Fig. 4. The 3L-ANPC and 3L-SNPC duty cycles

Table 2

Switching sequences of the 3L-ANPC and 3L-SNPC converters

Output voltage (V_{AO})	Switching state	Switch sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	1	0	1	0	1
0	O_1^-	0	0	0	1	1	0
	O_2^-	0	1	1	0	0	1
	O_3^+	0	1	1	0	0	0
	O_4^+	1	0	0	1	1	0
$V_{DC}/2$	P	1	0	1	0	1	0

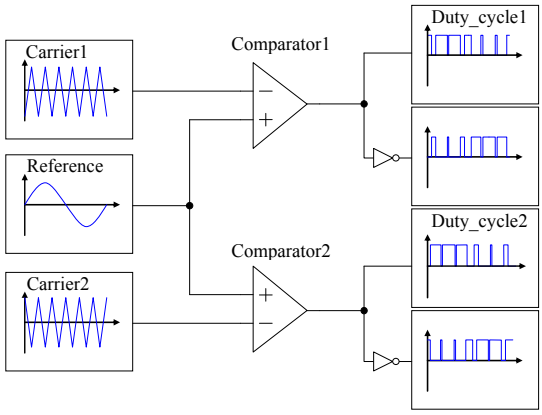


Fig. 5. PSCPWM control strategy

The states O_1^- and O_2^- are obtained when the reference voltage is negative, while the states O_3^+ and O_4^+ are obtained when the reference voltage is positive. The state O_1^- is obtained when the switches S_{2c} and S_3 are turned on. The state O_2^- is obtained when S_{1c}, S_2 and S_{3c} are turned on. The state O_3^+ is obtained when the switches S_{1c} and S_2 are turned on, while the state O_4^+ is obtained when the switches S_1, S_{2c} and S_3 are turned on.

4. Three-Level SNPC Converter

The 3L-SNPC converter (Fig. 1.c) is a combination between the 3L-SC and the 3L-NPC concepts. It is made up of six switches and two clamp diodes. The six switches form three basic commutation cells (S_1-S_{1c}, S_2-S_{2c} and S_3-S_{3c}) that are controlled by the same duty cycles as the 3L-ANPC converter (Fig. 4). The 3L-SNPC converter is controlled with a PSCPWM principle (Fig. 5).

The 3L-SNPC converter has the same switching states as the 3L-ANPC converter: P, N, O_1^-, O_2^-, O_3^+, O_4^+ (Table 2).

Compared to the 3L-ANPC topology, the 3L-SNPC converter has three available paths for the inductive load current. The converters topology is able to conduct the inductive load current on parallel paths with the help of the two clamp diodes. The upper current path (S_2 and D_u) and the lower current path (S_{2c} and D_d) are unidirectional. The middle current path composed of the S_{1c} and the S_3 active switches is bidirectional. If the inductive load current is positive, it is divided between the upper path and the middle path. For negative values of the induction current, the lower path and the middle path are in conduction. Because the inductive load current is divided between two paths, a part of the stress on the outer switches will be transferred to the middle switches.

5. Three-Level ASNPC Converter

The 3L-ASNPC converter (Fig. 1.d) is a derivative of the 3L-SNPC topology. It has two transistors connected antiparallel with the clamp diodes. The 3L-ASNPC topology contains eight switches disposed in four basic commutation cells (S_1-S_{1c}, S_2-S_{2c}, S_3-S_{3c}, S_4-S_{4c}). The four commutation cells are controlled by the α_1, α_2, α_3 and α_4 duty cycles (Fig. 6). The α_1 and α_2 duty cycles are applied to the S_1-S_{1c} and S_2-S_{2c} commutation cells when the voltage reference is positive. The S_3-S_{3c} and S_4-S_{4c} commutation cells are controlled by α_3 and α_4 duty cycles on the negative values of the reference voltage.

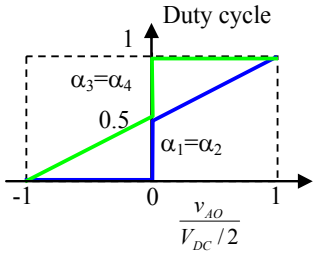


Fig. 6. The 3L-ASNPC duty cycles

Table 3

Switching sequences of the 3L-ASNPC converter

Output voltage (V_{AO})	Switching state	Switch sequence							
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}	S_4	S_{4c}
$-V_{DC}/2$	N	0	0	0	1	0	1	0	1
0	O_1^-	0	0	0	0	0	1	1	0
	O_2^-	0	0	0	1	1	0	0	1
	O_3^+	0	1	1	0	0	0	0	0
	O_4^+	0	1	0	1	1	0	0	0
$V_{DC}/2$	P	1	0	1	0	1	0	0	0

The control strategy for the 3L-ASNPC converter [12] is based on the PSCPWM principle (Fig. 5). In order to improve the static conversion, the 3L-ASNPC has more degrees of freedom than the 3L-ANPC and the 3L-SNPC converters. The converter has six switching states: P, N, O_1^-, O_2^-, O_3^+, O_4^+ (Table 3). The P switching state is obtained when the voltage reference is positive and the N switching state is obtained when the voltage reference is negative. The switching state P ($V_{DC}/2$) is obtained when the switches S_{2c}, S_{3c} and S_{4c} are on. The switches S_1, S_2 and S_3 are turned on in order to obtain the state N ($-V_{DC}/2$).

Like the 3L-ANPC and 3L-SNPC converters, the 3L-ASNPC converter has also four zero states. The states O_1^- and O_2^- are obtained when the voltage reference is negative. The state O_1^- is obtained by turning on the switches S_{3c} and S_4. The state O_2^- is obtained by turning on the switches S_{2c}, S_3 and S_{4c}. The O_3^+ and O_4^+ states are obtained when the voltage reference is positive. The state O_3^+ is obtained by turning on the switches S_{1c} and S_2. The state O_4^+ is obtained by turning on the switches S_{1c} and S_{2c} and S_3.

6. The FPGA application

The development of multilevel power static converter requires, beside computer simulation, experimental testing and validation. In the research and development phase of power converters, small and medium scale control functions are implemented in order to test different PWM commands.

This paper describes an FPGA application that can be configured in order to implement PWM strategies for various power converters topologies. The control function is realized for the Altera FPGA EP1K100QC208-1 circuit with the Altera Quartus development tool [19]. The Quartus II development software permits the use of a HDL programming language and/or the use of discrete circuits and logic gates.

Fig. 7 shows the block diagram of the FPGA control function. The control function is composed of four configurable logic blocks (Carrier, Reference, Comparator, DeadTime) coded in AHDL (Altera Hardware Description

Language) and one graphic block (User). The four configurable logic blocks have various parameters attached that can be tuned with the help of the Quartus II graphic interface. By configuring these logic blocks, the user easily obtains different carrier and sinusoidal signals for CRPWM or PSCPWM control type strategies. The User block (Fig. 7) is a graphic block reserved for implementing PWM strategies with the help of discrete circuits or logic gates.

The only input of the FPGA application is the onboard 16 MHz clock signal from the FPGA circuit. The 16 MHz clock signal is used to synchronize the internal computations of the logic blocks. The onboard clock signal is considered to be the only input of the logic function because all the other signals (carriers, reference, duty cycles, PWM control) are being computed by divers algorithms inside the logic blocks.

The Carrier logic block (Fig. 7) generates two carrier signals (Carrier1 and Carrier2). The user can configure the two carrier signals with the help of two parameters: PWM type and Frequency.

With the PWM type parameter, the user chooses between the CRPWM (Fig. 3) and the PSCPWM (Fig. 5) control strategies. The internal design of the Carrier logic block applies a vertical offset between the carriers for the CRPWM strategy. If the user chooses to implement a PSCPWM type strategy, the two carrier signals are being phase shifted with a half period by the internal logic of the Carrier block. The carriers are generated with an 8 bit up-down counter for the CRPWM strategy and with a 9 bit up-down counter in case of the PSCPWM strategy. The carrier amplitude is set to 255 in the case of the 8 bit up-down counter and it is set to 511 in case of the 9 bit up-down counter [16].

The carrier frequency is set with the Frequency parameter. The frequency of the carrier is generated from the 16MHz onboard clock signal by using frequency dividers.

The Reference logic block (Fig. 7) has as output a sinusoidal reference signal (S_r). The S_r has a DC component equal to 255. The amplitude of the S_r signal is computed from the Modulation index parameter. The user can choose the modulation index for his PWM control and the Reference logic block computes the amplitude of the sinusoidal signal according to the modulation index and the carrier amplitude. The positive reference signal (S_{rp}) is generated in order to have additional information about the reference. The S_{rp} signal is equal to 1 if the S_r signal is higher than the DC component. The S_{rp} signal is equal to 0 if the S_r signal is lower than the DC component.

The numeric values of the sinusoidal reference are stored in an internal FPGA ROM memory. This generates a fixed reference frequency and represents a limitation of a standalone FPGA application. A variable frequency for the sinusoidal reference can be obtained with a DSP/FPGA architecture. The DSP circuit can generate a variable sinusoidal signal in real time that can be an input to

the FPGA circuit. The development of a DSP/FPGA architecture is time consuming and expensive and it is not taken into account by this article.

The Comparator logic block (Fig. 7) has as output two duty cycles. The Duty_cycle1 signal is generated by comparing the S_r signal with the Carrier1 signal. Duty_cycle2 signal is obtained from the comparison of the S_r signal with the Carrier2 signal. The user can limit the maximum and minimum values for the duty cycle with the help of two parameters (Min Duty Cycle and Max Duty Cycle). The numeric duty cycle for a commutation cell is depicted in Fig. 8. The limitation of the duty cycle is used for protecting the IGBT switches.

In the User block (Fig. 7), the PWM strategy is defined with the help of logic gates. The duty cycle signal, generated in the Comparator logic block, is already the result of the comparison between a carrier signal and a reference signal. For classic PWM strategies, the duty cycle signal and its complementary signal can be applied directly to an IGBT commutation cell. For complex PWM strategies, the duty cycle from the Comparator block needs to be transformed in order to obtain PWM signals with different characteristics. This is done in the User block. In the User block, a wide range of PWM signal can be generated. The development of new PWM strategies is done in the User block in the same way as with a power simulation software, PSIM [20] for example.

The User block has as input the two duty cycles generated in the Comparator block and the S_{rp} signal. Fig. 9 shows as example the 3L-ASNPC PWM control for the S_1-S_{1c} commutation cell [12]. The c_x signal represents the PWM control for the S_x switch. Fig. 9.a shows the PWM control specified with the PSIM simulation software and Fig. 9.b shows the same PWM control defined in the User block.

The S_1 switch is controlled only on the positive half period of the reference. In order to implement this into the User block, a AND logic gate is used. The Duty_cycle1 signal is transferred through the AND logic gate to the c_1 signal if the S_{rp} signal is equal to 1. The control is correctly implemented because the S_{rp} signal is computed to be equal to 1 on the positive half period of the reference. On the negative half period of the reference, the S_1 switch is off. This is obtained with the same AND logic gate because on the negative half period of the reference the S_{rp} signal is equal to 0. In this case, the c_1 signal is equal to 0. The complementary c_{1c} signal is obtained by using an additional NOT logic gate.

The DeadTime logic block introduces a user defined dead time for the PWM signals in order to avoid the short circuit of the input voltage. The output of this block represents the PWM control for the switches.

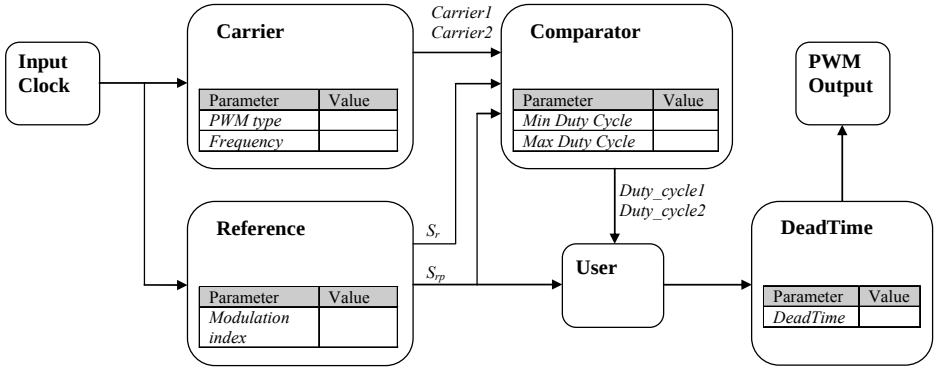


Fig. 7. The block diagram of the FPGA control function for multilevel power converters

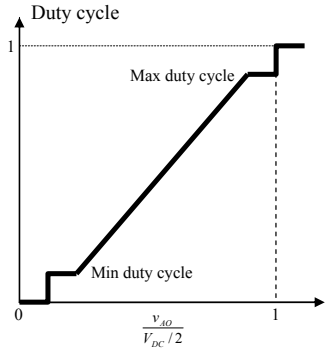
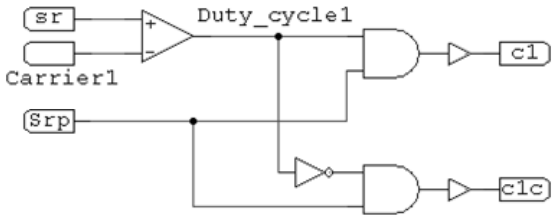
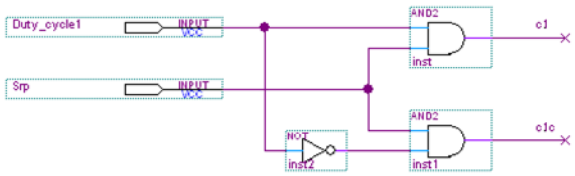


Fig. 8. The numeric duty cycle for a commutation cell



(a)



(b)

Fig. 9. The PWM strategy for the S_1-S_{1c} commutation cell of the 3L-ASNPC converter specified in: (a) PSIM software, (b) User block

Once the PWM strategy is defined, the user can verify the control signals with the help of simulation. The next step consists in downloading the PWM control function into the FPGA circuit for experimental validation. This approach leads to fast prototyping of PWM strategies and validation of new static power conversion topologies.The purpose of the described FPGA logic function is to create an easy to use environment for developing and testing new PWM strategies.

In this article, the proposed FPGA logic function controls a single phase inverter, but the application can be extended to the multiphase case. The Altera FPGA EP1K100QC208-1 internal resources in terms of ROM memory are enough for the multiphase control. The sinusoidal reference stored in the ROM memory for a single-phase converter occupies only 4% of the available ROM memory.

In order to generalize the application for a three phase inverter, three sinusoidal references, phase-shifted with 120^0 should by stored in the FPGAs ROM memory. The Comparator block in Fig.7 will have as input the two carrier signals and the three sinusoidal signals phase-shifted with 120^0 from the ROM memory. The logic for the Comparator block is the same for a multiphase case. The output of the Comparator block will consist in three sets of complementary duty cycles. The three sets of complementary duty cycles will be phase shifted with 120^0. The PWM control will be applied to the three converter phases by combining the duty cycles inside the User block.

7. Experimental results

A test bench has been made for the 3L-ASNPC converter. The input voltage V_{DC} is made of two serially connected sources (2x150V). An RL load has been connected to the output of the converter (R=29Ω, L=4mH). The control of the converter is realized with a standalone Altera FPGA EP1K100QC208-1 circuit.

Fig. 10 shows some experimental results for the 3L-ASNPC converter [12] controlled with the FPGA logic function. The FPGA logic function is configured for the PSCPWM strategy type, 4 KHz carrier frequency, 0.8 modulation index and 1.25μs dead time.

The PWM control strategy [12] implemented for the S_1-S_{1c} and S_2-S_{2c} switches of the 3L-ASNPC converter are presented in Fig. 10.a and in Fig. 10.b. Because the topology of the 3L-ASNPC converter is symmetric, the PWM control is similar for the S_3-S_{3c} and S_4-S_{4c} switches.

All the switches in the 3L-ASNPC topology are operating at the switching frequency only on a half cycle [12]. Thus, the average switching frequency on the

entire cycle is equal to half of the carrier frequency. For this application, the average switching frequency of the switches is equal to 2 KHz.

The output of the 3L-ASNPC converter is depicted in Fig. 10.c. The output voltage has three levels of voltage and the load current is sinusoidal.

The 3L-ASNPC converter doubles the apparent output frequency (Fig. 10.d). The carrier frequency is equal to 4 KHz and the first harmonic of the output voltage is found at 8 KHz.

Compared to other converters, the commutation and switching losses of the 3L-ASNPC converter are better balanced between the internal switches [20]. The unequal loss distribution among the semiconductor devices is a major drawback for static power converters because the most stressed semiconductor device in a topology will reach the maximum junction temperature. This has a direct consequence on the output power. Because the 3L-ASNPC converter obtains a better balancing of the switching and commutation losses, the maximum output power of the converter can be increased [21]. This makes the 3L-ASNPC converter an attractive solution for medium and high power applications.

8. Conclusion

The field of multilevel power converters presents a great interest to authors. In the last years, new converter structures were proposed as well as new PWM strategies to control them.

In this paper, an FPGA based control is described as a fast solution for developing and implementing multilevel PWM control. The application permits the implementation of CRPWM or PSCPWM multilevel PWM strategies. The carrier frequency, modulation index and the dead time are set by the user with the help of a graphic interface. The reference frequency is fixed in the case of a standalone FPGA application. The reference frequency can be variable in real time with a DSP/FPGA control architecture. This represents the premises for future work.

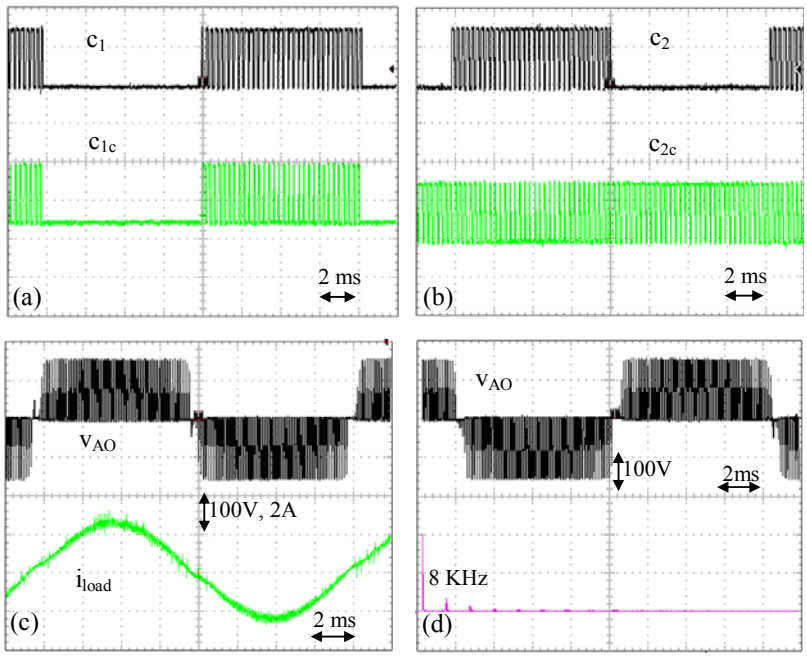


Fig. 10. Experimental results for the 3L-ASNPC converter (R=29 Ω, L=4mH, V_{DC}=300V): (a) PWM control for S_1-S_{1c} switches, (b) PWM control for S_2-S_{2c} switches, (c) output voltage v_{AO} and output load current i_{load}, (d) spectrum analysis of the output voltage v_{AO}

The FPGA application allows the user to implement the PWM control for the switches with the help of logic gates. The PWM control is constructed in a similar way as with a simulation tool. The FPGA standalone application represents a solution for fast prototyping of new PWM control strategies for multilevel static power converters.

Experimental results were presented for the 3L-ASNPC converter. The average switching frequency of the 3L-ASNPC converter is half of the carrier frequency, while the apparent output frequency is doubled.

REFERENCES

[1] *J. Rodriquez*, *J.-S. Lai*, *F.Z. Peng*, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", in IEEE Trans. on Ind. Electronics, **vol. 49**, 2002, pp.724-738.

[2] *R.H. Baker*, "Electric Power Converter", U.S.Patent 3 867 643, Feb.1975

[3] *P. Bhagwat*, *V.R. Stefanovic*, "Generalized structure of a multilevel PWM inverter," in IEEE Industry Applications Society Annual Meeting, 1980, pp.761-76

[4] *W.E. Brumsickle*, *D.M. Divan*, *T.A. Lipo*, "Reduced Switching Stress in High-Voltage IGBT Inverters via a Three-Level Structure", in Applied Power Electronics Conference and Exposition APEC'98, **vol. 2**, 1998, pp.544-550

[5] *A. Nabae*, *I. Takahashi*, *H. Akagi*, "A new neutral-point-clamped PWM inverter", in IEEE Trans.Industry Applications, **vol. IA-17**, 1981, pp.518-523.
[6] *T.A. Meynard*, *H. Foch*, "Multi-level Conversion: High Voltage Choppers and Voltage-Source-Inverters", in IEEE Power Electronics Specialist Conference, 1992, pp.397-403
[7] *T. Brückner*, *S. Bernet*, "Loss balancing in three-level voltage source inverters applying active NPC switches", in Proc. IEEE PESC, Vancouver 2001, pp.1135-1140.
[8] *T. Brückner*, *S. Bernet*, *H. Güldner*, "The Active NPC Converter and Its Loss-Balancing Control", in IEEE Trans.Ind.Electronics, **vol. 52**, 2005, pp.855-868
[9] *D. Floricau*, *E. Floricau*, *M. Dumitrescu,* „Natural Doubling of the Apparent Switching Frequency using Three-Level ANPC Converter", in International School on Nonsinusoidal Currents and Compensation – ISNCC, Łagów, Poland, 2008, pp.1-6
[10] *D. Floricau*, *G. Gateau*, *M. Dumitrescu*, *R. Teodorescu*, "A New Stacked NPC Converter: 3L-topology and control," 12th European Conference on Power Electronics and Applications – EPE 2007, Aalborg, Denmark, 2007, pp.1-10
[11] *D. Floricau*, *E. Floricau*, *G. Gateau*, "Three-level SNPC Commutation Cell: Features and Control", IEEE International Symposium on Industrial Electronics – ISIE, Cambridge, UK, 2008, pp.44-49
[12] *D. Floricau*, *G. Gateau*, *A. Leredde*, "New Active Stacked NPC Multilevel Converter: Operation and Features", IEEE Transactions On Industrial Electronics, no. 7, **vol. 57**, 2010, pp.2272-2278
[13] *S.B. Lecb*, "Putting Profit Into Power Electronic Products with Digital Control", in Proc. of the IEEE Applied Power Electronics Conference, Anaheim, Califomia, 2004
[14] *J. Bastos*, *L. Farronato*, *H. Figueroa*, "FPGA-Based Control of Power Converter: Comparing Alternative Solutions", in Twentieth Annual IEEE Applied Power Electronics Conference and Exposition - APEC, **vol. 3**, 2005, pp.1983-1989
[15] *S.-L. Jung*, *M.-Y. Chang*, *J.-Y. Jyang*, *L.-C. Yeh*, *Y.-Y. Tzou*, "Design and Implementation of an FPGA-Based Control IC for AC-Voltage Regulation", in IEEE Transactions on Power Electronics, no. 3, **vol. 14**, 1999, pp.522-532
[16] *L. Spătaru*, *D. Floricău*, *F. Ionescu*, "FPGA Control for the 3L-SNPC Power Converter", in Advanced Topics in Electrical Engineering, Bucharest, 2008, pp.103-106
[17] *B.J. Patella*, *A. Prodic´*, *A. Zirger*, *D. Maksimovic´*, "High-Frequency Digital PWM Controller IC for DC–DC Converters", in IEEE Transactions on Power Electronics, no. 1, **vol. 18**, 2003, pp.438-446
[18] *A. Castro*, *P. Zumel*, *O. García*, *T. Riesgo*, *J. Uceda*, "Concurrent and Simple Digital Controller of an AC/DC Converter With Power Factor Correction Based on an FPGA", in IEEE Transactions on Power Electronics, no. 1, **vol. 18**, 2003, pp.334-343
[19] Altera Home Page, www.altera.com
[20] Powersim Home Page, http://www.powersimtech.com
[21] *L. Spătaru*, *D. Floricău*, *F. Ionescu*, "Junction Temperature Distribution for Three-Level Static Power Converters", in Advanced Topics in Electrical Engineering, Bucharest, 2011, pp.321-326.