INVESTIGATION OF USING TAPERED COPLANAR WAVEGUIDE IN RF MEMS PHASE SHIFTER

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This paper presents the analysis and design of coplanar waveguide (CPW) in distributed MEMS phase shifters for communication systems. The phase shift can be obtained by changing MEMS Bridge capacitors located periodically over the transmission line. Simulation results of phase shifters with various structural parameters of CPW are analyzed to develop the optimized designs. The various structures of CPW are analyzed using quasi-TEM conformal mapping technique. The phase shifters are designed on the high-resistivity silicon substrate, using suspended AuSi bridge membrane. The simulated results demonstrate a phase shift of 286 at 36 GHz with the actuation voltage of 25 V, and a return loss better than 10 dB over 0–40 GHz band. It shows that the use of tapered CPW in phase shifter design produces more phase shift per unit length compared with conventional CPW phase shifter.

Keywords: microelectromechanical systems (MEMS), phase shifter, structural parameters

1. Introduction

Phase shifters have wide application areas, such as phased-array radars, satellite communication systems and measurement instrumentations. Most of the microelectromechanical systems (MEMS) phase shifters developed are based on low-loss MEMS switches developed in the past few years. MEMS switch replaced p-i-n diode or FET switch of conventional loaded-line phase shifters, which reduces the insertion loss of phase shifters at high frequencies.In existing methods, MEMS phase shifters satisfy stringent requirements concerning geometrical characteristics such as small size, light weight and manufacturing constraints like low cost, adaptability to integration. There are a number of topologies for these configurations, such as reflection-line [1], switched line [2], and loaded-line, etc. In comparison with other types, the distributed phase shifters can offer very wideband performance and work well at high frequencies. In general, this device consists of a coplanar waveguide (CPW) line that is periodically loaded with MEMS bridges, as shown in Fig. 1.

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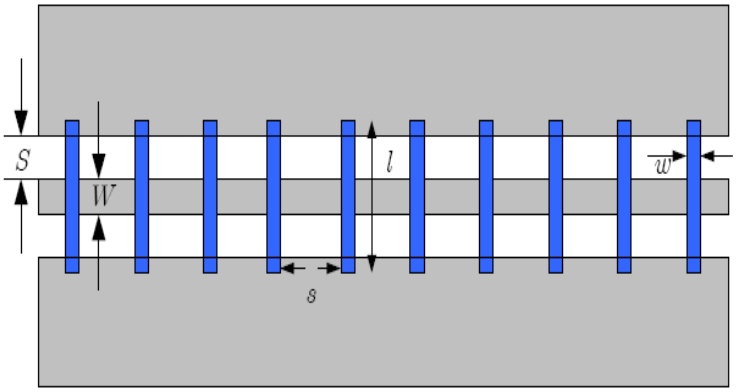

Fig. 1. Schematic layout of the MEMS distributed phase shifter

Barker *et al.* [3] proposed and studied the first MEMS distributed phase shifter. Further improvements in this phase shifter were presented in [4]–[7]. A one-bit low-loss phase shifter was achieved with 154°/dB at 25GHz and 160°/dB at 35 GHz [4]. In Lakshminarayanan *et al.* [7], here a phase shifter was approximately 240°/dB at 35 GHz with the return loss better than 10 dB from 10 to 35 GHz. Then, a multibit phase shifter can be easily fabricated by cascading the several one-bit phase shifters [8], [9]. Prior studies have dealt with the structure design of the phase shifters. However, the dependence of mechanical and electrical properties on various structural parameters is still an active area of research. Furthermore, for any device to be used in a practical application it must be reliable, and published reports of their reliability are scarce.

Our work focuses on developing the optimized designs of structural parameters and investigating the MEMS phase shifters. A MEMS phase shifter on high-resistivity silicon substrate has been designed, analyzed and simulated in this paper. In this case, tapered CPW with Si is chosen as the material to provide an outstanding phase shift compared to conventional CPW. Finally, an extensive study and simulated results for various structural parameters are presented.

2. CPW Analysis

The CPWs were designed to verify the models, material properties, and analysis procedures that will be used to design waveguide inputs and interfaces with the actual RF MEMS switches. Therefore, these waveguides were modeled in high-frequency electromagnetic. The high impedance CPW transmission line and its equivalent circuit is shown in Fig. 2(a) and 2(b).

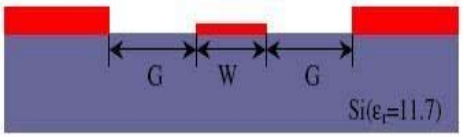

Fig. 2. (*a*) Layout of the CPW

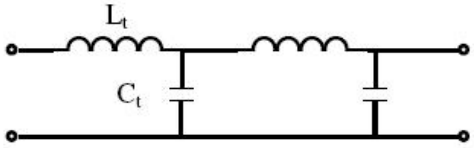

Fig. 2. (b) Equivalent Circuit of the CPW

The Veyres – Fouad Hanna approximation [10] is used in our case, in which the line capacitance of the CPW shown in Fig. 2. (a) can be written as the sum of two line capacitances, i.e.

$$C_{CPW} = C_0 + C_1 \tag{1}$$

C_0 is the line capacitance of the CPW in the absence of all dielectrics as shown in Fig. 3. and this boundary problem can be solved using conformal mapping [10], which gives

$$C_0 = 4\varepsilon_0 \frac{K'(k)}{K(k)} \tag{2}$$

where K is the complete elliptical integral of the first kind, and K'(k) = K(k'). The variables k and k' are given as

$$k = \frac{x_c}{x_b}\sqrt{\frac{x_b^2 - x_a^2}{x_c^2 - x_a^2}} \tag{3}$$

$$k' = \sqrt{1 - k^2} \tag{4}$$

The configuration of C_1 is shown in Fig. 4. , in which the electrical field exists only in a dielectric layer with thickness of h_1 and relative dielectric constant of ε_{r1}-1. Using conformal mapping [10],

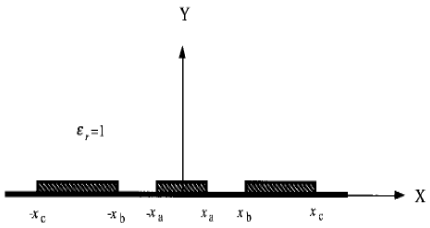

Fig. 2. Capacitance C_0 Configuration

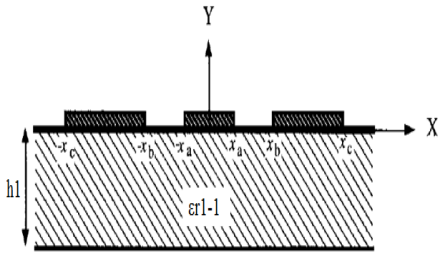

Fig. 3. Capacitance C_1 Configuration

$$C_1 = 2\varepsilon_0(\varepsilon_{r1} - 1)\frac{K'(k_1)}{K(k_1)} \tag{5}$$

where

$$k_1 = \frac{\sinh(\frac{\pi x_c}{2h_1})}{\sinh(\frac{\pi x_b}{2h_1})}\sqrt{\frac{\sinh^2(\frac{\pi x_b}{2h_1}) - \sinh^2(\frac{\pi x_a}{2h_1})}{\sinh^2(\frac{\pi x_c}{2h_1}) - \sinh^2(\frac{\pi x_a}{2h_1})}} \tag{6}$$

$$k_1^{'} = \sqrt{1 - k_1^2} \tag{7}$$

The effective dielectric constant ε_{eff}, phase velocity ν_{ph}, and characteristic impedance Z_0, of a transmission line are given as [11]

$$\varepsilon_{eff} = \frac{C_{CPW}}{C_0} \tag{8}$$

$$\nu_{ph} = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{9}$$

$$Z_0 = \frac{1}{C_{CPW}\nu_{ph}} \tag{10}$$

where c is the speed of light in free space, C_{CPW} is the line capacitance of the transmission line, and C_0 is the line capacitance of the transmission line when no dielectrics exist. To obtain the quasi-static wave parameters of a transmission line, we only have to find the capacitances C_{CPW} and C_0.

The complete elliptical integrals of the first kind using the approximations given by Hilberg [10] is given as

$$\frac{K(k)}{K^{'}(k)} \approx \frac{2}{\pi}\ln(2\sqrt{\frac{1+k}{1-k}}) \quad \text{for} \quad 1 \le \frac{K}{K^{'}} \le \infty \quad \text{and} \quad \frac{1}{\sqrt{2}} \le k \le 1 \tag{11}$$

$$\frac{K(k)}{K^{'}(k)} \approx \frac{\pi}{2\ln(2\sqrt{\frac{1+k^{'}}{1-k^{'}}})} \quad \text{for} \quad 0 \le \frac{K}{K^{'}} \le 1 \quad \text{and} \quad 0 \le k \le \frac{1}{\sqrt{2}} \tag{12}$$

3. Phase Shifter Design

The circuit design proposed here is based on a CPW transmission line whose phase velocity can be varied by using a single analog control voltage that varies the height of the MEMS loading capacitors, and the distributed capacitive loading on the transmission line and its propagation characteristics, as shown in Fig. 4. This results in analog control of the phase velocity and, therefore a true time delay phase shifter. The design requires a small value of loading capacitance per unit length, which results in very high actuation voltage. The topology of the CPW transmission line presented here, that varies the impedance, helps to increase the phase shift per unit length, resulting in a reduced physical line length, reduced pull down voltage and high capacitance ratio. The impedance and propagation velocity of the slow-wave transmission line are determined by the size of the MEMS bridges and their periodic spacing. The equivalent circuit of the loaded distributed MEMS transmission line is shown in Fig. 5. The shunt capacitance associated with the MEMS bridges is in parallel with the distributed capacitance of the transmission line, shown in Fig. 5.

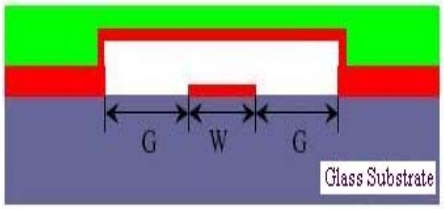

Fig. 4. Layout of the CPW with MEMS switch

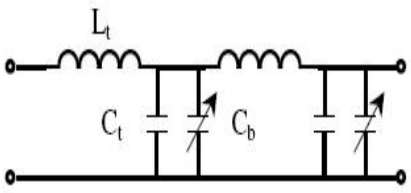

Fig. 5. Equivalent Circuit of the CPW with MEMS switch

The control voltage and operational frequency range play an important role in determining the performance of a distributed MEMS phase shifter, so the design of the actuation voltage and Bragg frequency is of crucial importance.

The per unit-length capacitance and inductance of the unloaded CPW line, are given by [3]

$$C_t = \frac{\sqrt{\varepsilon_{eff}}}{cZ_0} \quad \text{and} \quad L_t = C_t Z_0^{\,2} \tag{13}$$

where ε_{eff} is the effective dielectric constant of the unloaded CPW transmission line, Z_0 is the characteristics impedance of the unloaded CPW line, and c is the free space velocity. The MEMS bridge only loads the transmission line with a parallel capacitance C_b, the loaded line impedance Z_1 and phase velocity V_1 of the loaded line, become

$$Z_l = \sqrt{\frac{L_t}{C_t + \frac{C_b}{s}}} \quad \text{and} \quad V_l = \frac{1}{\sqrt{L_t\left(C_t + \frac{C_b}{s}\right)}} \tag{14}$$

where s is the periodic spacing of the MEMS bridges and C_b/s is the distributed MEMS capacitance on the loaded CPW line. Thus, the loaded line can be designed for Z_l=50Ω by choosing an unloaded line impedance Z_o>50Ω and the periodic spacing of MEMS bridge capacitance C_b. A result of creating a periodic structure is the existence of a cut-off frequency or Bragg frequency, f_{bragg}, near the point where the guided wavelength approaches the periodic spacing of the discrete components. In many of the distributed circuits, this cutoff frequency can be designed such that it will not limit the device performance since the discrete components will have a comparable maximum frequency. In the case of the distributed MEMS transmission lines used in this work, the self-resonant frequency of the MEMS bridges is not approached and thus the operation is limited by the Bragg frequency of the line. The periodic structure has an upper frequency limit due to the Bragg reflection occurring at [3].

$$f_{Bragg} = \frac{1}{\pi s\sqrt{L_t(C_t + C_b/s)}} \tag{15}$$

The force on the MEMS bridge due to an applied bias on the CPW center conductor is given by

$$F = \frac{\varepsilon_0 W w}{2g^2} V_{bias}^2 \quad \text{N} \tag{16}$$

where ε_0 is the free-space permittivity, W is the center conductor width, w is the width of the MEMS bridge, g is the height of the bridge, and V_{bias} is the applied bias voltage. The spring constant of the bridge is approximated by [3]

$$k = \frac{32Et^3 w}{L^3} + \frac{8\sigma(1-\nu)tw}{L} \quad \text{N/m} \tag{17}$$

where E is the Young's modulus of the bridge material, t is the bridge thickness, L=(W+2G) is the bridge length, σ is the internal residual stress of the bridge and ν is the Poisson's ratio.

The pull-down voltage of the MEMS bridge can be found by setting up a force–balance equation between the electrostatic force and the restoring force of the bridge. It is found that the MEMS bridge becomes unstable at $2g_0/3$, where g_0

is the zero-bias bridge height. The voltage at which this instability occurs is the "pull-down" voltage and is given by

$$V_p = \sqrt{\frac{8k}{27Ww} g_0^3} \quad V \tag{18}$$

The relative phase between the two states or the net phase shift ($\Delta\varphi$) is found from the change in the phase constant given by

$$\Delta\phi = \frac{\omega Z_0 \sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \tag{19}$$

The design consists of a 7.94mm long coplanar waveguide (CPW) transmission line whose centre conductor width (W) is 80μm and the gap is 45μm is fabricated on a 425μm silicon substrate with a dielectric constant of 11.7 and tan(δ)=0.008 and with 11 fixed-fixed beam MEMS bridge capacitors placed periodically over the transmission line, creating a slow-wave structure, shown in Fig. 6. The height of the bridge above the centre conductor is 3μm. The effective dielectric constant (ϵ_{eff}) of the unloaded CPW line has an average value of 6.25 and is linearly invariant with frequency. The width and span of the MEMS bridges are 40μm and 340μm, respectively. The same parameters are used for designing MEMS phase shifter using tapered coplanar waveguide. By applying analog voltage, the MEMS switch is actuated from UP state to the DOWN state, which induces an increase in loading capacitance. The effect is an increase in total capacitance per unit length of the transmission line, and hence a change in phase velocity and characteristic impedance. The change in phase velocity produces a phase shift that is determined by the capacitance ratio C_{up}/C_{down} of the MEMS switch. The line has characteristic impedance of $Z_0 = 50\Omega$. If the bias voltage is applied directly between the membrane and the center conductor with a control circuit, the pull down voltage V_p can be reduced.

A section of two linear taper designs between two MEMS switches with spacing of 750μm with varying impedances is shown in Fig. 7. Table. 1. shows the CPW width, gap and its impedance of the linear tapers used in the design. The characteristic impedances are calculated using quasi-TEM conformal mapping technique. The characteristic impedance of linear taper varies from 48Ω to 78Ω.

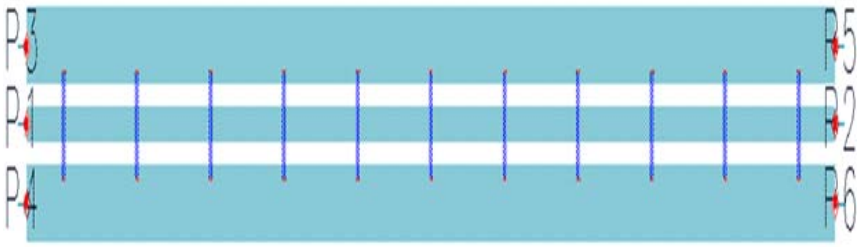

Fig.6. Layout of CPW loaded with 11 MEMS bridges.

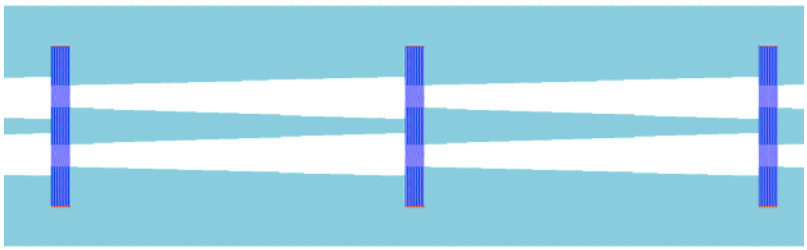

Fig.7(a). Layout of Linear CPW Design-I between with 3MEMS bridges.

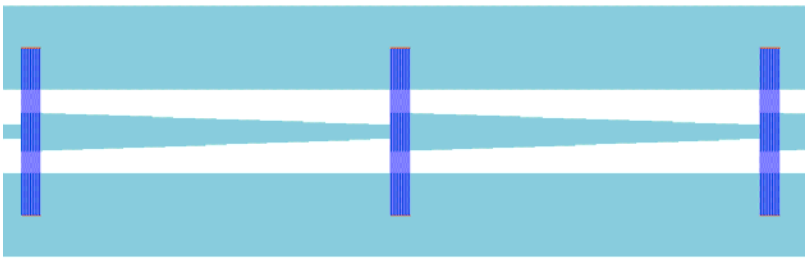

Fig.7(b). Layout of Linear CPW Design-II between with 3MEMS bridges.

Table. 1

Calculated Characteristic Impedance for various widths and gaps

Design – I			**Design – II**		
Width(μm)	**Gap (μm)**	**Z_0 (Ω)**	**Width(μm)**	**Gap (μm)**	**Z_0 (Ω)**
80	45	48.3	80	45	48.3
69	54	53.4	71	50	51.7
60	63	58.2	59	57	56.7
49	72	64.2	49	61	61.1
40	81	70.4	39	66	66.7
30	89	78.1	30	70	73.0

4. Results

The simulated results are shown in Fig. 8-10. The insertion loss of the phase shifter is -0.5dB to -1.5dB at 20GHz and the phase shifter- Design II insertion loss is a little larger compared with the other two designs as its delay line is the longest. Both the output and input return loss is less in the range 5-10dB. The change in phase shift is more in Design-I compared with conventional CPW and taper CPW design-II for the same length. Table. 2. consolidates the results obtained for the various CPW phase shifter designs. From Table. 2., the phase shift per unit length is more in taper Design-I compared with the other designs.

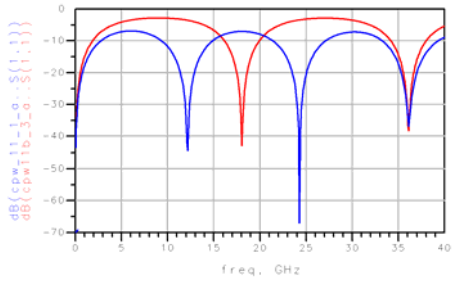

Fig.8(a).S_{11}(dB) of the conventional CPW in UP and DOWN state

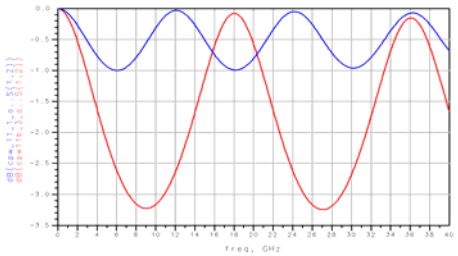

Fig.8(b).S_{12}(dB) of the conventional CPW in UP and DOWN state

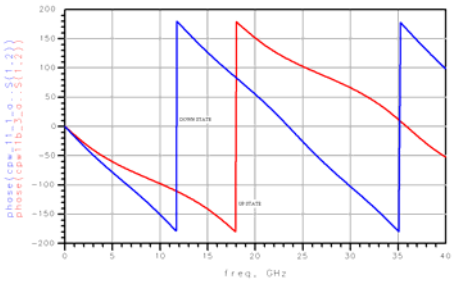

Fig.8(c).S_{12} (phase) of the conventional CPW in UP and DOWN state

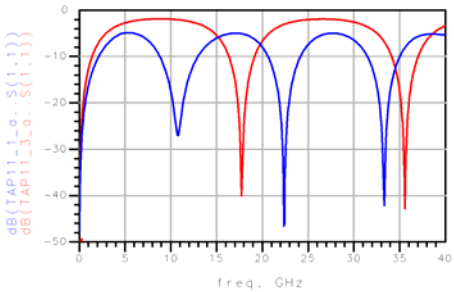

Fig. 9(a). S_{11} (dB) of the linear tapered CPW Design – I in UP and DOWN state

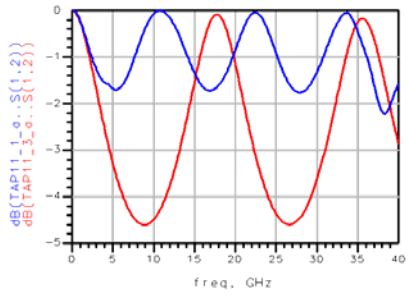

Fig. 9(b). S_{12} (dB) of the linear tapered CPW – I in UP and DOWN state

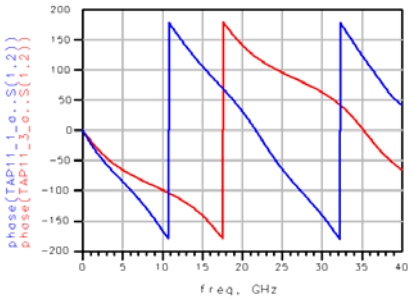

Fig. 9(c). S_{12} (phase) of the linear tapered Design CPW Design – I in UP and DOWN state

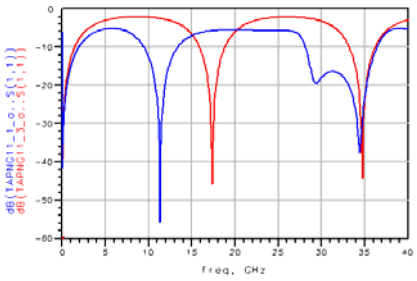

Fig. 10(a). S_{11} (dB) of the linear tapered CPW Design – II in UP and DOWN state

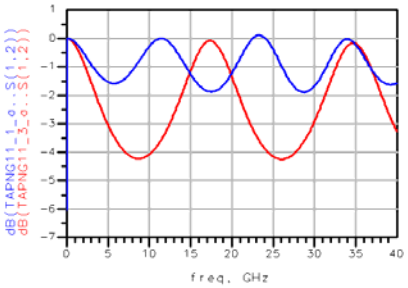

Fig. 10(b). S_{12} (dB) of the linear tapered CPW Design – II in UP and DOWN state

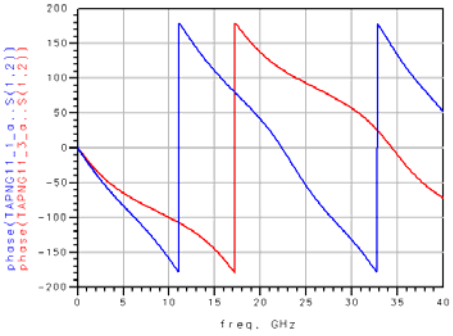

Fig. 10(b). S_{12} (phase) of the linear tapered CPW Design – II in UP and DOWN state

Table. 2

In consolidating the results for the various CPW phase shifter designs

Parameters	Conventional CPW Phase shifter		Tapered CPW Phase Shifter – Design I		Tapered CPW Phase Shifter – Design II	
	UP State	**DOWN State**	**UP State**	**DOWN State**	**UP State**	**DOWN State**
S_{11} (dB)	-9.711	-7.941	-6.650	-8.168	-5.952	-5.533
S_{12} (dB)	-0.569	-0.804	-1.149	-0.854	-1.358	-1.224
S_{12} (°)	151	55	145	32	140	38
Change in Phase	96		113		102	

6. Conclusions

MEMS phase shifter using different transmission lines have been designed and simulated. It indicates tapered CPW Design-I produce more phase shift among the three designs. Accurate phase shift change and relatively low insertion loss are obtained. The future work is to increase the isolation, reduce the insertion loss and mainly to increase the phase shift per unit length.

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