HVDC LINK DETAILED MODEL AND CONTROL DESIGN FOR DYNAMIC SIMULATIONS

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This paper presents an approach to modelling MMC-HVDC converters using detailed equivalent schemes, which are more suitable for dynamic simulations. Next, a thorough view is given to converter controller design, focusing on modulus optimum criterion for parameter tuning. Finally, the model and controller are validated using Matlab/Simulink.

Keywords: modular multilevel converter, high voltage direct current transmission, vector control

1. Introduction

The modular-multilevel-converter (MMC) is an emerging technology which enables high voltage direct current (HVDC) transmission. One of the reasons why it is increasingly regarded, is that it provides support to the AC network, by fully controlling the active power and the reactive power (separately from the active power). Moreover, the MMC-HVDC is a topic of interest for both the academia and the industry. In fact, this technology was first presented by Prof. Reiner Marquardt from the University of Munich and it was quickly put to use in the Trans-Bay-Cable project by Siemens, in 2010. Ever since, the MMC has been further deployed in China, Germany, between France and Spain etc., with more than 40 projects being completed and in use. This paper is focused on showing the proper approach to MMC-HVDC modelling and control which are targeted for dynamic simulations, by using detailed equivalent models and vector control.

2. Model for MMC-HVDC using Half-Bridge Submodules

The MMC-HVDC converter consists of three phase units, and each phase unit is made from an upper and lower multivalve (MV) (also called upper and lower arm). Each MV consists of several submodules (SM), typically made from a half-bridge (HB) circuit. Moreover, depending on the desired output voltage, the SMs will be bypassed or inserted. Due to this modularity, the output voltage will

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have low harmonic content and the need for filter will be diminished. Additionally, active and reactive power can be controlled separately, which leads to great flexibility. When the converter is in operation, it is necessary to ensure that SM capacitor voltages remain in a narrow band during charging and discharging, which happens because of the change in current polarity.

For dynamic simulations, the most appropriate modelling technique is the detailed equivalent model (DEM). The objective of DEM is to reduce SMs to a "one resistor – one voltage source" per MV [1] [2]. As such, the IGBTs and antiparallel diodes are represented by resistances, and the capacitor is represented by an equivalent voltage source in series with a resistance. This conversion (equivalence) is summarized in Fig. 1. Consequently, the IGBT can be equivalated to two resistors (Fig. 1.b). Next, it is possible to construct a Thevenin equivalent circuit (EC) consisting of a voltage source and a resistance (Fig. 1.c).

The SM can have three states:

1. If the SM is inserted, then R_1 will have a low value, only reflecting the conduction losses. R_2 will have a high value.
2. If the SM is bypassed, then R_2 will have a low value and R_1 will have a high value.
3. If the SM is blocked, then both R_1 and R_2 will have a high value.

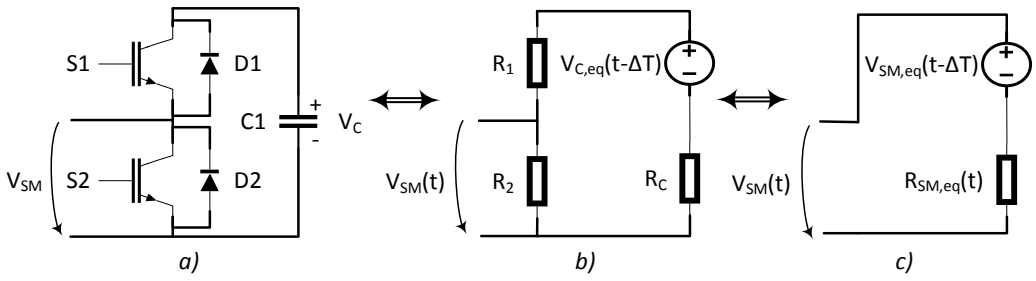

Fig. 1. The EC of a HB SM: a) SM structure; b) EC; c) Thevenin EC

Firstly, the voltage of the equivalent voltage source can be calculated using a trapezoidal integration method, applied to capacitor current equation:

$$\boldsymbol{I_C(t) = C\frac{dV_C}{dt}} \tag{1}$$

Integrating eq. (1) for the time interval between t - ΔT and t, and applying the trapezoidal integration method, the following equation is identified:

$$\boldsymbol{V_C(t) = \frac{\Delta T}{2C}I_C(t) + \frac{\Delta T}{2C}I_C(t-\Delta T) + V_C(t-\Delta T)} \tag{2}$$

Considering eq. (3) and (4), the voltage is defined as in eq. (5):

$$\boldsymbol{R_C = \frac{\Delta T}{2C}} \tag{3}$$

$$\boldsymbol{V_{C,eq}(t-\Delta T) = \frac{\Delta T}{2C} I_C(t-\Delta T) + V_C(t-\Delta T)} \tag{4}$$

$$\boldsymbol{V_C(t) = R_C I_C(t) + V_{C,eq}(t-\Delta T)} \tag{5}$$

For the calculation of R_1 and R_2, an iterative method is used. From the equivalent circuit, a simplified Thevenin equivalent circuit is developed. As such, an equivalent voltage source ($V_{SM,eq}$) and an equivalent resistance ($R_{SM,eq}$) is used.

The SM voltage is defined as:

$$\boldsymbol{V_{SM}(t) = R_{SM,eq}(t) I_{MV}(t) + V_{SM,eq}(t-\Delta T)} \tag{6}$$

The values of $V_{SM,eq}$ and $R_{SM,eq}$ are calculated using a two-step Thevenin approach, which leads to:

$$\boldsymbol{R_{SM,eq}(t) = \frac{R_2(t) * (R_1(t) + R_C)}{R_2(t) + R_1(t) + R_C}} \tag{7}$$

$$\boldsymbol{V_{SM,eq}(t-\Delta T) = R_2(t) * i(t) = V_{C,eq}(t-\Delta T) \frac{R_2(t)}{R_2(t) + R_1(t) + R_C}} \tag{8}$$

The current which passes through each SM (I_{MV}) is in fact the current which passes through the MV. Considering n SMs which make up the MV, the voltage output of the MV (V_{MV}) can be defined as:

$$V_{MV}(t) = R_{eq}(t) I_{MV}(t) + V_{eq}(t-\Delta T) \tag{9}$$

The values of V_{eq} and R_{eq} are calculated as follows:

$$R_{eq}(t) = \sum_{i=1}^{nrSM} R_{SMi,eq}(t) \tag{10}$$

$$V_{eq}(t-\Delta T) = \sum_{i=1}^{nrSM} V_{SMi,eq}(t-\Delta T) \tag{11}$$

3. MMC-HVDC Control

The most used control method is based on vector control, for which the three-phase system voltages and currents are translated into a stationary frame ($\alpha\beta\gamma$) and are associated to a rotating vector (Clarke transformation), after which Park transformation is applied, in order to obtain a rotating frame (*dq0*) in which the associated vector is stationary respective to the rotating frame. This leads to a more streamlined approach to controller design, since controlled values are not sinusoidal. It is possible to directly move between the (*abc*) frame and the (*dq0*) frame, by using the forward transformation and the reverse transformation, applied to three phase voltages v_a, v_b, v_c, and currents i_a, i_b, i_c,

The instantaneous active and reactive powers are expressed using (12) and (13), where "·" denotes the scalar product and "×" represents the cross product:

$$\begin{cases} \boldsymbol{p} = \underline{\boldsymbol{v}}_{\boldsymbol{abc,r}}{}^{\boldsymbol{T}} \cdot \underline{\boldsymbol{i}}_{\boldsymbol{abc,r}} & (12) \\ \boldsymbol{q} = \underline{\boldsymbol{v}}_{\boldsymbol{abc,r}}{}^{\boldsymbol{T}} \times \underline{\boldsymbol{i}}_{\boldsymbol{abc,r}} & (13) \end{cases}$$

$$\underline{\boldsymbol{v}}_{\boldsymbol{abc,r}} = \begin{bmatrix} \boldsymbol{v_a} \\ \boldsymbol{v_b} \\ \boldsymbol{v_c} \end{bmatrix} \qquad \underline{\boldsymbol{i}}_{\boldsymbol{abc,r}} = \begin{bmatrix} \boldsymbol{i_a} \\ \boldsymbol{i_b} \\ \boldsymbol{i_c} \end{bmatrix} \tag{14}$$

Because in the steady state condition, the phase-locked-loop ensures that the voltage phasor is always placed on the direct axis, this means the quadrature voltage is zero. By neglecting the zero component, the two powers become:

$$\begin{cases} \boldsymbol{P_S} = \dfrac{\boldsymbol{3}}{\boldsymbol{2}} \boldsymbol{v_d i_d} \\ \boldsymbol{Q_S} = -\dfrac{\boldsymbol{3}}{\boldsymbol{2}} \boldsymbol{v_d i_q} \end{cases} \tag{15}$$

Therefore, active power reference influences direct axis current and the reactive power reference influences quadrature axis current.

One MMC-HVDC converter arm consists of several SMs, in series with an arm reactor, which is connected to the AC side through a power transformer. The insertion/bypass of SMs can be assimilated to an AC voltage source, in series with a resistance (associated to conduction losses) and the arm reactor. Converter AC side can be modelled through a voltage source in series with a resistance and a reactor. The equivalent one-phase circuit is presented in Fig. 2. Next, Kirchhoff's voltage loop is applied to the upper arm and lower arm, as seen in (16)[3].

$$\begin{cases} \boldsymbol{V_{MV,u}} + \boldsymbol{R_{arm} i_u} + \boldsymbol{L_{arm}} \dfrac{\boldsymbol{di_u}}{\boldsymbol{dt}} + \boldsymbol{R_t i_s} + \boldsymbol{L_t} \dfrac{\boldsymbol{di_s}}{\boldsymbol{dt}} + \boldsymbol{V_s} = \dfrac{\boldsymbol{V_{DC}}}{\boldsymbol{2}} \\ -\boldsymbol{V_{MV,l}} - \boldsymbol{R_{arm} i_l} - \boldsymbol{L_{arm}} \dfrac{\boldsymbol{di_l}}{\boldsymbol{dt}} + \boldsymbol{R_t i_s} + \boldsymbol{L_t} \dfrac{\boldsymbol{di_s}}{\boldsymbol{dt}} + \boldsymbol{V_s} = -\dfrac{\boldsymbol{V_{DC}}}{\boldsymbol{2}} \end{cases} \tag{16}$$

Firstly, in order to obtain the AC circuit equivalent model, the two equations in (16)(16) are added. The resulting equation is divided by 2, while considering eq. (17) and (18). This leads to eq. (19).

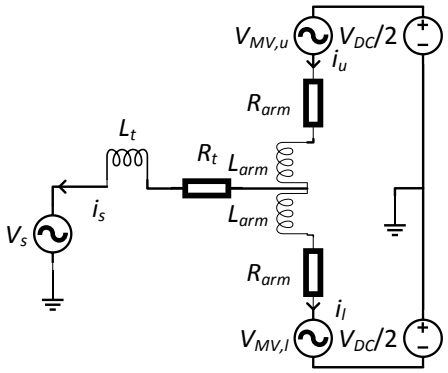

Fig. 2. Simplified model of a one-phase converter

$$\boldsymbol{i_s = i_u - i_l} \tag{17}$$

$$\boldsymbol{(V_{MV,u} - V_{MV,l})/2 = V_{MV,AC}} \tag{18}$$

$$V_{MV,AC} + V_s = -i_s\left(\frac{R_{arm}}{2} + R_t\right) - \frac{di_s}{dt}\left(\frac{L_{arm}}{2} + L_t\right) \tag{19}$$

Next, Park is applied to the terms in equation (19)(19).

$$T_r \cdot \begin{bmatrix} V_{MV,d} \\ V_{MV,q} \\ V_{MV,0} \end{bmatrix} + T_r \cdot \begin{bmatrix} V_{s,d} \\ V_{s,q} \\ V_{s,0} \end{bmatrix} = -T_r \cdot \left(\frac{R_{arm}}{2} + R_t\right) \cdot \begin{bmatrix} i_{s,d} \\ i_{s,q} \\ i_{s,0} \end{bmatrix} - \frac{d}{dt}\left(T_r \cdot \begin{bmatrix} i_{s,d} \\ i_{s,q} \\ i_{s,0} \end{bmatrix}\right) \cdot \left(\frac{L_{arm}}{2} + L_t\right) \tag{20}$$

The conclusion which can be drawn, based on (20), is the fact that current $i_{s,d}$ is influenced by $i_{s,q}$ and vice-versa. However, it is possible to decuple them using feed-back and feed-forward loops, as shown in [4]. The multivalve voltages $V_{MV,d}$ and $V_{MV,q}$ are expressed using (21) and (22):

$$\begin{cases} \boldsymbol{V_{MV,d} = \dfrac{V_{DC}}{2} \cdot m_d} \\ \boldsymbol{V_{MV,q} = \dfrac{V_{DC}}{2} \cdot m_q} \end{cases} \tag{21}$$

$$\begin{cases} \boldsymbol{m_d = \dfrac{2}{V_{DC}} \cdot \left[u_d + \left(\dfrac{L_{arm}}{2} + L_t\right) \cdot \dfrac{d\delta}{dt} i_{s,q} - V_{s,d}\right]} \\ \boldsymbol{m_q = \dfrac{2}{V_{DC}}\left[u_q - \left(\dfrac{L_{arm}}{2} + L_t\right) \cdot \dfrac{d\delta}{dt} i_{s,d} - V_{s,q}\right]} \end{cases} \tag{22}$$

Replacing $m_d$and m_q in equation (21) based on (22), replacing the resulting $V_{MV,d}$ and $V_{MV,q}$ and applying Laplace transformation leads to:

$$\begin{cases} \boldsymbol{u_d(s) = -\left(\frac{R_{arm}}{2} + R_t\right) \cdot i_{s,d}(s) - \left(\frac{L_{arm}}{2} + L_t\right) \cdot s \cdot i_{s,d}(s)} \\ \boldsymbol{u_q(s) = -\left(\frac{R_{arm}}{2} + R_t\right) \cdot i_{s,q}(s) - \left(\frac{L_{arm}}{2} + L_t\right) \cdot s \cdot i_{s,q}(s)} \\ \boldsymbol{V_{MV,0}(s) + V_{s,0}(s) = -\left(\frac{R_{arm}}{2} + R_t\right) \cdot i_{s,0}(s) - \left(\frac{L_{arm}}{2} + L_t\right) \cdot s \cdot i_{s,0}(s)} \end{cases} \quad (23)$$

The first two equations of (23) are now decoupled (independent). Therefore, it is possible to control $i_{s,d}$ through u_d and $i_{s,q}$ through u_q:

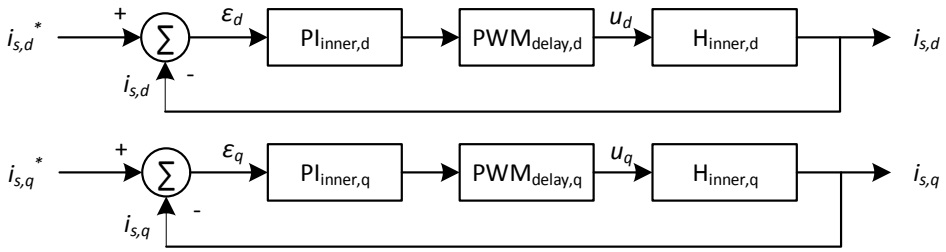

Fig. 3. Inner decoupled control loops

In Fig. 3, $H_{inner,d}$ and $H_{inner,q}$ are process transfer functions based on (24):

$$\begin{cases} \boldsymbol{H_{inner,d}(s) = \frac{i_d(s)}{u_d(s)} = \frac{1}{-\left(\frac{L_{arm}}{2} + L_t\right) \cdot s - \left(\frac{R_{arm}}{2} + R_t\right)}} \\ \boldsymbol{H_{inner,q}(s) = \frac{i_q(s)}{u_q(s)} = \frac{1}{-\left(\frac{L_{arm}}{2} + L_t\right) \cdot s - \left(\frac{R_{arm}}{2} + R_t\right)}} \end{cases} \quad (24)$$

Moreover, $PI_{inner,d}$ and $PI_{inner,q}$ are the inner controllers, and are defined using the following first order transfer functions:

$$\begin{cases} \boldsymbol{PI_{inner,d}(s) = \frac{k_{p,d}s + k_{i,d}}{s}} \\ \boldsymbol{PI_{inner,q}(s) = \frac{k_{p,q}s + k_{i,q}}{s}} \end{cases} \quad (25)$$

The delay introduced by the PWM generator and the switching actions is modelled through transfer functions $PWM_{delay,d}$ and $PWM_{delay,q}$. The time delay of the PWM generator and converter is chosen as half the switching period.

$$PWM_{delay,d}(s) = PWM_{delay,q}(s) = \frac{1}{T_{delay} \cdot s + 1} \quad (26)$$

Tuning of the PI controllers is done through modulus optimum criterion [5] [6] [7]. This ensures fast response. Because both the *d* and *q* axis controllers are identical, only one will be calculated. The open loop transfer function of the *d* axis loop is:

$$\boldsymbol{H_{OL,d}(s)} = \frac{\frac{\boldsymbol{k_{p,d}}}{\boldsymbol{k_{i,d}}}\boldsymbol{s}+\boldsymbol{1}}{\frac{\boldsymbol{1}}{\boldsymbol{k_{i,d}}}\boldsymbol{s}} \cdot \frac{\boldsymbol{1}}{\boldsymbol{T_{delay}}\cdot\boldsymbol{s}+\boldsymbol{1}} \cdot \frac{\boldsymbol{1}}{\left[-\left(\frac{\boldsymbol{R_{arm}}}{\boldsymbol{2}}+\boldsymbol{R_t}\right)\right]\cdot\left[\frac{-\left(\frac{\boldsymbol{L_{arm}}}{\boldsymbol{2}}+\boldsymbol{L_t}\right)}{-\left(\frac{\boldsymbol{R_{arm}}}{\boldsymbol{2}}+\boldsymbol{R_t}\right)}\cdot\boldsymbol{s}+\boldsymbol{1}\right]} \tag{27}$$

According to the modulus optimum criterion, it is possible to cancel the slow process pole by the controller zero, as done in (28), which leads to (29).

$$\frac{\boldsymbol{k_{p,d}}}{\boldsymbol{k_{i,d}}}\boldsymbol{s}+\boldsymbol{1} = \frac{-\left(\frac{\boldsymbol{L_{arm}}}{\boldsymbol{2}}+\boldsymbol{L_t}\right)}{-\left(\frac{\boldsymbol{R_{arm}}}{\boldsymbol{2}}+\boldsymbol{R_t}\right)}\cdot\boldsymbol{s}+\boldsymbol{1} \tag{28}$$

$$\boldsymbol{H_{OL,d}(s)} = \frac{\boldsymbol{1}}{-\left(\frac{\boldsymbol{R_{arm}}}{\boldsymbol{2}}+\boldsymbol{R_t}\right)\cdot\frac{\boldsymbol{1}}{\boldsymbol{k_{i,d}}}\cdot\boldsymbol{T_{delay}}\cdot\left(\boldsymbol{s}+\frac{\boldsymbol{1}}{\boldsymbol{T_{delay}}}\right)\boldsymbol{s}} \tag{29}$$

According to modulus optimum criterion, the open loop transfer function should have the following format:

$$\boldsymbol{H_{BO}(s)} = \frac{\boldsymbol{\omega_0^2}}{\boldsymbol{s}\cdot\left(\boldsymbol{s}+\sqrt{\boldsymbol{2}}\boldsymbol{\omega_0}\right)} = \boldsymbol{H_{OL,d}(s)} \tag{30}$$

Therefore, the term ω_0 is equal to:

$$\boldsymbol{\omega_0} = \frac{\boldsymbol{1}}{\sqrt{\boldsymbol{2}}\boldsymbol{T_{delay}}} \tag{31}$$

Moreover, from (29) and (30) ω_0^2 equals to:

$$\boldsymbol{\omega_0^2} = \frac{\boldsymbol{1}}{-\left(\frac{\boldsymbol{R_{arm}}}{\boldsymbol{2}}+\boldsymbol{R_t}\right)\cdot\frac{\boldsymbol{1}}{\boldsymbol{k_{i,d}}}\cdot\boldsymbol{T_{delay}}} \tag{32}$$

From (28) (29) and (30), it can be concluded that $k_{i,d}$ and $k_{p,d}$ are equal to:

$$k_{i,d} = \frac{-\left(\frac{R_{arm}}{2} + R_t\right)}{2T_{delay}} \tag{33}$$

$$k_{p,d} = \frac{-\left(\frac{L_{arm}}{2} + L_t\right)}{2T_{delay}} \tag{34}$$

From a design perspective, the outer control loop is faster than the inner control loop. Therefore, the inner control loop can be expressed through unity transfer function or, better, through a first order transfer function, as in (36):

$$T_{eq} = 2T_{delay} \tag{35}$$

$$H_{inner} = \frac{1}{T_{eq}s + 1} \tag{36}$$

The active and reactive power is expressed through equation (15). From this equation, the following transfer functions for the system can be obtained:

$$H_{proc,P} = \frac{P_S}{i_d} = \frac{3}{2}v_d \tag{37}$$

$$H_{proc,Q} = \frac{Q_S}{i_q} = -\frac{3}{2}v_d \tag{38}$$

The PI controllers for the active power and the reactive power are:

$$PI_{outer,P} = \frac{k_{p,P}s + k_{i,P}}{s} \tag{39}$$

$$PI_{outer,Q} = \frac{k_{p,Q}s + k_{i,Q}}{s} \tag{40}$$

In Fig. 4, complete control loops for active and reactive power are shown.

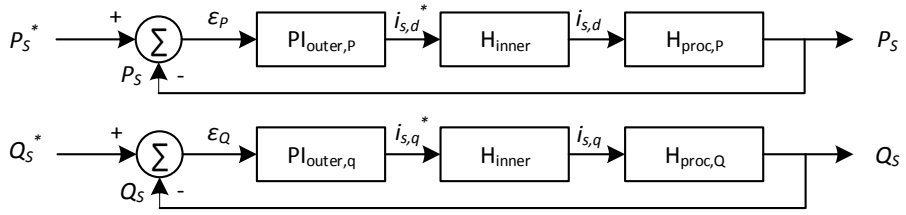

Fig. 4. Outer control loops for active and reactive power

The open loop transfer functions for the active power control and the reactive power control are:

$$\boldsymbol{H_{OL,P}(s) = \frac{k_{p,P}s + k_{i,P}}{s} \cdot \frac{1}{T_{eq}s + 1} \cdot \frac{3}{2} v_d} \tag{41}$$

$$\boldsymbol{H_{OL,Q}(s) = -\frac{k_{p,Q}s + k_{i,Q}}{s} \cdot \frac{1}{T_{eq}s + 1} \cdot \frac{3}{2} v_d} \tag{42}$$

Modulus optimum criterium is again used to find the proportional and integral constants. Eq. (41) and (42) are rewritten to obtain a format which is closer to (30):

$$\boldsymbol{H_{OL,P}(s) = \frac{k_{p,P}s + k_{i,P}}{T_{eq}} \cdot \frac{3}{2} v_d \cdot \frac{1}{s\left(s + \frac{1}{T_{eq}}\right)}} \tag{43}$$

$$\boldsymbol{H_{OL,Q}(s) = -\frac{k_{p,Q}s + k_{i,Q}}{T_{eq}} \cdot \frac{3}{2} v_d \cdot \frac{1}{s\left(s + \frac{1}{T_{eq}}\right)}} \tag{44}$$

For both previous equations, ω_0 can be identified as:

$$\boldsymbol{\omega_0 = \frac{1}{\sqrt{2}T_{eq}}} \tag{45}$$

Nevertheless, the values for the controller constants become:

$$\boldsymbol{k_{p,P} = k_{p,Q} = 0} \tag{46}$$

$$\boldsymbol{k_{i,P} = -k_{i,Q} = \frac{1}{3 v_d T_{eq}}} \tag{47}$$

DC voltage control is ensured through a balance between the AC side active power flow and the DC side active power flow. This is shown in (48):

$$\boldsymbol{V_{DC} I_{DC} = \frac{3}{2} v_d i_d} \tag{48}$$

It means that the process transfer function $H_{proc,VDC}$ can be expressed as:

$$\boldsymbol{H_{proc,VDC} = \frac{V_{DC}}{i_d} = \frac{3}{2}\frac{v_d}{I_{DC}}} \tag{49}$$

The DC voltage loop diagram can be designed in a similar manner to the power control loop, and it consists of the PI controller, the inner control loop equivalent transfer function and the process transfer function (Fig. 5):

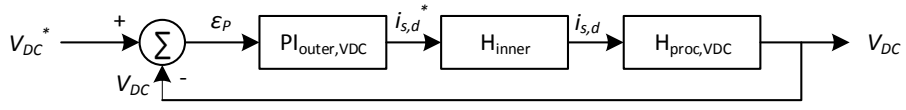

Fig. 5. Outer controller loop for DC voltage

The open loop transfer function is shown in (50) and ω_0 is given in (51):

$$H_{OL,VDC}(s) = \frac{k_{p,VDC}s + k_{i,VDC}}{T_{eq}} \cdot \frac{3}{2} \cdot \frac{v_d}{I_{DC}} \cdot \frac{1}{s\left(s + \frac{1}{T_{eq}}\right)} \tag{50}$$

$$\boldsymbol{\omega_0 = \frac{1}{\sqrt{2}T_{eq}}} \tag{51}$$

Nevertheless, the following values for controller constants are obtained:

$$k_{p,VDC} = 0;\ k_{i,VDC} = \frac{I_{DC}}{3v_d T_{eq}} \tag{52}$$

3. Case study

In this chapter, all controllers are tuned and tested on a segment of the *Cigre Working Group B4.57* network [1]. This segment consists of two converter stations, Cm-*A1* and Cm-*C1* (Fig. 6). This HVDC link is in a symmetric monopole configuration, having a rated DC voltage of ±200kV, and connects the off-shore wind power plant *B0-C1* with the on-shore AC grid *Ba-A1*.

Fig. 6. Cigre point-to-point test system [1]

The control modes of each converter are:

- *Cm-A1*: DC voltage, V_{DC}^* = ±200kV; Reactive power, Q_S^* = 0MVAr.
- *Cm-C1*: Active power, P_S^* = -400MW; Reactive power, Q_S^* = 0MVAr.

Converter losses are calculated as 0.25% of rated power. Between the two converters, an underground cable is used (Table 1). Moreover, all converter parameters are summarized in Table 2. Furthermore, switching frequency is 1000Hz. Using values presented in Table 1 and 2, as well as all equations defining PI coefficients, controller values are calculated and summarized in Table 3.

In the first scenario, at 0.5s, the rectifier active power setpoint is changed from -300MW to -400MW. Both converters have 0MVAr reactive power setpoint.

Table 1.

DC line data [1]

Line data	r_0 [Ω/km]	l_0 [mH/km]	c_0 [µF/km]	g_0 [µS/km]	Max. current [A]
DC cable +/-200kV	0.011	2.615	0.2185	0.055	1962

Table 2.

Converter data [1]

	Data	A1	C1
Rated power		800MVA	800MVA
Arm reactor		29mH	29mH
Converter transformer	Leakage reactance	35mH	35mH
	Resistance	0.363Ω	0.363Ω
	Primary rated voltage	380kV	145kV
	Secondary rated voltage	220kV	220kV
Sub-modules	Number/half arm	200	200
	Individual capacitance	10mF	10mF
	Ron	1.361mΩ	1.361mΩ

Table 3.

Control loop PI coefficients

Type of loop	Coefficient	Value
Inner control loop	kp,d = kp,q	-49.5
	ki,d = ki,q	-499.1
Active power control loop	kp,P	0
	ki,P	0.001515
Reactive power control loop	kp,Q	0
	ki,Q	-0.001515
DC voltage control loop	kp,VDC	0
	ki,VDC	1.515

As it can be seen from Fig. 7, the speed of the control system is fast enough. More specifically, the active power stabilizes in 0.04 seconds at the reference value. The small ripple, which can be seen on the active power curve, is due to the sizing of inductors and capacitors in the system. These parameters have not been changed in order to keep a reference system, which is the Cigre network. On the inverter side, there is a longer stabilisation time because the DC voltage control loop has much longer reaction time. The ripple effect is not noticeable on the measured reactive power, at both inverter and rectifier side.

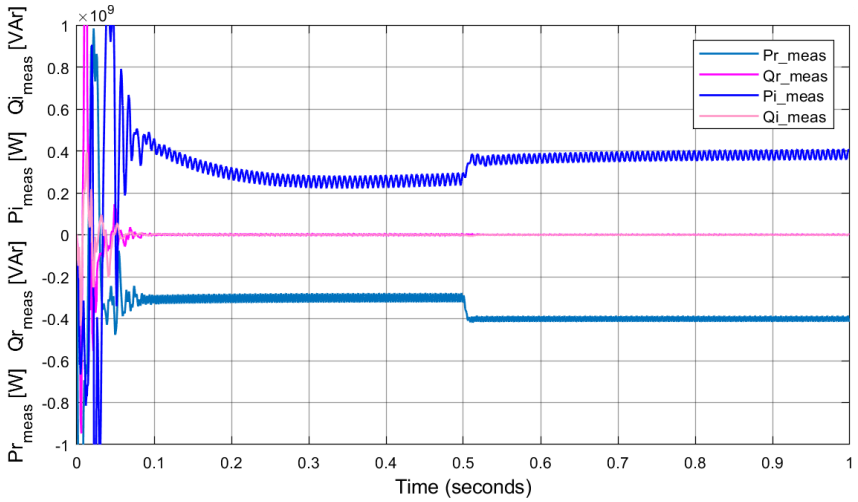

Fig. 7. Active and reactive power at rectifier and inverter AC node

Additionally, Fig. 8 shows the capacitor voltages for the upper arm of the rectifier. As it can be concluded, the balancing technique ensures a small capacitor voltage ripple. Moreover, all capacitor voltages remain within a specific band of ±10%. The capacitor voltage ripple is increased following the rise in active power.

In the second scenario, reactive power is change at time 0.5s from 0MVAr to 100MVAr, on the rectifier side. The active power changes from -400MW to -300MW at 0.6s. On the inverter side, reactive power changes from 0 to 50MVAr (at 0.6s), and the DC voltage setpoint remains unchanged.

Fig. 9 shows active and reactive power change at rectifier and inverter AC output. Graphics demonstrate that PIs have been properly tuned because the reaction time is less than 0.05s, with little overshot. Moreover, any change in active power has little influence on reactive power and vice-versa, since there is independent control for the two parameters, through decoupled *dq0* control.

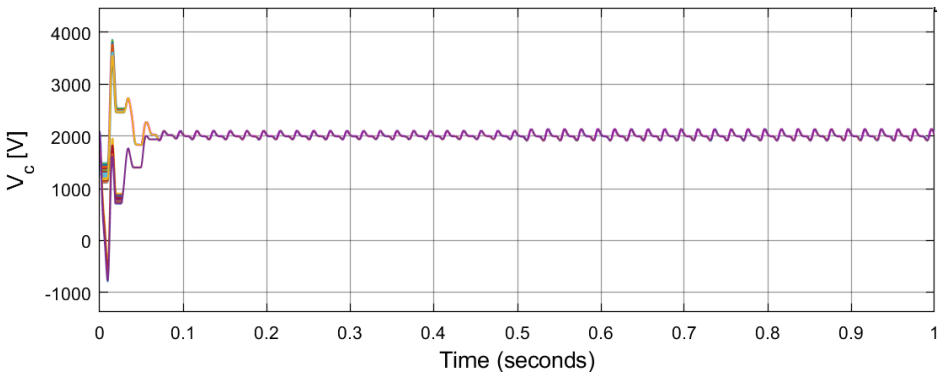

Fig. 8. Upper arm capacitor voltages for upper arm (phase a, rectifier)

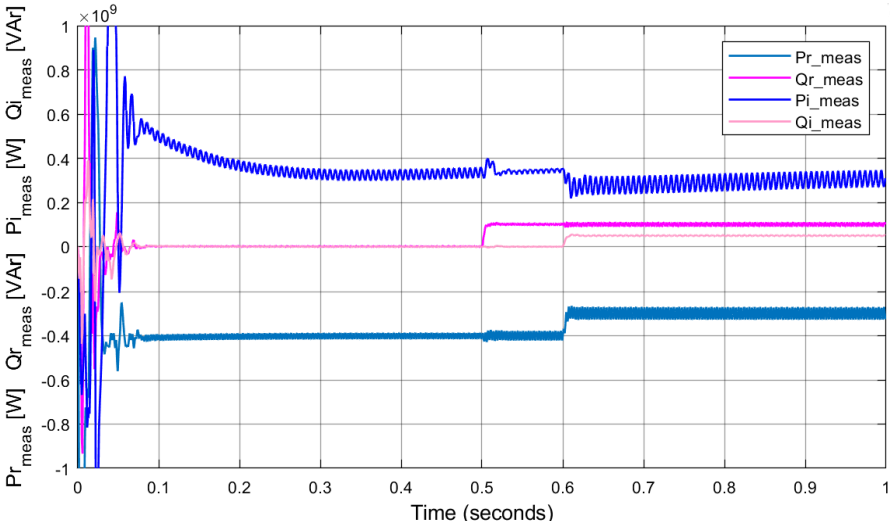

Fig. 9. Active and reactive powers at rectifier and inverter for Scenario 2

4. Conclusions

Summing up, the scope of this paper was to present the proper method for HVDC network modelling with the goal of obtaining correct control loops. Moreover, another goal was to show relevant aspects related to controller design of a HVDC link.

Furthermore, significant weight was given to the procedure of PID tuning and validation, by deploying a compact and flexible algorithm which uses *modulus optimum criterion*.

Nevertheless, several simulations were shown, with the scope of evaluating system behavior under variable conditions. All simulations were aggregated into scenarios which are representative to actual HVDC network operation: change of active power setpoint, change of reactive power setpoint etc.

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