ON THE TRANSIENTS OPTIMIZATION AND THE POWER FACTOR CORRECTION OF THE STATIC CONVERTERS

N. FULGA[1], M. O. POPESCU[2], Claudia POPESCU[3]

Obiectivul acestei lucrări constă în dezvoltarea şi implementarea unui regulator digital PID pentru convertoarele statice. Sunt studiate prin simulare şi experimentări efectele factorilor K_P, K_I şi K_D asupra răspunsului buclei de reglare. În partea a doua a lucrării, este prezentată o analiză comparativă experimentală a două convertoare (un redresor comandat realizat din tiristoare cu filtru capacitiv şi un convertor cu corecţia factorului de putere), din punct de vedere al conţinutului armonic al curenului de intrare, regimurilor tranzitorii şi dimensiunilor de gabarit.

The goal of this paper consists in the development and implementation of a digital PID controller for the static converters. The effects on the closed-loop response of the controller terms K_P, K_I and K_D are investigated through simulation and experiments. In the second part of the paper, an experimental comparative analysis of two a.c.-d.c. converters (a thyristor controlled bridge with capacitive filter and a power factor correction converter), concerning the harmonic contents of the input current, the dynamics and the size, is presented.

Keywords: d.c.-d.c. and a.c.-d.c. converters, power factor correction, digital controller, large signal transients, harmonics reduction.

1. Introduction

The recent advances in semiconductor and control technology have greatly increased the performance of the switching static converters. The d.c.-d.c. and a.c.-d.c. static converters are widely used in the industrial and commercial applications. The telecommunication industry and other industries have specific technical requirements for this converters: accurate and very stable output voltages, excellent load regulation, fast transient response, limited short circuit current, very low noise, and very low electromagnetic interference (EMI).

The many topologies of the d.c.-d.c. and a.c.-d.c. switching converters are derived from the following three types of the converters, without galvanically

[1] Eng., Research and Development Department, Electrotehnica Company of Bucharest, e-mail: nicolae.fulga@electrotehnica.ro
[2] Prof., Dept. of Electrical Measurements, Electrical Apparatus and Static Converters, University “Politehnica” of Bucharest, Romania;
[3] Prof., Dept. of Electrical Measurements, Electrical Apparatus and Static Converters, University “Politehnica” of Bucharest, Romania.

isolation, which are considered elementary structures: step-down (buck), step-up (boost) and step-down/up (buck-boost) [1]-[3].

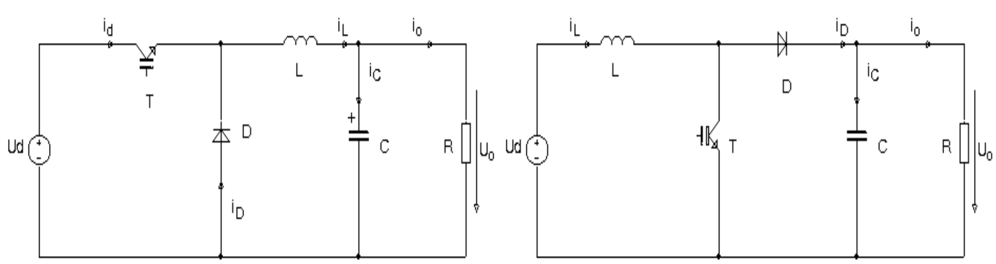
The transient responses in open loop of the elementary converters (buck, boost and buck-boost) on purpose to determine their optimal structures are investigated in [4] and [5]. In the first part of this paper, the dynamic behaviour of the closed loop d.c.-d.c. converters, through modelling and simulation, considering the load or the supply voltage variations is studied using digital controllers.

The diode or thyristor bridge rectifier with a large filter capacitor inject current harmonics in the supply mains. Due to the presence of these harmonics, the total harmonic distortions (THD) is high and the input power factor is poor. The a.c-d.c. switching converters with power factor correction are utilized to achieve a sinusoidal input current waveform that is in phase with the source voltage. In the final part of this paper, an experimental comparative analysis of two a.c.-d.c. converters (a thyristor controlled bridge with capacitive filter and a power factor correction converter), concerning the harmonic contents of the input current, the dynamics and the size, is presented.

2. Study on the transient responses of the closed-loop d.c.-d.c. converters using digital PID controller

The simulation models of a digitally controlled switching converters based on Matlab/Simulink [6], [7] are first presented. Then, the dynamic behaviour of the closed loop d.c.-d.c. converters is investigated through experiments.

Fig. 1 shows the electrical circuit diagrams of the elementary d.c.-d.c. converters (buck and boost).



a). b).

Fig. 1. The electrical circuit diagrams of the elementary d.c.-d.c. converters buck (a) and boost (b).

The dynamics of these converters operating in the continuous conduction mode (CCM) can be easily understood by applying Kirchhoff's voltage law on the loop containing the inductor L and Kirchhoff's current law on the node with the capacitor C branch connected to it.

In the case of the buck converter, when the switch T is on, the differential equations of the inductor current i_L and the capacitor voltage u_C are:

$$\frac{di_L}{dt} = \frac{1}{L}\left(U_d - R_L i_L - u_0\right), \qquad \frac{du_C}{dt} = \frac{1}{C}\left(i_L - \frac{u_0}{R}\right) \tag{1}$$

When the switch T is off, the differential equations of the inductor current i_L and the capacitor voltage u_C are:

$$\frac{di_L}{dt} = \frac{1}{L}\left(- R_L i_L - u_0\right), \qquad \frac{du_C}{dt} = \frac{1}{C}\left(i_L - \frac{u_0}{R}\right) \tag{2}$$

The output voltage u_0 is:

$$u_0 = R_C C \frac{du_C}{dt} + u_C \tag{3}$$

where R_L is equivalent series resistance (ESR) of the inductor and R_C is equivalent series resistance of the capacitor.

Utilizing these equations, the Simulink model of the buck converter is presented in Fig.2.

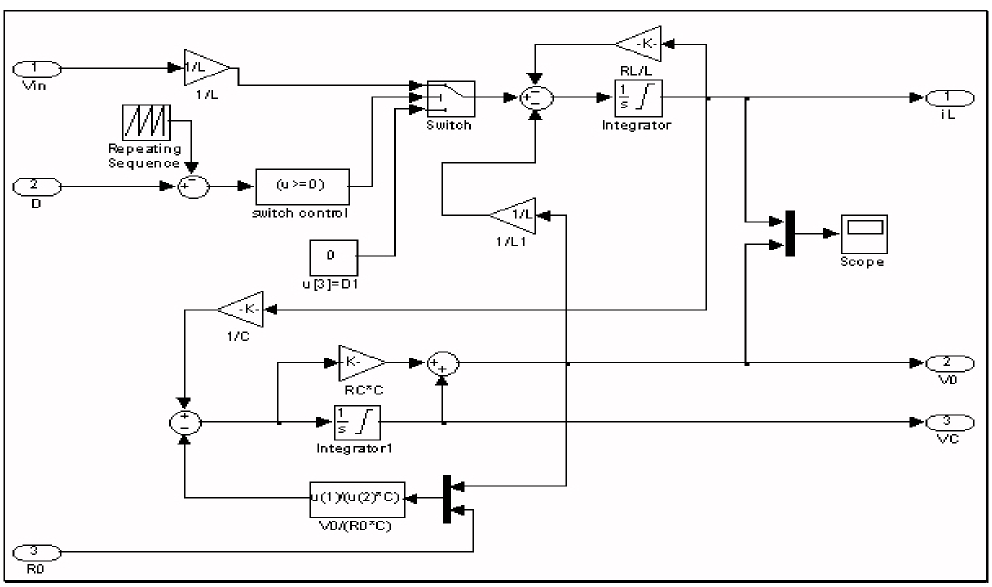


Fig. 2. Simulink model of the buck converter.

The converter duty cycle was calculated using a proportional-integral-derivative (PID) controller. The continuous time transfer function for a PID controller is given in equation (4).

$$G(s) = K_{pa} + \frac{K_{Ia}}{s} + K_{Da} \cdot s \tag{4}$$

where: K_{Pa} is the proportional gain, K_{Ia} is the integral gain, K_{Da} is the derivativ gain. This transfer function is converted to a difference equation for digital implementation:

$$d(k) = K_{pa} e(k) + K_{Ia} T \sum_j e(j) + \frac{K_{Da}}{T} \left[e(k) - e(k-1) \right] \tag{5}$$

This equation can be rewritten as:

$$d(k) = K_p e(k) + K_I \sum_j e(j) + K_D \left[e(k) - e(k-1) \right] \tag{6}$$

where: d(k) is the calculated duty cycle for the k^{th} sample, T is the sampling period, K_P is the digital proportional gain, K_I is the digital integral gain, K_D is the digital derivativ gain and e(k) is the error, defined as the difference between the measured output voltage and the desired output voltage.

The Simulink model of a digitally controlled switching converter is presented in Fig.3.

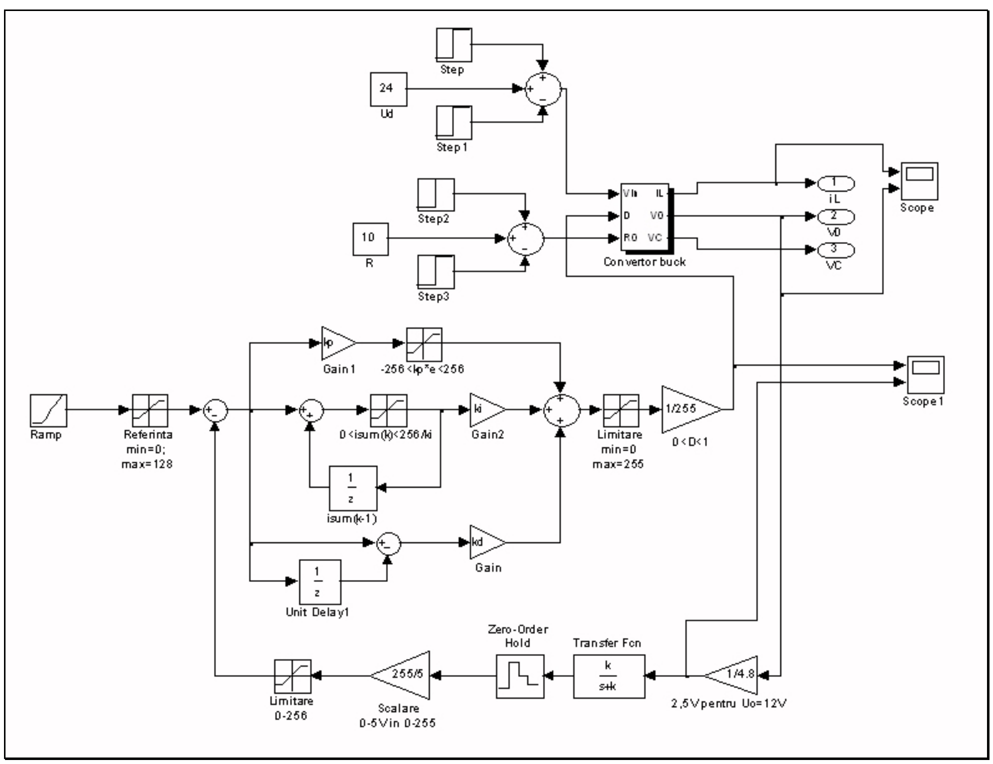
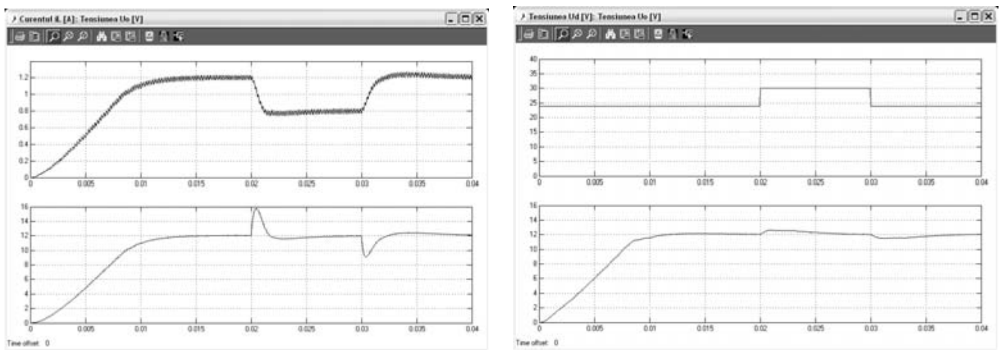


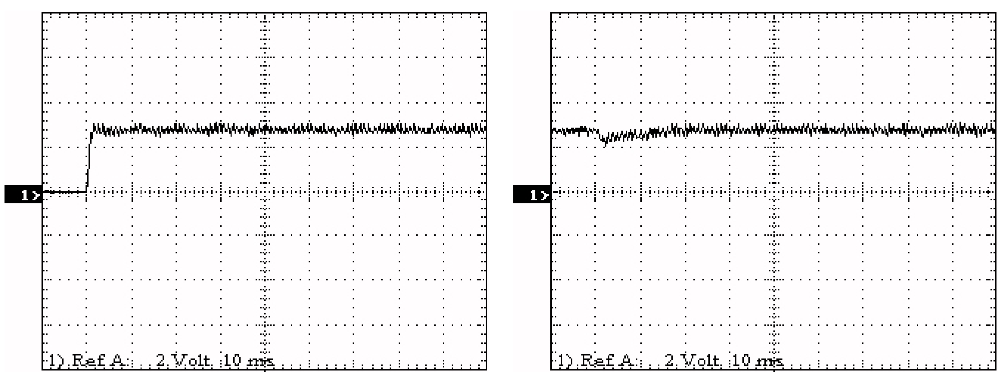
Fig. 3. Simulink model of a digitally controlled switching converter with PID regulator.

The simulation and experimental transient responses for the step variations of the load, supply voltage or reference d.c. voltage are presented in Fig. 4 and Fig. 5.



a). b).

Fig. 4. The simulation transient responses for the step variations of the load (a) or supply voltage (b).



a). b).

Fig. 5. The experimental transient responses for the step variations of the reference voltage (a) or load (b).

The effects on the closed-loop response of the controller terms K_P, K_I and K_D are presented in Table 1. A large proportional term K_P will have the effect of reducing the rise time and will reduce (but never eliminate) the steady-state error. Integral term K_I will have the effect of eliminating the steady-state error, but it will make the transient response worse. Derivative term K_D will have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response.

Table 1

Effects on the closed-loop response of the controller terms K_P, K_I and K_D

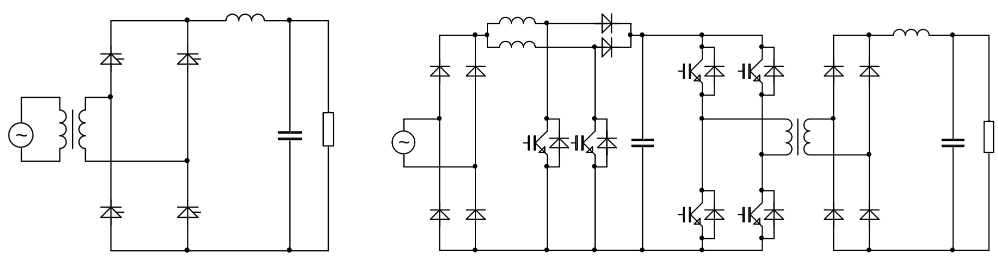
	Rise time	Overshoot	Settling time	Steady-state error
K_P	Decrease	Increase	Small change	Decrease
K_I	Decrease	Increase	Increase	Eliminate
K_D	Small change	Decrease	Decrease	Small change

These correlations are not exactly accurate, because K_P, K_I, K_D are related to each other. Changing one of these variables can change the effect of the other two.

3. An experimental comparative analysis of two a.c.-d.c. converters (a thyristor controlled bridge and a power factor correction converter)

In this section, an experimental comparative analysis of two a.c.-d.c. converters (a thyristor controlled bridge with capacitive filter and a power factor correction converter), concerning the harmonic contents of the input current, the dynamics and the size, is presented.

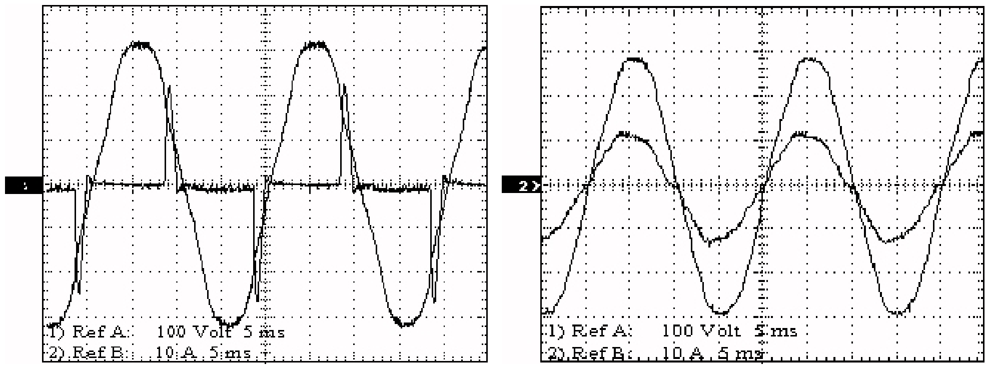
Fig. 6 shows the electrical circuit diagrams of the thyristor converter with LC filter (a) and the a.c.-d.c. converter with power factor correction (b).



a). b).

Fig. 6. The electrical circuit diagrams of the thyristor converter with LC filter (a) and the a.c.-d.c. converter with power factor correction (b).

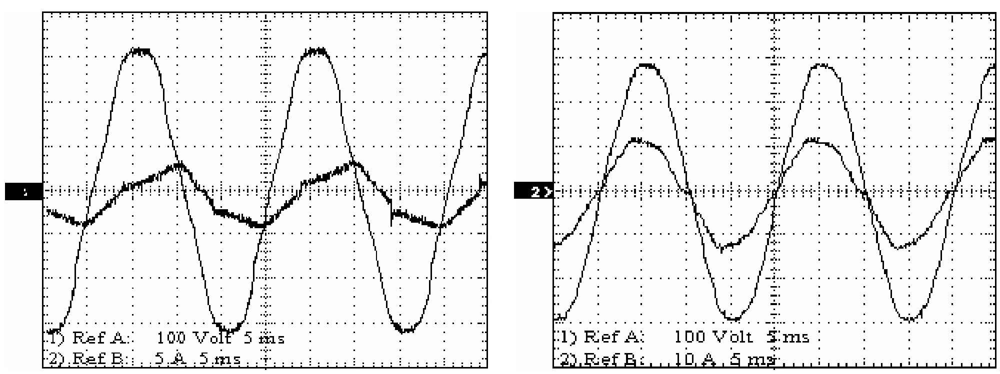
In Fig. 7 and Fig. 8 are presented the input current and supply voltage waveforms for the thyristor converter (with capacitive filter or LC filter) and for the power factor correction (PFC) converter.



a). b).

Fig. 7. The input current and supply voltage waveforms for thyristor converter with capacitive filter (a) and for PFC converter (b).

The thyristor converter with capacitive filter produces considerable harmonics and operates at varying power factors, depending on the actual firing angle. Using the capacitive-inductive (LC) low-pass filter the input current waveform are improved. In the case of the PFC converter, the input current waveform is almost sinusoidal and in phase with the supply voltage waveform.



a). b).

Fig. 8. The input current and supply voltage waveforms for thyristor converter with LC filter (a) and for PFC converter (b).

In Fig. 9 are presented the input current harmonics for the thyristor converter (with capacitive filter or LC filter) and for the power factor correction (PFC) converter.

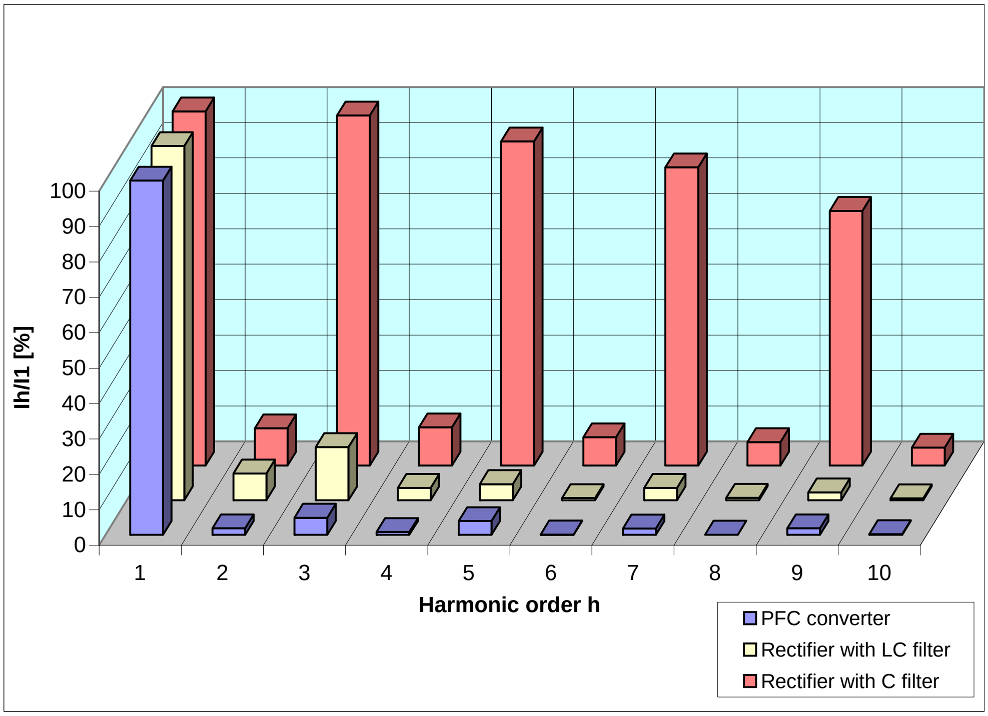


Fig. 9. The input current harmonics for thyristor converter with capacitive or LC filter and for PFC converter.

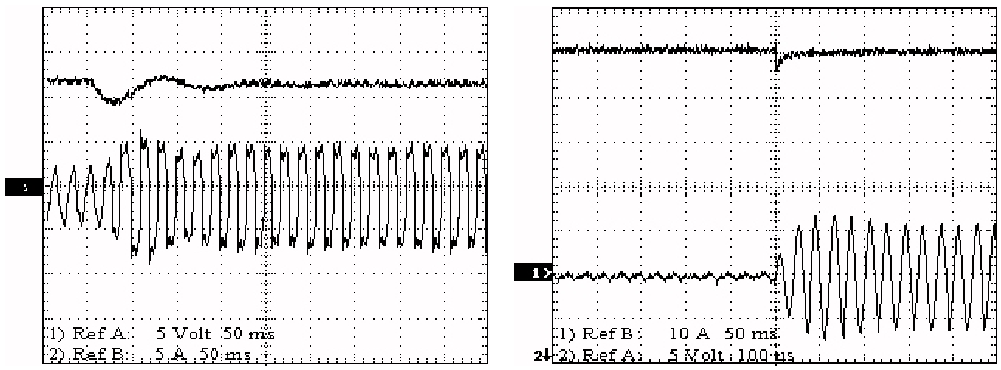
The total harmonic distortions (THD), the displacement power factor (DPF) and power factor (PF), for the thyristor converter (with capacitive filter or LC filter) and for the converter with power factor correction, are presented in Table 2.

Table 2

THD, DPF and PF for the thyristor converter (with C or LC filter) and for PFC converter

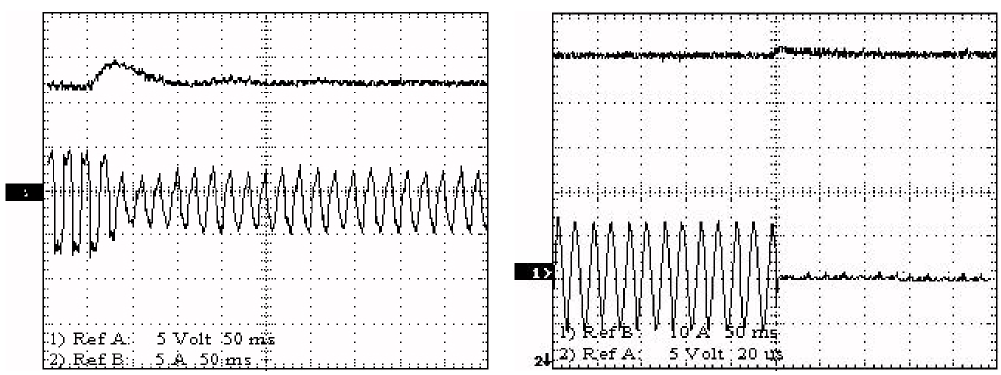
	Rectifier with C filter	**Rectifier with LC filter**	**PFC converter**
THD	175.39%	17.86%	7.02%
DPF	51.3	52.2	0.55
PF	0.261	0.575	0.976

The experimental transient responses to the load variations, for the thyristor converter with LC filter and for the power factor correction (PFC) converter are presented in Fig. 10 and Fig. 11.



a). b).

Fig. 10. The experimental transient responses to step increase load: for the thyristor converter (a) and for the PFC converter (b).



a). b).

Fig. 11. The experimental transient responses to step decrease load: for the thyristor converter (a) and for the PFC converter (b).

Analyzing the waveforms relative to the transients for two type of converters, we can conclude that the dynamic performances in the case of the PFC converter are better.

The size and weight of the PFC converter are reduced due to high switching frequency, what leads to a small isolation transformer and output filter components.

4. Conclusions

The dynamic behaviour of the closed-loop d.c.-d.c. converters, through modelling and simulation, considering the load or the supply voltage variations is studied using digital PID controllers. The results are validated by the experiments. The effects on the closed-loop response of the controller terms K_P, K_I and K_D are presented. A large proportional term K_P will have the effect of reducing the rise time. Integral term K_I will have the effect of eliminating the steady-state error, but it will make the transient response worse. Derivative term K_D will have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response.

In the final part of this paper, an experimental comparative analysis of two a.c.-d.c. converters (a thyristor controlled bridge with capacitive filter and a power factor correction converter), is achieved. The performances of the last converter, concerning the harmonic contents of the input current, the dynamics and the size, are improved.

R E F E R E N C E S

[1] *Popescu M., Manias S., Popescu Cl.*: Convertoare statice cu comutație forțată. Surse de c.c. în regim de comutație. Filtre active. Bucureşti, Ed. ICPE, 1997.

[2] *Ionescu F., Floricău D., Nițu S., Fodor D., ş.a.*: Electronică de putere. Modelare şi Simulare. Bucureşti, Ed. Tehnică, 1997.

[3] *Popescu M., Radomirescu B., Popescu Cl.*: Convertoare statice c.c.-c.c. cu comutație forțată. Bucureşti, Ed. ICPE, 1999.

[4] *Popescu M., Fulga N., Popescu Cl.:* Asupra regimurilor tranzitorii ale convertoarelor elementare buck şi boost. Simpozion SIELMEC'99, **vol. 1**, pag. 237-240, ISBN: 9975-944-30-2, Chişinău, 1999.

[5] *Fulga N., Frumuşelu S., Popescu M. O., Popescu Cl.*: Convertoare statice c.c.-c.c. cu comportare tranzitorie optimală. EEA – Electrotehnica, **vol. 50**, nr. 2, pag. 1-9, ISSN: 0376-4745, Bucureşti, 2002.

[6] *Juing-Huei Su, Jiann-Jong Chen, Dong-Shiuh Wu*.: Learning Feedback Controller Design of Switching Converters via Matlab/Simulink, IEEE Transactions on Education, **vol. 45**, no. 4, 2002.

[7] *Boudreaux, R.R.; Nelms, R.M.; Hung, J.Y.*: Simulation and Modeling of a DC-DC Converter Controlled by an 8-bit Microcontroller, IEEE APEC'97, **vol.2**, pp. 963 - 969, 23-27 Feb. 1997.