PROGRAMMABLE VOLTAGE REFERENCE FOR A LOW VOLTAGE MONITOR CIRCUIT

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Aplicațiile de joasă putere, alimentate din baterii, au cunoscut o dezvoltare continuă în ultimii ani. Acestea își găsesc utilitatea în produsele portabile, ceea ce impune restricții în privința dimensiunilor fizice şi a puterii consumate. De asemenea, un alt scop important este reducerea costurilor de producție pentru a permite lansarea produselor finale pe piață la prețuri mai mici. Toate aceste cerințe conduc către dezvoltarea de circuite care pot fi alimentate dintr-o singură baterie şi care pot funcționa în parametrii normali la tensiuni şi curenți de alimentare mici. Circuitul monitor de tensiune cu referință de tensiune programabilă care va fi prezentat în această lucrare îndeplineşte condițiile enumerate mai sus, ceea ce se verifică prin implementarea experimentală.

Low-power, battery supplied applications have known a continuous development in the last years. They are mainly implemented for portable products and, therefore, there is a restrain regarding the physical dimensions and the power consumption. At the same time there is a request to reduce the costs for such application in order to provide them on the market at lower prices. These conditions stress the need to develop circuits that can be supplied from a single battery and that are able to function in good parameters at low supply voltages and currents. The voltage monitor circuit with programmable voltage reference that will be presented in this paper meets these expectations, as the experimental implementation demonstrates.

Keywords: programmable floating gate voltage reference, switched capacitor hysteresis

1. Introduction

A big area of interest in nowadays electronics is the development of portable applications, supplied from battery, that exemplify low-power operation obtained by aiming for low supply voltage and low quiescent current. For portability reasons, the size of the equipment has to be reduced, imposing a maximum integration of the circuitry. However, as the size and the number of batteries is now becoming one of the important limiting factors, the reduction of

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the power dissipation has become a design constraint [1]. As consequence, for the voltage monitor circuit with programmable voltage reference presented in this paper we will have as a target supply voltages down to 0.9V and supply currents lower than 10μA.

Design methodology for low power circuits has known several approaches and some of them are the use of sub-threshold MOS operation [2], the scaling of the threshold voltages of the implemented transistors [3] or the development of circuitry on alternative technologies as the double-gate (DG) MOSFET architectures on system-on-insulator (SOI) substrates [4].

The voltage monitor circuit that is referred to in this paper is presented in Fig. 1. It monitors the supply voltage, V_{DD}, and outputs a logic signal, active low, when it drops below a set limit. The circuit includes a comparator, Comp, an internal voltage reference, V_{REF}, implemented with programmable Floating Gate Devices, logic control blocks and an open drain output. When the monitored V_{DD} input exceeds the set limit, the RESET alarm output is deactivated by the Reset Logic block, with a delay time set by the Timer block. The circuit also provides a Manual Reset, MR, logic input which is active on zero logic and has an internal pull-up resistor.

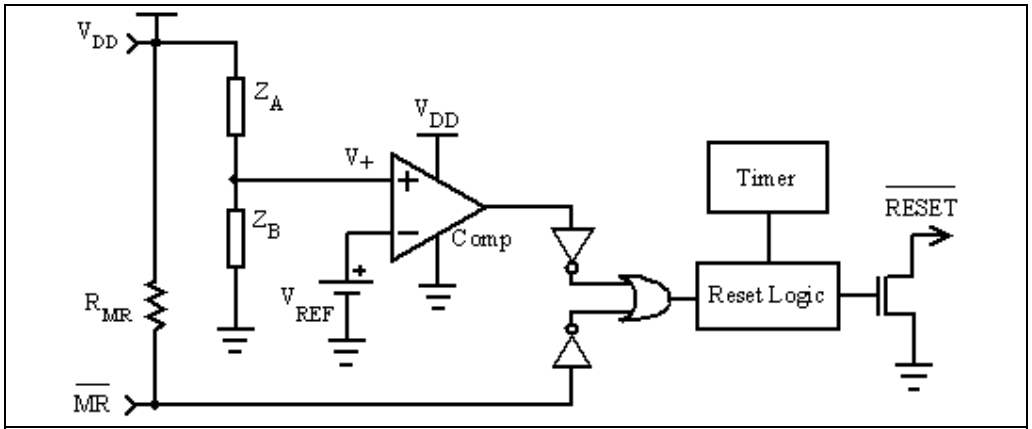

Fig. 1. Voltage Monitor Block Schematic

As a summary, the discussed circuit has as main target to monitor its supply voltage that can go below 1V, comparing it to a programmable limit value that can go as low as 0.86V, while having a stand-by supply current of typically 1.5μA. The application is also providing an internally generated hysteresis that will be further detailed in the next chapter.

For achieving functionality at low voltage supplies and low power consumption we had to implement all analog circuitry using low threshold MOS

transistors and to find a low quiescent current solution including for the voltage divider composed by Z_A and Z_B.

2. Solutions for achieving the supply voltage level and power consumption goals for this application

2.1 Conveniently choosing the transistor type

Low power consumption is one of the requests that have to be met in nowadays applications. At the same time, nominal power supply voltage for scaled technologies has to be lowered mainly in order to reduce the device internal electric fields and the active power consumption, which is proportional to V_{DD}^2. The scaling of gate oxide thickness, source - drain extension, junction depths and gate lengths resulted in reducing the MOS gate dimensions from 10μm in the 1970's to a present day size of tens of nanometers [5]. As nominal V_{DD} lowers, V_{th} must also be reduced in order to maintain performance, but lower values for V_{th} lead to higher off-state leakage currents. However, constant field scaling requires a scaling of the threshold voltage proportional to the feature size reduction. The resulted threshold voltage range is limited by the sub-threshold slope of the MOS transistor, which, in its turn, is limited by the thermal voltage kT/q, where k is the Boltzmann constant and q the electron charge [6].

Challenges that are related to the scaling process refer to digital drive currents (since saturation current is proportional to $(V_{gs} - V_{th})^2$) and parasitic effects such as leakages, capacitances, resistances. As shown, dynamic power and leakage current are the major sources of power consumption in CMOS circuitry (especially important for portable applications).

For the present application, a 0.5μm technology was available for implementation. However, for the low supply voltages considered, the voltage drop across the gate and the source of a MOS transistor diminishes. It follows that low threshold MOS transistors are needed for operation at lower power supplies.

Further more, for selecting the V_{th} levels, speed and stand-by power limitations have to be evaluated. All these considered, for the present application we chose the solution of using transistors with different threshold values across the circuit in a manner that would suit the targeted application parameters. For example, we could use low V_{th} transistors where it is needed for functionality and speed reasons, and high V_{th} transistors for the rest of the circuitry, particularly for the digital blocks were we need to eliminate the off-state leakage problem. In the application we are discussing here, for the analogical blocks we used Low Voltage NMOS transistors (LV NMOS) with 0.3V threshold and Low Voltage PMOS transistors (LV PMOS) with -0.3V threshold, while for the digital blocks we used NMOS transistors with 0.5V threshold and PMOS transistors with -0.5V threshold.

2.2 Low quiescent current implementation for the Z_A – Z_B voltage divider

In order to maintain a low current consumption for the entire application, we need to minimize the current flow into the voltage divider composed by Z_A and Z_B (Fig. 1). But implementing it with resistors will lead to large area consumption because, for limiting the quiescent current, we would need high resistor values. For economic reasons we aim to reduce as much as possible the silicon area the chip occupies. For meeting these expectations, we replace the resistive divider with a capacitive one, having a zero dc current consumption.

In order to develop the mathematical equations, we will consider that Z_A will be implemented with capacitor C_A, and Z_B with capacitor C_B. The voltage on the non-inverting input of the comparator (V_+) will be:

$$V_+ = V_{DD} \cdot \frac{Z_B}{Z_A + Z_B} \text{ where } Z_A = \frac{1}{j\omega C_A} \text{ and } Z_B = \frac{1}{j\omega C_B}$$

leading to:

$$V_+ = V_{DD} \cdot \frac{C_A}{C_A + C_B} = V_{DD} \cdot r \tag{1}$$

It follows that the ratio (r) between the two considered voltages will depend only on the ratio of the capacitances. The area occupied by this type of voltage divider is significantly lower than the one of the resistive divider. However, one should not choose to work with minimum capacitances because they would be more likely to be affected by process variations that could alter their matching.

2.3 Low quiescent current implementation for the comparator hysteresis schematic

Small amounts of parasitic feedback or noise or interference that affect a comparator input signal can cause undesirable rapid changes between its output states, especially when the input voltage level is close to the voltage reference value. In order to avoid these parasitic transitions, internal hysteresis is introduced generally by using positive feedback. Besides, this method also offers a fast output transition from one state to the other, considerably reducing the time of the indeterminate state.

The proposed hysteresis schematic (Fig. 2) takes advantage of the fact that we are using a capacitive divider on the non-inverting input of the comparator. It

comprises the capacitive voltage divider (C_1-C_2) and one positive feedback capacitor C_3 which is switched between V_{DD} and ground by the output voltage of the comparator [7].

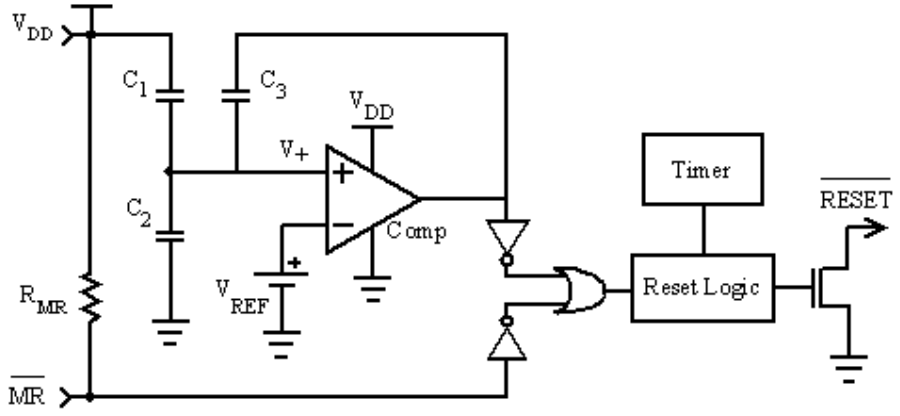

Fig. 2. Voltage Monitor Detailed Block Schematic

Two cases will be considered. First, when voltage V_+ is above the V_{REF} level, the output of the comparator will be held to V_{DD}, and therefore C_3 command terminal will be high, connected to V_{DD}. In equation (1) we can replace C_A with $C_1 + C_3$ and C_B with C_2, leading to:

$$V_+ = V_{DD} \cdot \frac{C_1 + C_3}{C_1 + C_2 + C_3} \tag{2}$$

For the second case, when voltage V_+ is lower than V_{REF} level, the output of the comparator will be held to ground. At this point C_3 command terminal will be low. In equation (1) we can replace C_A with C_1 and C_B with $C_2 + C_3$, following that:

$$V_+ = V_{DD} \cdot \frac{C_1}{C_1 + C_2 + C_3} \tag{3}$$

If we take into consideration only the comparator itself, the input variable voltage will be V_+, but if we consider the entire voltage monitor application, the input voltage will be the V_{DD} supply voltage (Fig. 3). It follows that we can define the V_{DD} voltage levels at which the output of the comparator changes state as the trip-points V_{trip1} and V_{trip2}. Considering a fixed V_{REF} and starting from (2) and (3), the following equations are developed:

$$V_{trip1} = \frac{C_1 + C_2 + C_3}{C_1 + C_3} \cdot V_{REF} \tag{4}$$

$$V_{trip2} = \frac{C_1 + C_2 + C_3}{C_1} \cdot V_{REF} \tag{5}$$

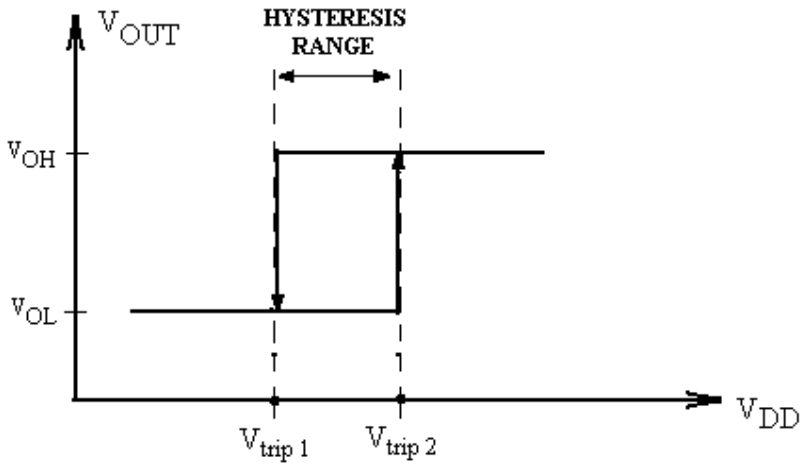

Fig. 3. Transfer Characteristic

The difference between the two V_{trip} levels is the hysteresis associated to the voltage monitor application, V_{HYST}.

From (4) and (5) it results that $V_{trip2} > V_{trip1}$ and that both V_{trip1} and V_{trip2} values depend only on the reference voltage and on the capacitor ratios.

Starting from those stated above, the hysteresis voltage is:

$$V_{HYST} = V_{trip2} - V_{trip1} \tag{6}$$

If we introduce (4) and (5) in (6) the following expression for the hysteresis voltage will be obtained:

$$V_{HYST} = V_{REF} \cdot \frac{(C_1 + C_2 + C_3) \cdot C_3}{(C_1 + C_3) \cdot C_1} \tag{7}$$

Following that, the hysteresis voltage value also depends only on the reference voltage value and on the capacitor ratios. The hysteresis circuit previously detailed is fully described in [7].

3. Implementation of the programmable voltage reference

The proposed voltage reference (Fig. 4) is implemented with a Floating Gate (FG) transistor, by storing a precise charge on the floating gate cell. This reference type is highly programmable both at wafer and package level. The programming of the FG cell consists in applying a predefined electrical signal sequence on the IC pins while also synchronizing the generation of the high voltage used for charge tunneling in the floating gate node [10].

3.1 Floating Gate MOS Transistor

The floating-gate MOS (FGMOS) transistor has a structure similar to a standard MOS transistor, but it is provided with two gates. The command gate can be contacted while the floating gate is completely surrounded by a high quality insulator, silicon dioxide. The silicon dioxide creates a potential barrier that prevents the charge stored on the floating gate from leaking off. Frequent applications for the FGMOS transistors are storage elements for the EPROM and EEPROM memories. However, due to their long-term charge retention, such devices can be used in analog circuits as non-volatile elements for analog trimming [8], [9]. The advantages of the FG cells consist in bi-directional fine trimming (charge can either be added or removed from the floating node), low programming voltages, good charge stability and large trim range.

Programming a FGMOS consists in setting the DC voltage of the floating node to any target value by adding or removing charge from the floating gate. It follows that the FG cell can be assimilated to a MOS transistor that has the gate pre – biased with a known and controlled voltage. The programming process consists in charging and discharging the floating gate by using the flow of electrons onto or off the FG node by means of Fowler-Nordheim tunneling [10]. In this manner, the analog voltage on the floating gate is set, and this voltage controls the operation of the sense transistor.

3.2 Detailed schematic of the programmable voltage reference and comparator for Voltage Monitor

Due to the pre-biased transistor nature of the FGMOS, it is a common approach in the analog circuitry to place the sense transistor (Q1) of the FG cell in a differential pair [11, 12]; for the present application we will consider the reference voltage as input to the branch containing the FGMOS, while the second branch will have its input connected to the external V_{DD} variable voltage (Fig. 4).

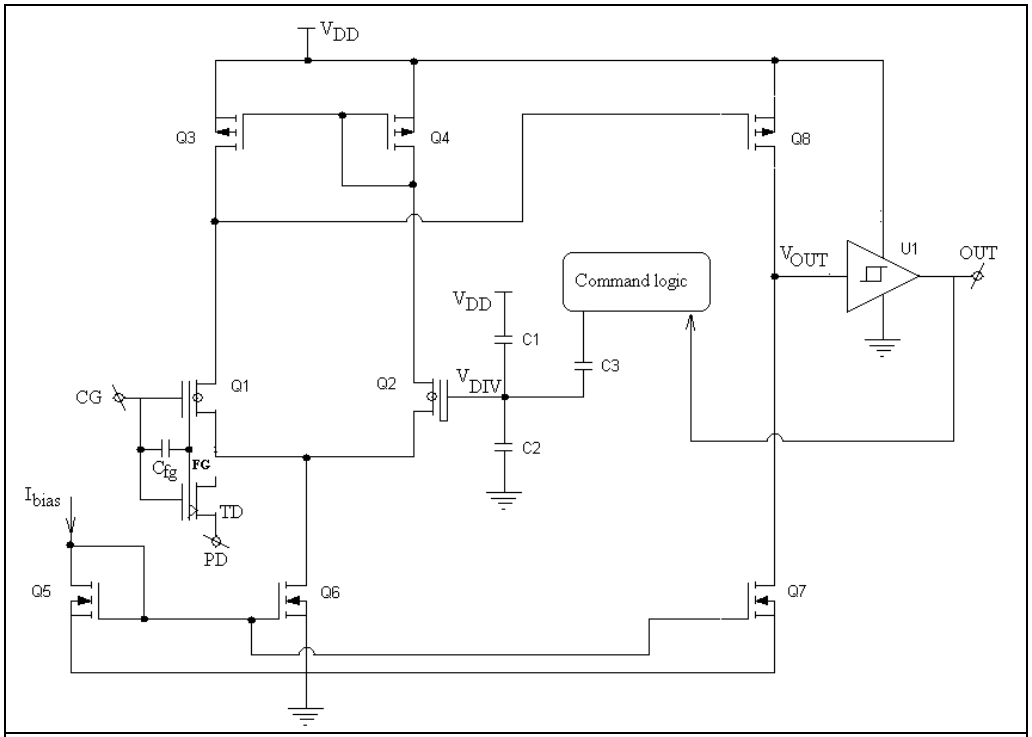

Fig. 4. Detailed schematic of the FG reference and Comparator for V_{DD} Voltage Monitor

The actual programmable voltage reference uses Q1 Floating Gate Cell (FG cell) as sense transistor of the structure. Tunnel diode TD is used during the programming process which involves pins CG (Control Gate) and PD (Program Drain). In normal operation both CG and PD are grounded by means of external, dedicated circuitry. For a good matching, transistor Q2 is identical to Q1 but it has the floating gate shorted to its control gate. The input gate voltage for this transistor, V_{DIV}, is given by the capacitive divider C1 – C2 and by the switch capacitor (C3) hysteresis circuit as shown before.

The biasing is ensured by the Q5, Q6 and Q7 NMOS current mirror. The output stage of the comparator consists in PMOS transistor Q8. Bias current I_{bias} is internally generated by a Widlar current source integrated in the main application.

When the V_{DD} supply voltage is low and V_{DIV} voltage is under the reference voltage set on the Q1 FG cell, the output, V_{OUT}, is 1 logic. When the V_{DD} supply voltage is rising over the trip-point level following that V_{DIV} voltage is over the reference voltage set on the Q1 FG cell, the output of the comparator is 0 logic (Fig. 5). Note that the output voltage associated to the 1 logic state will

follow the supply voltage level which is also the input signal for the voltage monitor application.

For the considered values of the capacitors, the resulting hysteresis values can be calculated with respect to the appropriate reference voltage level.

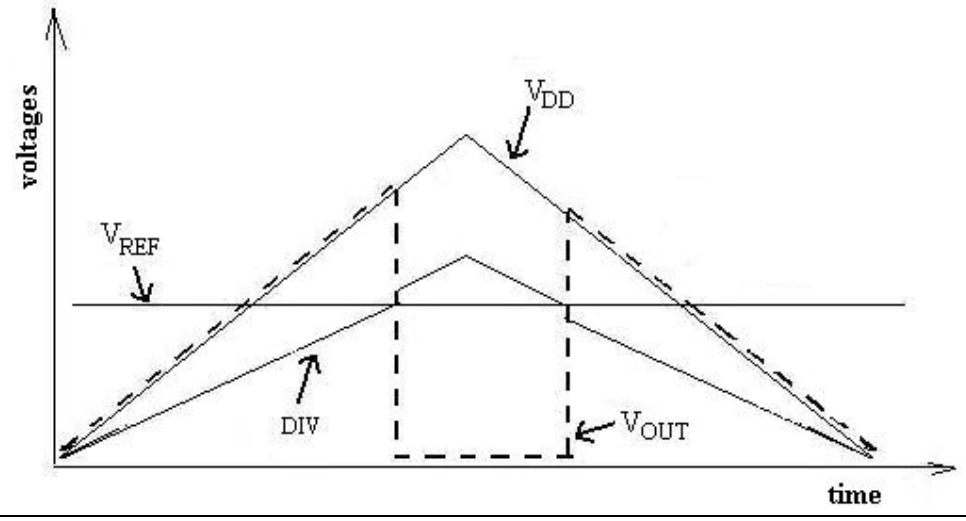

Fig. 5. Comparator input/output waveforms

In Table 1, results using expression (7) with $V_+ = V_{DIV}$ are presented.

Table 1

Calculus results

	Symbol	Value				Unit
Equivalent Application Trip-point	V_{trip1}	0.86	1.15	2	2.9	V
Corresponding FG Node Voltage	V_{REF}	0.563	0.752	1.308	1.897	V
Computed Hysteresis Voltage	V_{HYST}	12.9	17.3	30.0	43.5	mV

The values for the three capacitors were chosen having in mind the targeted hysteresis voltage that is specified in the datasheet and the fact that the minimum FG Node voltage the circuit would exhibit should be high enough to maintain Q1 transistor in saturation. It can be seen in table 1 that the minimum FG Node voltage is 0.56V. This aspect together with the 0.9V minimum supply voltage led us to choose low threshold transistors for both the current mirrors and the differential pair (Q2 and sense transistor Q1) for whom $V_{th} = 0.3V$.

4. Experimental Results

The experimental results consist in both simulation and measurement data on a test structure in 0.5µm technology. The HSpice simulator and a curve tracer for measurements were used for the tests performed on the main integrated voltage monitor application.

Table 2

Simulation results

	V_{trip1}	0.86	1.15	2	2.9	V
	V_{HYST}	14	18	31	44	mV
DATASHEET LIMIT (typ.)	$0.8V < V_{trip1} < 1.5V$	20	20			
	$1.6V < V_{trip1} < 2.4V$			30		
	$2.5V < V_{trip1} < 3.3V$				50	

Table 2 illustrates the hysteresis simulation results, V_{HYST}, obtained for the voltage monitor application. Parameter V_{trip1} is the Voltage Monitor Threshold, as stated in the previous chapters. For each one of its values there is a corresponding internally programmed reference voltage on the FG cell. The simulated response time for the comparator has an average value of 6 µs.

Table 3 contains the measurement results that targeted the hysteresis levels for the voltage monitor application.

Table 3

Measurement results

	V_{trip1}	0.86	1	1.15	2	2.5	2.9	V
	V_{HYST}	17	19	22	37	44	53	mV
DATASHEET LIMIT (typ.)	$0.8V < V_{trip1} < 1.5V$	20	20	20				
	$1.6V < V_{trip1} < 2.4V$				30			
	$2.5V < V_{trip1} < 3.3V$					50	50	

Simulations and measurements were also performed for the supply current on the entire Voltage Monitor application. The case that was considered was the one when the supply voltage is higher than the equivalent trip-point of the application (here: $V_{trip1} = 0.86V$) the RESET output is in its OFF state and the timer for the reset delay is in stand-by. The results are the Stand-by Supply Current values, I_{SB} (simulation – Fig.6, measurement – Fig.7). A maximum of 500nA was obtained in the specified conditions.

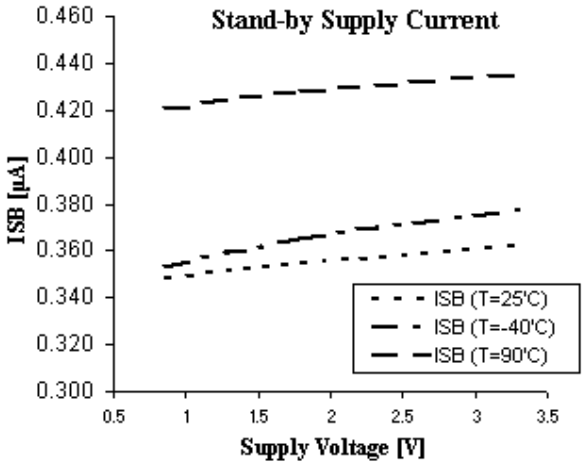

Fig. 6. Supply Current Simulation Results

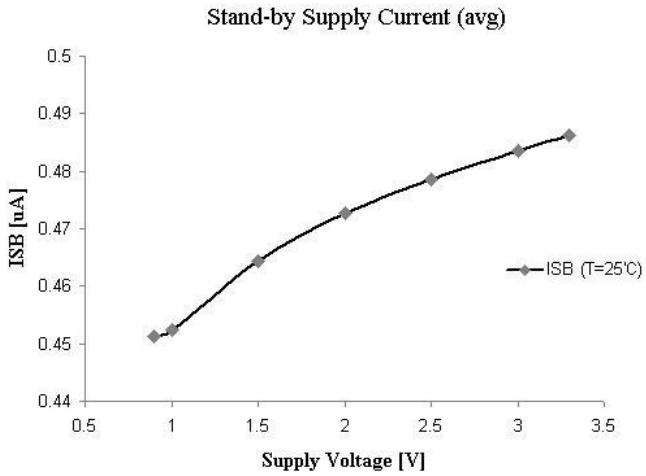

Fig. 7. Supply Current Measurement Results

5. Conclusions

This paper presents the block architecture and the implementation for a programmable voltage reference included in low voltage monitor circuits. Both low supply voltage and current levels were targeted in order to develop a low power integrated circuit suitable for portable applications.

The chosen implementation for the programmable reference was a Floating Gate cell that forms part of the input differential pair of the comparator.

Because of the targeted supply voltage range, the use of low threshold transistors was compulsory. The internal voltage divider that feeds the input signal into the comparator was implemented with a capacitive divider in order to reduce the quiescent current. A switched capacitor schematic for obtaining a hysteresis voltage was added. This schematic is also the object of a US patent application publication [7].

Experimental results, both simulations and measurements, were presented and correlated with the imposed targets. The practical implementation was possible due to the resources gracefully provided by ON Semiconductor.

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