PHASE NOISE AND AREA − POWER CONSUMPTION TRADE-OFF IN THE FREQUENCY SYNTHESIZERS FOR SOFTWARE DEFINED RADIO TRANSCEIVERS

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Lucrarea analizează compromisul dintre zgomotul de fază, aria şi consumul de putere ce defineşte proiectarea sintetizoarelor de frecvenţă utilizate în transiverele reconfigurabile de bandă largă, urmărind identificarea unei arhitecturi optime pentru sintetizatorul de frecvenţă, ţinând cont de particularităţile proiectării de radiofrecvenţă. Lucrarea descrie şi analizează principalele surse de zgomot din circuit şi construieşte un model în baza căruia performanţele de zgomot ale sintetizorului pot fi simulate cunoscându-se contribuţiile individuale ale sub-blocurilor componente. În urma acestei analize, este dezvoltată o nouă arhitectură a sintetizorului de frecvenţă ce implementează două filtre trece jos, unul extern, ce optimizează zgomotul de fază, şi unul intern, de dimensiuni reduse, ce optimizează aria şi consumul de putere.

This paper presents the phase noise and area – power consumption trade-off defining the frequency synthesizers used in Software Defined Radio Transceivers (SDR), focused on finding the optimum frequency synthesizer architecture, given the wide-band RF design specifics. The paper describes and analyses the major noise sources of the circuit and builds a model used is simulating the synthesizer's noise performance. Based on the analysis, a new architecture for the SDR frequency synthesizer is proposed. The proposed synthesizer implements two loop filters: an external one, optimizing the phase noise performance, and an internal one of reduced size, optimizing area and power consumption.

Keywords: Software Defined Radio, frequency synthesizer

1. Introduction

The software driven System on a Chip (SoC) combining a re-configurable RF front-end and a multi-core DSP, as the baseband processor, represents a simplified version of the Software (Defined) Radio (SDR) introduced in [1].

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The block schematic of such a system is depicted in Fig. 1. The common architecture of the SDR RF front-end is the quadrature direct conversion, which implies $f_{LO} \equiv f_{RX}$ and $f_{LO} \equiv f_{TX}$ see Fig. 1, [2].

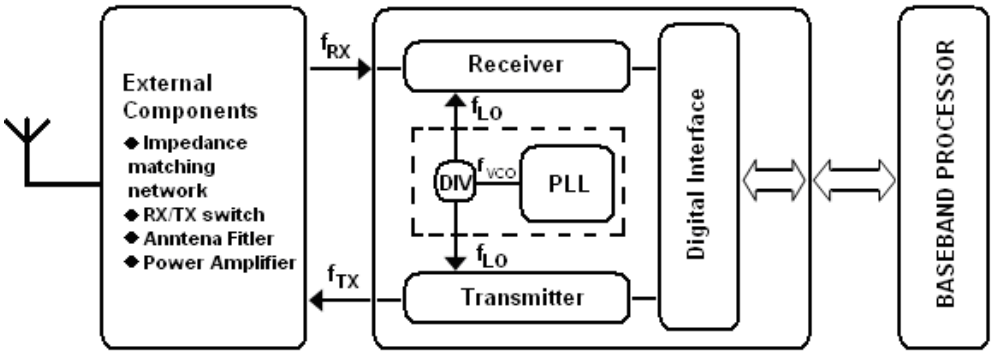


Fig. 1 – Software Re-configurable Radio Transceiver

The three main blocks comprising the SDR Transceiver of Fig. 1 are the frequency synthesizer (SY), the receiver (RX) and the transmitter (TX). The transceiver acts as an analog signal conditioning block. It either prepares the received signal for digital demodulation or it shapes the digitally modulated signal for the wireless transmission.

The digital signal processor (DSP), also known as the baseband processor, represents the digital back-end processing block. The DSP drives the analog front-end via the digital interface. By dynamically changing the transceiver settings, its performance can be adjusted depending on the noise-linearity requirements of the particular transmitted burst can be re-configured on-the-fly.

The task on any wireless receiver is to ensure the analog signal conditioning of the received signal allows its correct digital demodulation. This implies the whole process of down converting the received useful radio signal, from its radio frequency (RF), and its digitalization allows the baseband transmitted data it carries data to be extracted correctly during the digital demodulation.

Oppositely to the RX, the TX chain must ensure the up conversion on the RF frequency of the digitally modulated baseband signal. In the transmitter case the accent is placed on avoiding the disturbance of adjacent radio frequencies. This implies the whole process of up converting the wanted informational signal, from baseband to the RF carrier frequency, dispenses almost all the transmitted energy into the allocated bandwidth.

But, the "heart" of the transceiver is the SY. Its beat is represented by the generation of the local oscillator (LO) signals which drive the receiver, respectively the transmitter chain mixer. Section 2 overviews the typical architecture for the SDR frequency synthesizer. In Section 3 the major noise contributors to the PLL phase noise are revealed and the trade-off between the PLL phase noise performance and its power consumption is presented.

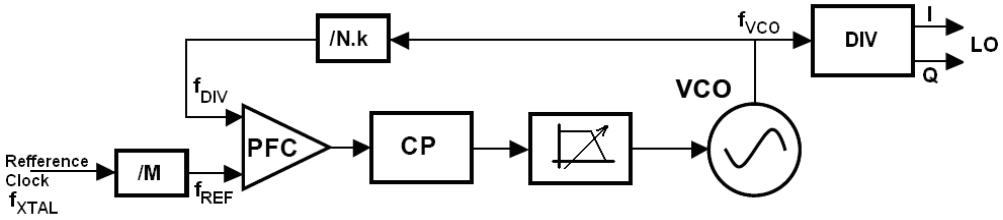


Fig. 2 – Frequency synthesizer block schematic.

Based on this trade-off, an enhanced frequency synthesizer architecture is constructed. Section 0 analyses the PFC-CP duo and describes the best circuit topology option minimizing the PLL jitter. Finally, Section 5 concludes the paper by reviewing the proposed architecture.

2. SDR Frequency Synthesizer Architecture

In Fig. 2 the typical SDR frequency synthesizer block schematic is presented. Basically, the SY is a programmable Phase Locked Loop (PLL) circuit. Given the small channel spacing of various wireless standards, a fractional-N divider is the favored choice for a software reconfigurable radio transceiver, [3]. By tuning the Voltage Controlled Oscillator (VCO) frequency to the appropriate value, the selection of receiving or transmitting channel is realized.

The VCO frequency of the system from Fig. 2, F_{VCO}, is given by

$$F_{VCO} = N.k \times F_{XTAL} / M = N.k \times F_{REF} \tag{1}$$

where F_{XTAL} is the quartz oscillator (XTAL) reference clock frequency, M the F_{REF} division ratio, and $N.k$ the fractional loop divider division factor.

The SDR transceiver of Fig. 1 is a quadrature one. Hence, the frequency synthesizer of Fig. 2 requires at its output a wide-band quadrature frequency generator. To cover the wide frequency range of the modern wireless standards, [3], the best option is to use a Johnson counter, [4]. For such quadrature generators, the VCO frequency must be twice of the desired LO frequency. Considering the case of GSM standard – one of the best example of wireless

standards to suit perfectly an SDR transceiver – available worldwide in 4 frequency bands, [3], the VCO tuning range should span from 3 to 6 GHz, see Table 1. Thus, the frequency synthesizer uses a programmable LO divider circuit (DIV), which structure has been analyzed in [5].

Table 1

VCO Tuning Range and LO Frequency Ranges

VCO Tuning Range	LODIV Division Factor	LO Frequency
3…6 GHz	/2	1.5…3 GHz
3…6 GHz	/4	0.75…1.5 GHz
3…6 GHz	/8	0.375…0.75 GHz

By investigating the VCO topologies, analyzed in depth in [6], it results the only viable solution for a PLL used in mobile wireless application is the LC-VCO. This types of VCOs offer the smallest phase noise amongst the reviewed configurations.

The LC oscillator has also another advantage: given the low values of the integrated spiral inductors that render its high oscillation frequency, it is offering even a lower phase noise if the targeted application uses a carrier located at a frequency lower than half the VCO frequency. Each division by 2 of the LO frequency reduces its phase noise with 6 dB.

The VCO presented in [7] matches the requirements needed for incorporation into a SDR SY. The CMOS LC-VCO, implemented in a 0.13 μm process, covers a frequency range between 3 GHz to 5 GHz, has a sensitivity of 150 MHz/V and its measured phase noise for 4 GHz oscillation frequency is −96 dBc/Hz @ 100 kHz offset, −118 dBc/Hz @ 1 MHz offset and −137 dBc/Hz @ 10 MHz offset.

The PLL reference signal is originating from an on-chip quartz resonator. The monolithic crystal oscillator used in GSM/UMTS applications has an oscillation frequency, f_{XTAL}, of 26 MHz − 96 times the GSM bit rate − and a phase noise of about -140 dBc/Hz @ 1 kHz, a corner frequency lower than 10 kHz and a phase noise floor of -152 dBc/Hz, [8].

In practice, for monolithic PLLs a charge pump is used, because of the more relaxed and efficient implementation, [9]. The PFC-CP duo is analyzed in detail in Section 0.

The Loop Filter optimizes the PLL's noise and transient behavior, by introducing poles and zeroes in the loop's transfer function, and provides additional suppression of the reference frequency harmonics. In order to get a better suppression of the reference frequency harmonics and a faster locking time, a high filter order must be implemented, [10].

The loop filter schematic for a third order charge pump PLL is depicted in Fig. 3.

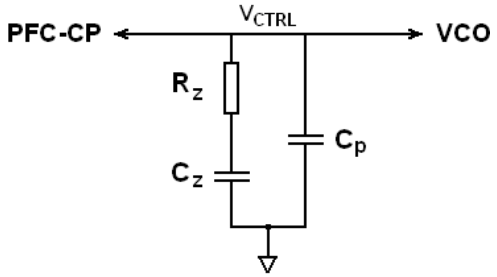


Fig. 3 – Loop Filter for Third Order Charge-Pump PLL.

3. Noise – Power Consumption Trade-Off in Frequency Synthesizers

From the RF design perspective, the main parameter of the PLL circuit is the phase noise, measured in dBc/Hz. The phase noise measures how much of the carrier energy is dispersed around it. During receiving, due to the LO signal noise "tail", the receiver downconverts a fraction of the signals located in the adjacent channels; while transmitting the LO noise tail or other spurious generated by the frequency synthesizer will corrupt the adjacent frequency bands.

The major phase noise contributors to the total PLL output phase noise are the reference clock, the VCO and the loop LPF resistor. The total PLL output phase noise, PN_{PLL}, calculated as a function of the reference signal phase noise, PN_{REF}, the VCO phase noise, PN_{VCO}, and the LPF resistor noise is given by, [10]:

$$PN_{PLL} = PN_{REF} \cdot \left|\frac{1}{1+GH}\right|^2 + PN_{VCO} \cdot \left|\frac{G}{1+GH}\right|^2 + 4kTR_z \cdot \left|\frac{K_{VCO}}{s}\frac{1}{1+GH}\right|^2, \quad (2)$$

where PN_{VCO}, PN_{REF} and PN_{PLL} represent the phase noise spectral density measured in dBc/Hz, G, respectively H, represent the forward loop gain, respectively the feed-back ratio; G and H can be calculated as:

$$\begin{cases} G(s) = K_{PFC-CP} \cdot K_{LPF}(s) \cdot K_{VCO}(s) \\ H = 1/N.k \end{cases}, \quad (3)$$

with $K_{PFC\text{-}CP}=I_{CP}/2\pi$ the PFC-CP gain – I_{CP} the CP current, $K_{LPF}(s)$ the loop filter transfer characteristic and $K_{VCO}(s)=K_{VCO}/s$ the VCO sensitivity.

Equation (2) shows the loop response is low pass type for PN_{REF} and high pass type for PN_{VCO}. The 3-dB cut-off frequency of these characteristics is ω_c, loop cross-over frequency, or the frequency at which the PLL open loop gain has a magnitude equal to one. The loop rejects PN_{VCO} for small frequency offsets around the center oscillation frequency, where $GH >> 1$, as opposed to

amplifying PN_{REF} by N^2. For frequency larger than ω_c, the loop suppressing action towards PN_{VCO} fades-out and increases towards the XTAL phase noise with a slope of 20 dB/dec, as $GH << 1$. The noise originating from R_z when transferred at the PLL output is of band-pass type; as it is filtered both at low frequencies, due to the VCO pole in the origin, and at frequencies larger than ω_c.

In practice, for mobile wireless applications the out of band noise performance is more important due to the large level of the blockers and interferers, on the RX side, or due to the stringent output spectral mask, on the TX side, [3]. Hence, the common value of ω_c is the order of 100 kHz. This value trades off the XTAL noise reference contribution, amplified by $N.k^2$ by the loop, with the good phase noise performance of LC-VCOs at carrier offsets larger than 1 MHz, [6].

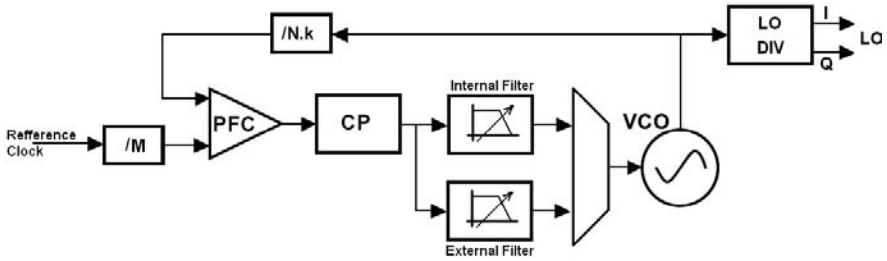


Fig. 4 – Frequency Synthesizer Embedding Power Consumption - Noise Trade-Off

The loop cross-over frequency, ω_c, for a PLL implementing the LPF from Fig. 3 can be calculated as:

$$\omega_c = \frac{K_{PFC-CP} \cdot K_{VCO}}{N.k} \cdot \frac{R_z C_z}{C_p + C_z} \tag{4}$$

The values of the loop filter components are dimensioned to ensure the Fig. 2 PLL stability, [11]. This constraint translates to the following equations:

$$\begin{cases} R_z = 10 \cdot N.k \cdot \omega_c / 9 \cdot K_{PFC-CP} \cdot K_{VCO} \\ C_z = 5 / \xi^2 \cdot R_z \cdot \omega_c \\ C_p = C_z / 9 \end{cases} \tag{5}$$

where $\xi = 0.707$ for a phase margin of 45°.

The loop filter components, sized by eqs. (5), have been calculated in the assumption the loop LPF pole frequency is 10 times larger the its zero frequency.

To maintain a low phase noise specification required by the long range wireless standards (e. g. GSM/UMTS requires −116 dBc/Hz @ 600 kHz offset, [12]) a low value for R_z is required. This will render large values for the filter's

capacitors, making the LPF integration pricey. While for short range wireless standards a much larger filter resistor can be implemented, as the phase noise requirement is relaxed with almost 12 dB (e. g. W-LAN requires −110 dBc/Hz @ 1 MHz offset, [13]).

Hence, the area – noise trade-off will be realized by enhancing the synthesizer architecture, as shown in Fig. 4. For a low phase noise output spectrum an external filter, implementing low resistor values, will be used.

Also, at each PFC comparison the charge pump drives a current equal to I_{CP} to the loop filter impedance. This triggers a VCO frequency jump equal to:

$$\Delta f = K_{VCO} \cdot \Delta V_{LPF} = K_{VCO} \cdot I_{CP} R_Z \tag{6}$$

In order to maintain the loop locking time for low values of R_z, the instantaneous voltage jump on the VCO control node must have the same value as for large R_z. This is achieved by increasing the charge pump current.

In this way, the loop phase margin is also kept constant. When low noise performance is not required, the internal filter is switched at the multiplexer output, thus reducing the charge pump current requirements and, subsequently, reduces the PLL power consumption.

Fig. 5.a presents the simulated PLL phase noise for 3 values of the charge pump current. The PLL phase noise has been calculated using eq. (2). The XTAL and VCO phase noise contributions were the ones presented in Section 2, while the LPF components have been calculated using eq. (5), considering a phase margin of 45° − worse case for stability. The VCO is assumed to oscillate at 4 GHz driven by a 26 MHz XTAL reference; this $N.k = 153.84$.

As I_{CP} increases from 100 μA to 10 mA, R_z is decreased from 34 kΩ to 340 Ω, while C_Z, respectively C_p, are increased from 0.24 nF to 24 nF, respectively from 26 pF to 2.6 nF to maintain a constant ω_c of 100 kHz. As a result, the phase noise contribution of the loop LPF resistor is reduced.

The PLL phase noise peak at 100 kHz offset is decreasing from -99.6 dBc/Hz to -106.2 dBc/Hz. The latter value corresponds to a 3 dB higher value than of the in-band noise floor equal to -109.2 dBc/Hz, matching the characteristic of higher order systems exhibiting a phase margin of 45°.

In order to assess the optimal internal and external filter sizing, the loop phase noise has been evaluated using eq. (2).

Fig. 5.b plots the PLL phase noise @ 600 kHz offset, respectively @ 600 kHz offset, versus I_{CP} at the LODIV output set to divide by 2 the 4.8 GHz VCO signal.

Based on the Fig. 5.b plot the internal and external filter components are sized. To meet the W-LAN, respectively the GSM/UMTS, phase noise specifications the internal loop filter is driven by $I_{CP} = 0.1$ mA, respectively the

external LPF requires I_{CP} = 1 mA. The corresponding filter components values are noted on Fig. 5.b.

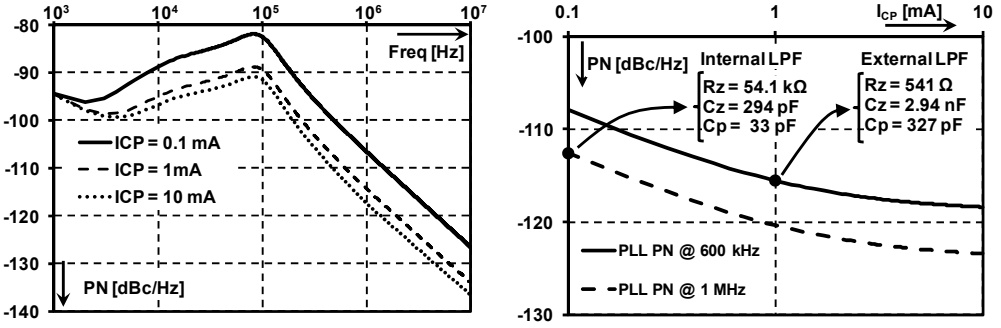


Fig. 5 – a. PLL Phase Noise (at VCO Output) vs. ICP;
b. PLL Phase Noise (at LODIV Output) vs. ICP

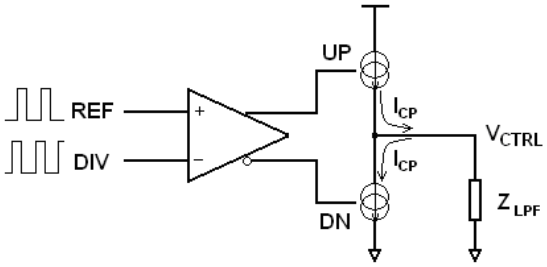


Fig. 6 – PFC-CP Operating Principle.

4. The Phase Frequency Comparator (PFC) and Charge Pump (CP)

The main requirements of the wide-band frequency synthesizer PFC-CP duo are to ensure a linear transfer characteristic and maintaining the large PLL frequency locking range. As shown in Fig. 6 the PFC has as inputs the reference clock signal, *REF*, and the divided VCO signal, *DIV*. The simplest Phase Detectors (PD) are the XOR gate, the S-R or J-K flip-flops. These PDs has a major disadvantage: the loop succeed to lock only if the VCO oscillation frequency is close to the wanted frequency, given by equation (1), [13]. To ensure loop locking even when the VCO starts oscillating at a frequency far off than the desired PLL output frequency, a more complex circuit called Phase Frequency Detector or Comparator has to be used. Basically, the PFC is a sequential PD controlled by a finite state machine. In this way, due to the Finite State Machine memory function, additional information is provided about the frequency offset between the two PFC input signals when the loop is not locked.

The operating principle of the PFC-CP (CP: Charge Pump) duo is presented in Fig. 6. The PFC analyses the time difference between two consecutive rising or falling edges of *REF* and *DIV* and provide then the control signals, *UP* and *DN*, for the CP current sources that regulate the voltage on the loop filters impedance. In practice, the PFC plus CP combination sets the VCO control voltage.

When the *UP* signal is high, the upper charge pump current is activated and I_{CP} is bleed into the loop's filter impedance. Hence, the oscillator control voltage, V_{CTRL}, is increased, rendering an increase or a decrease of its oscillation frequency, depending on its practical implementation. On the other hand, when the *DN* signal is high, the lower charge pump current sinks I_{CP} and V_{CTRL} is decreased. When the loop is locked both *UP* and *DN* signals will be low. In this way, the CP current sources will be off and its output will be in a high impedance state. Hence, ideally the VCO control voltage remains unchanged, maintaining the VCO oscillation frequency.

Table 2 summarizes the three possible states for the PFC, while Fig. 7.a shows the principle schematic of such PFC.

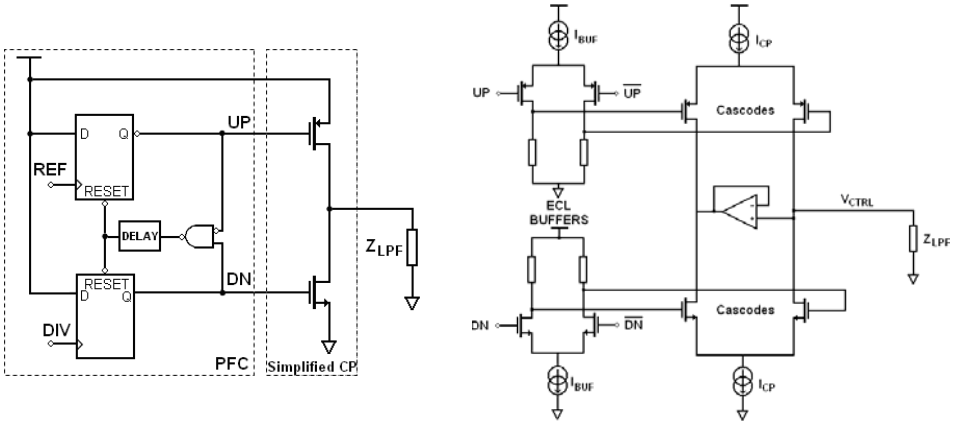
Table 2

PFC Operation

PFC input	PFC Output	CP State	V_{CTRL}
REF before DIV	UP = H (L) and DN = L (H)	Pump-Up (Down)	$V_{CTRL} \uparrow (\downarrow)$
REF after DIV	UP = L (H) and DN = H (L)	Pump-Down (Up)	$V_{CTRL} \downarrow (\uparrow)$
REF in sync with DIV (Locked Loop)	UP = L and DN = L	Hi-Z	$V_{CTRL} \leftrightarrow$

The delay block in Fig. 7.a alleviate the major PFC-CP duo problem: the cross-over distortion. This condition occurs when the loop is locked, as due to parasitic elements some of the charge stored on the loop filter capacitors will be lost. The VCO oscillation frequency is altered and the loop translates it to a small phase offset between the two PFC input signals. Given the PFC-CP finite time response, this phase offset will have no impact on the CP output. So, if no delay block were to be present, the PFC characteristic exhibits a dead-zone near zero phase offsets. This renders a situation incompatible with a low phase noise requirement, since the uncorrected offset corresponds to an equivalent PLL output jitter.

But, the delay block makes the *UP* and *DN* signals active for the minimum amount of time required for the PFD-CP to counter this un-wanted effect. The minimum *UP* and *DN* pulse width, hence the delay, should be larger than the propagation delays through the PFC logic plus the time required operating the CP switches. Thus, the same current will be pumped-in and, in the same time, will be pumped-out from the loop filter impedance, ensuring the PFC characteristic will be much closer to the linearity of an ideal one.



a. b.

Fig. 7 – a. Phase Frequency Comparator Implementation
b. Charge Pump Principle Schematic

Since, the same charge is injected into, respectively, extracted from the loop filter impedance, the operations will have no effect on the loop looking state, while the PLL phase noise performance is improved.

Given the PFC transfer characteristic dead-zone cancellation, the linear operation is now limited by the charge pump performance. The charge pump circuit implementation must ensure linear operation within its output voltage swing.

The principle schematic of such a circuit is depicted in Fig. 7.b. A differential CP was chosen to improve the linear operation. In addition, both CP current sources switches are implemented as cascodes. For optimal cascodes performance the switches are not driven directly by *UP* and *DN*, as they are digital controls varying between the supplies. To limit the *UP* and *DN* signals voltage swing, two source coupled buffers are used, as shown in the left part of Fig. 7.b.

There is one additional problem with the PFC-CP combination when the loop is locked: even if *UP* and *DN* signals are active simultaneously for the same short period of time, the charge injected into the loop's filter by the upper CP current source is not equal to the charge removed from the loop's filter by the lower CP current source. This issue resides with the inherent process variation of the CP transistors and translates to additional phase noise at the PLL output as well as higher reference frequency harmonics feed-through. So, if the phase noise performance is to be improved even more, the PFC concept must be further enhanced. Calibration of the charge pump current sources is required. [14]

5. Conclusion

This paper presented an overview of the frequency synthesizer architecture used in multi-standard re-configurable wide-band transceivers: the fractional-N frequency synthesizer based on a high oscillation frequency, wide-band frequency range, LC VCO, that guarantee best phase noise performance, while maintaining a fast locking time.

The main PLL phase noise contributors have been analyzed and a noise model was build to assess their influence on the total PLL phase noise. Based on the simulation results of the model, a new frequency synthesizer architecture was proposed. The new synthesizer architecture is implementing two loop filters: an external one, optimizing the phase noise performance (e. g. for GSM compatibility), and an internal one of reduced size, optimizing area and power consumption (e. g. for W-LAN compatibility). The external loop filter incorporates approximately 2.35 nF, and requires a CP current of 1 mA; while the internal filter integrates 10 times less capacitance and less CP drive, or equivalently 235 pF and 100 μA.

Finally, the PFC-CP duo topology has been analyzed. By implementing a PFC with dead-zone cancelation the synthesizer phase noise is reduced.

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