OPTIMIZED DRIE PROCESS FOR TAPERED WALLS THROUGH WAFER VIA HOLES MANUFACTURING

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Lucrarea prezintă o metodă nouă de realizare a unor treceri prin plachetele de siliciu cu pereți înclinați, utilizând un proces de corodare uscată de tip DRIE (Deep Reactive Ion Etching) cu izotropie variabilă.

Sunt prezentate principiul de realizare a trecerilor (bazat pe utilizarea unei corodări anisotrope de tip Bosch) şi optimizarea procesului pentru obținerea unui control bun al unghiurilor de înclinare a pereților.

This paper presents a new method of tapered walls through silicon wafers via holes (TSV) manufacturing, using a variable isotropy DRIE (Deep Reactive Ion Etching) process type.

TSV manufacturing method is presented (based on Bosch type anisotropic etching), as well as process optimization for a very good control over the wall angles.

Keywords: DRIE, TSV, variable isotropy

1. Introduction

Last generations of mobile phones or multifunctional computers were achieved due to the availability of technology development. One important aspect in recent years was the increasing of integration level, mainly by miniaturization through the LSI (Large Scale Integration) processes providing very small dimensions. Because in plane miniaturization it is close to arrive to its technological limits, tridimensional technology can offer a new breakthrough enabling to increase the integration density.

Conductive through silicon via's (TSV's) are the key component for electrical connections in stacking devices - replacing wire bonding with TSV's, it is possible to save the space that would be necessary for bonding wires and to reduce connections lengths [1].

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Two aspects should be solved during TSV's fabrication: through wafer via (TWV) manufacturing and holes filling with a conductive layer.

TWV were manufactured in last 20 years using different techniques - wet etching, powder blasting, laser processing or plasma etching, each with advantages and disadvantages in terms of aspect ratio, wall roughness, minimum size or positioning accuracy [2]. Due to the very good performances (aspect ratio higher than 20:1, positioning accuracy provided by photolithography, minimum size or roughness), DRIE began to be the main technique used in recent years.

Copper and doped polysilicon are commonly used as conductive materials for via holes filling due to the deposition features of these materials: electrochemical deposition for copper (with a much higher deposition rate in narrow areas) and LPCVD for polysilicon (very good coverage of the walls due to the conformal deposition) [3-5]. Unfortunately, due to the contamination problem is not easy to implement copper electroplating technology anywhere, while for high frequencies applications doped polysilicon cannot be used due to the large resistivity.

Although problems of adhesion, diffusion or holes filling were not fully resolved, gold was also used as conductive material [6-7].

Our aim was to develop a new type of conductive TSV using gold, allow depositing a barrier layer – Cr or Ti – on the walls.

In this paper a new process of tapered walls TSV manufacturing is described. A variable isotropy process was developed in order to obtain a very good control of the walls angles, based on alternatively using of anisotropic Bosch type process and isotropic etchings. After optimization, process showed a very good agreement with designed via's – deviation smaller than 10% were obtained.

2. TSV manufacturing method

Among other advantages offered by DRIE techniques, the ability to change the isotropy during processing allow manufacturing of structures which cannot be obtained using other techniques [8].

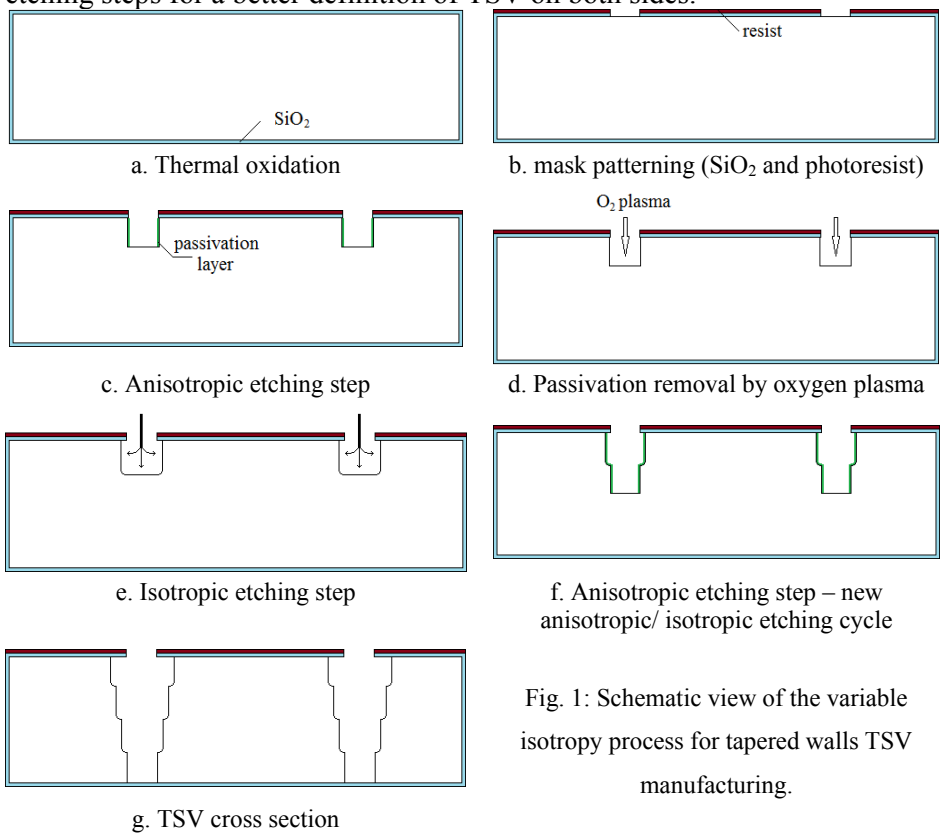
This unique feature can be exploited for tapered walls TSV, using isotropic etchings steps for a controlled enlargement of the via's.

The proposed method consist in alternatively using of anisotropic and isotropic etchings to achieve the required depth and to enlarge the holes on the top side of the wafer; during anisotropic etchings, due to the process directivity, silicon will be removed just in the vertical direction, while during isotropic steps etchings will act on all surfaces of the walls.

Anisotropic etching steps are based on the Bosch type process, consisting of etching and passivation of the walls sequences to achieve large rates etching and anisotropies. To enable etching of the entire walls surface during isotropic

steps, the passivation layer deposited during anisotropic steps must be removed first - this can be done using oxygen plasma before each isotropic etching step.

The technological flow is presented in figure 1. Manufacturing process starts with thermal oxidation, photoresist deposition and patterning, followed by SiO_2 etching from the via windows – figure 1 a and b. Both SiO2 and photoresist layers are used as masks during DRIE process, only one of them not being enough for TSV manufacturing. More than this, because photoresist is easily removed by oxygen plasma, SiO_2 layer thickness should be chosen as function of etching cycles number. DRIE processing (figure 1 c-g) starts and ends with anisotropic etching steps for a better definition of TSV on both sides.



a. Thermal oxidation

b. mask patterning (SiO_2 and photoresist)

c. Anisotropic etching step

d. Passivation removal by oxygen plasma

e. Isotropic etching step

f. Anisotropic etching step – new anisotropic/ isotropic etching cycle

g. TSV cross section

Fig. 1: Schematic view of the variable isotropy process for tapered walls TSV manufacturing.

One problem of DRIE processes is ARDE effect (Aspect Ratio Dependent Effect) – etching rate is strongly influenced by window area through which the etching is performed, significantly decreasing with surface; due to this effect is almost impossible to use different small size of the windows during the same process run. To estimate this effect, the process was performed and optimized for two different circular windows, having 20µm and 100µm diameter.

The second problem to achieve our purpose comes from the roughness of the wall after processing – depending of etching rate, Bosch type processes produce a specific roughness of the walls (scalloping) which can be up to 1µm. To reduce walls roughness different anisotropic etching recipes were used.

3. Experimental results and process optimization

First step in TSV manufacturing consist in etching rates finding for the specific windows used. Silicon wafers (<100> oriented, 200µm thick) and 100µm diameter circular masks were used for TSV manufacturing.

300nm thermal silicon oxide layer was grown on the wafers and a 10µm thick photoresist was used for etching windows patterning.

Two processes, with a different number of steps, were used in this stage, for a easier characterization: first one had three steps of anisotropic etching and two of isotropic etching (two etching cycles), while the second one had five steps of anisotropic etching and four of isotropic etching (four etching cycles) [9].

A high etching rate recipe (more than 10µm/min) was used for anisotropic etching steps.

Measurements performed on the manufactured structures (figure 2) showed etching depths of ~104µm in 6min for the process with two etching cycles, while for the process with four etching cycles etching depth of each anisotropic step was ~52µm in 3 min, leading in both cases to an etching rate of 17.33µm/min.

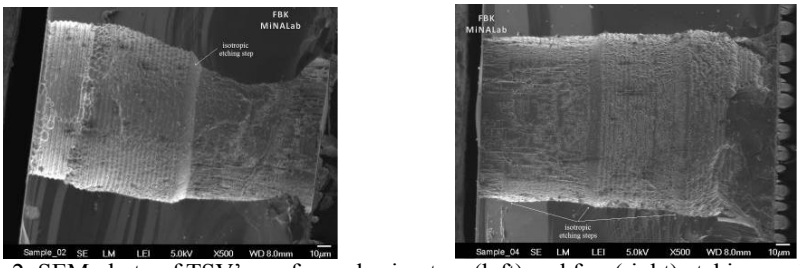


Fig. 2: SEM photo of TSV's performed using two (left) and four(right) etching cycles.

Regarding the isotropic etching steps, due to the much bigger anisotropic etching rates than the considered ones (almost double), can be seen just one isotropic etching step for the first process type and three for the second one (instead two and four respectively). Measurements performed showed an etching rate of about 2µm/min for this process type.

In fig 2 we can see the specific scalloping obtained after Bosch type anisotropic etching, providing a roughness of about 1µm.

One method to reduce walls roughness was to modify the anisotropic etching recipe: using lower gas flow and power it is possible to obtain smoother

walls, although in this way etching rates will decrease. Also, when bigger angles are needed (in first experiments obtained angles were between 1.8° and 2.9°; walls angles are computed considering top and bottom size of the TSV), isotropic etching acts to reduce the roughness, having a polishing effect.

In the next step two different anisotropic etching recipes were used, the first one providing a roughness of about 500nm, the second with a roughness lower than 100nm.

During this optimization step 500µm thick silicon wafers were used and mask with both 20µm and 100µm windows diameter on the same wafer; the aim was to obtain 100µm diameter holes with a 200µm depths, using variable isotropy process with 4 etching cycles. In addition to roughness reduction, other targets for this stage were to find exactly etching rates for these processes and to estimate the ARDE effect for these two windows dimensions.

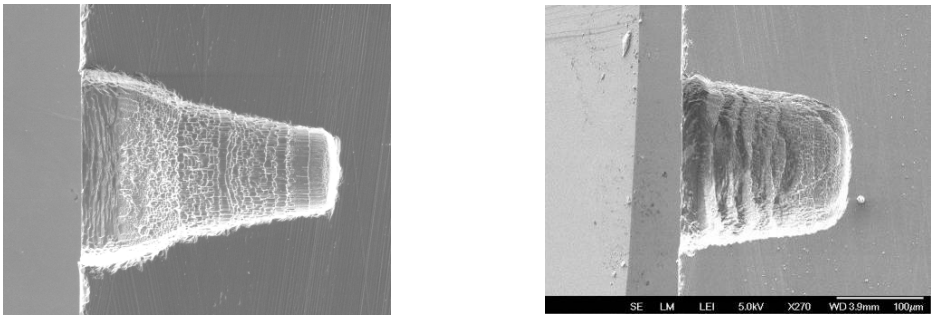


Fig. 3: SEM photos of the holes performed in 500µm silicon wafers using a variable isotropy process and anisotropic etching recipe with medium roughness, having 20µm (left) and 100µm (right) diameters.

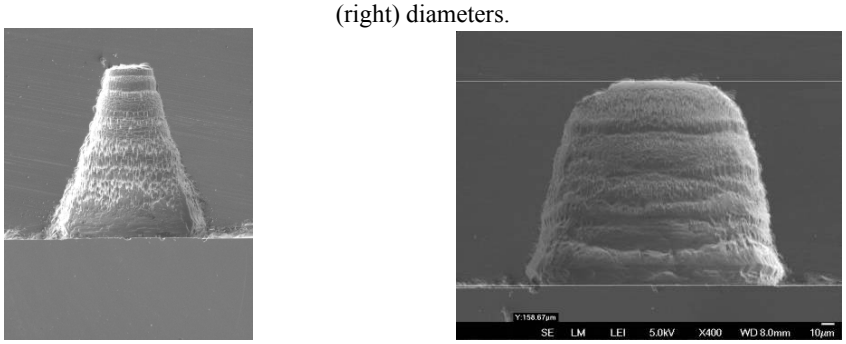


Fig. 4: SEM photos of the holes performed using a four cycles variable isotropy process with a low roughness anisotropic etching recipe, with 20µm (left) and 100µm (right) diameters.

Results obtained are presented in figures 3 for the recipe with a medium roughness and in figure 4 for the recipe with low roughness.

In all SEM photos can be seen a strong improvement of the walls roughness, but also the appearance of some nanometer peaks on the walls - mainly on 20µm diameter holes.

Measurements performed on the manufactured holes by medium roughness recipe showed a depth of about 195µm for 100µm diameter, while for the 20µm diameter depth obtained was of about 128µm. Using the recipe providing low roughness etching rates were smaller, obtaining a depth of about 159µm for 100µm diameter holes and 109µm for 20µm diameter. Both recipes provides a etching rates dropping of about 33% for the smaller holes diameter respect to the bigger ones due to the ARDE effect.

A very close ratio was obtained also regarding the isotropic etching rates: 45÷50µm lateral etching for 100µm diameter holes and 30÷35µm for 20µm diameter ones. A strong attenuation of the isotropic etchings was observed which should be taken into consideration in the final step – the process was designed to obtain wall angles of 21.8°, but angles obtained were between 14° and 18° (for 100µm diameter holes, lateral etching was between 45µm and 50µm instead of 80µm as was designed).

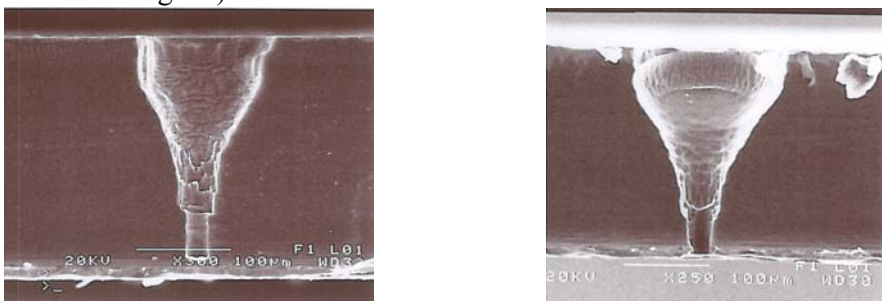


Fig. 5: TSV manufactured on 300µm thick silicon wafers using 20µm diameter masks; obtained wall angles: 10.3° (left) and 15.2° (right).

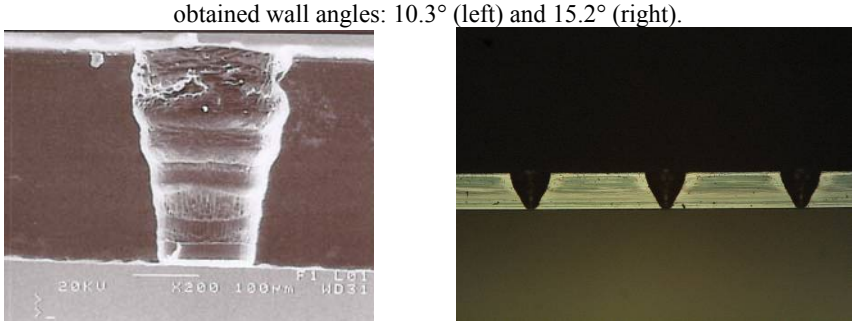


Fig. 6: SEM photos of the manufactured TSV on 300µm thick silicon wafers using 100µm diameter masks with wall angles of 10.7° (left) and 21.2° (right).

Optimized process was implemented on 300µm thick silicon wafers using a six etching cycles process; both etching windows dimensions (20µm and 100µm) were used for TSV manufacturing. For this last step target was to obtain both 11.3° and 21.8° walls angles, with lateral etching around the mask of 60µm and 120µm respectively. Results obtained are presented in figures 5 (for 20µm mask diameter) and 6 (for 100µm diameter).

Measurements performed (table 1) show in almost all cases an enlargement very close to the expected ones: 54.5μm to 56μm instead 60μm for 11.3° angles, while for 21.8° lateral etching was of about 115μm instead 120μm (for 100μm diameter mask). These data lead to errors smaller than 10% - between 9.17% (for 20μm diameter and 11.3° wall angle) and 6.67% (obtained for 100μm diameter and 21.8° wall angle). Strong reduction of the etching rate of isotropic processes can be seen in the much smaller enlargement obtained for 20μm diameter TSV: 81.5μm instead 120μm. Also, cross section of the 20μm diameter TSV's (figure 5) show the modification of the slope due to the changes of the etching rate with depth.

Table 1

Measurements of the manufactured TWV after process optimization

	Mask diameter			
Parameter	20μm		100μm	
Target angle (lateral etching)	11.3° (60μm)	21.8° (120μm)	11.3° (60μm)	21.8° (120μm)
Bottom size	~25μm	~27μm	~140μm	~100μm
Top size	~134μm	~190μm	~252μm	~330μm
Lateral etching	~54.5μm	~81.5μm	~56μm	~115μm
Measured angle	~10.3°	~15.2°	~10.57°	~20.97°

Computed angles, based on the measured data, were close to the wanted ones in three of four cases: 10.3° and 10.57° instead 11.3° and 20.97° instead 21.8°.

4. Conclusions

A new process for TSV was developed, consisting in alternated using of anisotropic and isotropic etching steps. This process was optimized for two different via sizes (20μm and 100μm) on 300μm thick silicon wafers. Optimization shows the possibility to obtain very small errors - in almost all cases errors were smaller than 10%.

The advantages of this process type reside in a very good control of the walls angles with possibility of barrier and seed layer deposition, thereby improving the adhesion and reducing the diffusion. Also, it can be easily implemented on other kind of DRIE equipments without the need for a long time and significant resources.

Comparing with others TSVs manufacturing techniques recently reported [1, 10-14], we can see the benefits of this technology in thick wafer processing or possibility of manufacturing tapered walls TSVs with a very good control of the angles and a short process optimization; also, the aspect ratio of the manufactured TSVs allow to obtain a minimum dimension of the same magnitude with that reported in the literature.

Acknowledgements

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