RAIL-TO-RAIL AMPLIFIER STRUCTURES

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Această lucrare prezintă: (1) *o trecere în revistă comparativă a trei topologii tipce pentru etajele de intrare CMOS "rail-to-rail" (RRIS): un etaj simplu, un etaj cu transconductanță constantă şi un etaj care funcționează în regim de inversie slabă,* (2) *implementarea etajului de sumare şi* (3) *influența celor trei topologii asupra etajului de sumare. Circuitele prezentate sunt implementate într-o tehnologie CMOS standard de* 0.8 *μm. Performanțele etajelor au fost determinate prin analiză manuală iar rezultatele au fost verificate prin simulare SPICE*

This paper presents (1) *a comparative overview for three widely used CMOS rail-to-rail input stage (RRIS) topologies: a simple stage, a constant transconductance stage, and a weak inversion RRIS stage,* (2) *the summing stage implementation, and* (3) *the three RRIS topologies influence on the summing stage. The described circuits have been implemented in a standard* 0.8 *μm CMOS process. The stages performances were determined by means of manual analysis and the results were checked by SPICE analysis.*

Keywords – rail-to-rail input stage, constant transconductance, output resistance.

Introduction

There is a significant interest for low voltage and low power circuits in today IC design. The circuit supply voltage has to be fully used as the supply voltages becomes smaller and smaller. To this purpose, rail-to-rail (RR) gain stages were developed, [1, 2]. This paper present three different rail-to-rail input stage (RRIS) topologies: the standard one, a constant total transconductance RRIS topology implemented using a Zener diode and a weak inversion constant transconductance RRIS. Manual analysis is used to evaluate the transconductance variation versus common-mode input voltage, the total current consumption and output resistance for all three RRIS topologies.

1. The Standard Active Load Input Stage

Firstly, we consider the common mode range of an active load *p* channel transistors differential pair. Based on the minimal voltage drops needed to keep

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each transistor in the active region (see Fig. 1) we get the minimum and maximum common mode input voltage values ($V_{CM,\,min}$ and, respectively, $V_{CM,\,max}$):

$$V_{CM,\max} = V_{dd} - \left|V_{Tp}\right| - V_{ov1} - V_{ov5} \tag{1}$$

$$V_{CM,\min} = -V_{ss} + V_{Tn} - \left|V_{Tp}\right| + V_{\mathrm{ov}3} \tag{2}$$

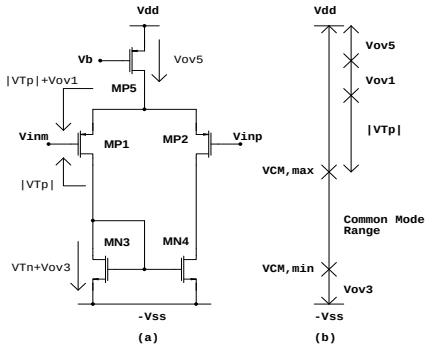

Fig. 1 (a) The standard differential stage and (b) its common mode input voltage range.

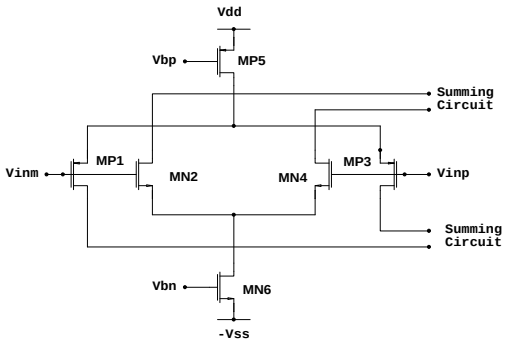

Fig. 2 Basic rail-to-rail input stage

The $V_{CM,min}$ value is limited by the voltage drop needed on the diode connected MN3 transistor and can be reduced to $-V_{SS}$.

Taking into account the typical absolute values of both the threshold voltage (about 0.8…1 V) and of the overdrive voltage (about 0.2 V) we get:

$$V_{dd} - V_{CM,\max} = V_T + 2V_{\mathrm{ov}} \cong 1.2\ \mathrm{V} \tag{3}$$

$$V_{CM,\min} + V_{ss} = V_{\mathrm{ov}} \cong 0.2\ \mathrm{V} \tag{4}$$

(the $V_{dd}-V_{CM,\max}$ and $V_{ss}+V_{CM,\min}$ show how close to the power supply rails is the input common mode voltage swing).

The active load differential stage common mode input voltage range is significantly smaller than the supply voltage range. If, for example, we consider a (relatively large) power supply of $3.3\ \mathrm{V} \pm 10\%$ we get the worst case $V_{CM,\min}$=0.2 V and $V_{CM,\max}$=1.8 V. From the 3.3 V supply voltage, we can use only $V_{CM,\max}-V_{CM,\min}$=1.6 V. This justifies the need for rail-to-rail input stages.

2. The Standard Rail-to-Rail Input Stage

The p channel differential pair common mode input voltage can reach the negative rail, $-V_{SS}$ and has an upper limit of $V_{DD}-|V_{Tp}|-2V_{\rm ov}$. Similarly, the n channel differential pair can operate between $-V_{SS}+V_{Tn}+2V_{\rm ov}$ and V_{DD}.

The basic principle of a rail-to-rail input stage (RRIS) is to use both an n channel and a p channel differential pair (see Fig. 2). The two differential pairs have the inputs connected together and their output currents are sent to a summing circuit, [1, 2]. By design, the differential pairs have the same transconductances, $g_{m1}=g_{m2}=g_m$ given by [2, 3]

$$g_{m1,2}=2I_{D1,2}/V_{ov1,2}=\sqrt{2K_{1,2}\,I_{D1,2}}=K\,V_{ov1,2} \tag{5}$$

We shall refer to the stage in Fig. 2 as the simple rail-to-rail input stage (S-RRIS). Let's take a common mode input voltage, V_{CM}, varying from $-V_{SS}$ to V_{DD}:

- For $-V_{SS}< V_{CM} < -V_{SS}+V_{Tn}$ the n channel differential pair is off, so $g_{m2}=0$. This forces MN6 to work in deep linear region, with $V_{ds}=0$. The p channel differential pair gives the total stage transconductance $g_{m,\rm tot}=g_{m1}=g_m$;
- For $-V_{SS}+V_{Tn} < V_{CM} < -V_{SS}+V_T+V_{\rm ov}+V_{\rm ov6}$ the n channel differential pair opens gradually and g_{m2} varies from 0 to g_m. The p differential pair is on, so $g_{m1}=g_m$. It results that $g_{m,\rm tot}$ varies from $g_{\rm m}$ to $2g_m$;
- For $-V_{SS}+V_{Tn}+V_{\rm ov}+V_{\rm ov6} < V_{CM} < V_{DD}-V_{Tp}-V_{\rm ov}-V_{\rm ov5}$ both differential pairs are on and the stage total transconductance is $g_{m,tot}= 2g_m$;
- For $V_{DD}-V_{Tp}-V_{\rm ov}-V_{\rm ov5} < V_{CM} < V_{DD}-V_{Tp}$ the p differential pair turns off and $g_{m,tot}$ varies from $2g_m$ to g_m;
- For $V_{DD}-V_{Tp} < V_{CM} < V_{DD}$ the p channel differential pair is cut off and the $g_{m,tot}$ is given only by the n channel differential pair, $g_{m,tot}=g_{m2}=g_m$.

This basic analysis provides us with the V_{CM} threshold voltages, corresponding to the transitions between operating states:

$$V_{CM}^{nL}=-V_{ss}+V_{Tp} \qquad V_{CM}^{nU}=-V_{ss}+V_{Tn}+V_{\rm ov}+V_{\rm ov6} \tag{6}$$

$$V_{CM}^{pL}=V_{dd}-\left|V_{Tp}\right|-V_{\rm ov}+V_{\rm ov5} \qquad V_{CM}^{pL}=V_{dd}-\left|V_{Tp}\right| \tag{7}$$

Fig. 3 presents the stage total transconductance, $g_{m,tot}$, versus V_{CM}.

We are also interested in the differential pair drain currents, as they affect the output stage resistance. Fig. 4 presents I_{D1} and I_{D2} currents versus V_{CM}.

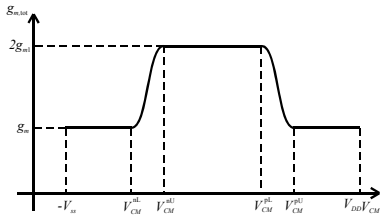

Fig. 3 S-RRIS total g_m variation

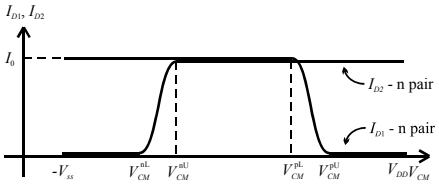

Fig. 4 S-RRIS outpu current variation

3. Constant Transconductance RRIS Circuit description

The S-RRIS $g_{m,tot}$ changes as the common mode input voltage varies from $-V_{SS}$ to V_{DD}; when V_{CM} is close to one supply rail voltage, the corresponding differential pairs turns off lowering $g_{m,\text{tot}}$. To compensate for this decrease and to keep $g_{m,\text{tot}}$ constant, the other differential pair must double its transconductance.

Fig. 5 presents an almost constant transconductance rail-to-rail input stage (CT-RRIS) implementation using a Zener diode [1, 4].

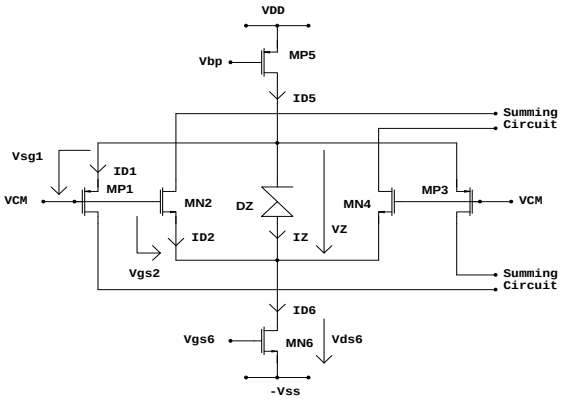

Fig. 5. Constant transconductance RRIS.

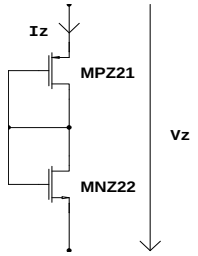

Fig. 6 Zener diode implementation.

Both MP5 and MP6 transistors provide a bias current equal to $8I_0$. For V_{CM} midrange both differential pairs are biased at I_0, so $g_{m1}=g_{m2}=g_m$, and the $6I_0$ extra bias current flows through the Zener diode. For small V_{CM} values the *n* pair is off ($g_{m2}=0$), but the *p* pair operates at $4I_0$ (as the Zener circuit is also off) and thus it has $g_{m1}=2g_m$. Similarly, for high V_{CM} values, the *p* pair is off, the Zener circuit is also off, and the *n* pair operates at $4I_0$. In all three cases we get $g_{m,\text{tot}}^{\max}=2g_m$.

The Zener diode functionality is implemented using diode connected MPZ21 and MPZ22 transistors (see Fig. 6). These transistors work at the same

overdrive voltage as the differential pair, but the Zener diode current must be $6I_0$. To achive this, we use $(W/L)_{Z21}=(W/L)_1$ and $(W/L)_{Z22}=(W/L)_2$.

4. Total Transconductance Variation

This section presents a simple model suitable for CT-RRIS $g_{m,\text{tot}}$ versus V_{CM} dependence manual analysis. A more detailed circuit behavior analysis can be found in [4]. The circuit operation has several states, each state corresponding to a specified V_{CM} range. The V_{CM} range threshold values are given by:

$$V_{CM}^{nL} = -V_{ss} + V_{Tn} - 2V_{ov} \quad (8)$$

$$V_{CM}^{n} = -V_{ss} + V_{Tn} + \left(1 - 2/\sqrt{7}\right) V_{ov6} \quad (9)$$

$$V_{CM}^{nU} = -V_{ss} + V_{Tn} + V_{ov} + V_{ov6} \quad (10)$$

$$V_{CM}^{pL} = V_{dd} - V_{Tp} - V_{ov} - V_{ov5} \quad (11)$$

$$V_{CM}^{p} = V_{dd} - V_{Tp} - \left(1 - 2/\sqrt{7}\right) V_{ov5} \quad (12)$$

$$V_{CM}^{pU} = V_{DD} - V_{Tp} + 2V_{ov} \quad (13)$$

The differential pair current variation is presented in Fig. 7

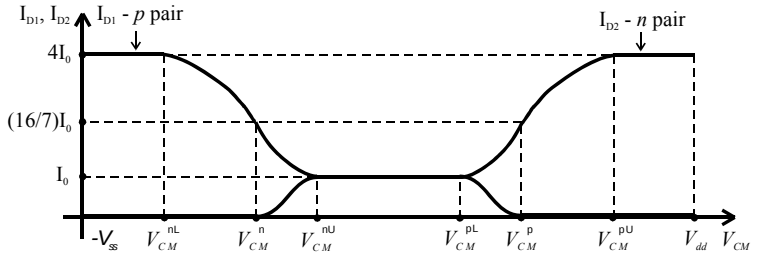

Fig. 7 Constant transconductance RRIS output current variation.

We can express the differential stages transconductance using the drain currents. From (5) we have

$$g_{m1,2} = \sqrt{2K_{1,2}\, I_{D1,2}} = \sqrt{2K_{1,2}\, I_0}\sqrt{I_{D1,2}/I_0} = g_m\sqrt{I_{D1,2}/I_0} \quad (14)$$

For all operating regions, the corresponding drain currents and transconductances values are presented in Table 1.

Table 1

V_{CM}	Differential pairs current		Differential pairs transconductance	
	$I_{D2}-n$ pair	$I_{D1}-p$ pair	$g_{m2}-n$ pair	$g_{m1}-p$ pair
$-V_{ss}<V_{CM}<V_{CM}^{nL}$	0	$4I_0$	0	$2g_m$
$V_{CM}^{nL}<V_{CM}<V_{CM}^{n}$	0	$4I_0\ldots(16/7)I_0$	0	$2\,g_m\ldots\left(4/\sqrt{7}\right)g_{\mathrm{m}}$
$V_{CM}^{n}<V_{CM}<V_{CM}^{nU}$	$0\ldots I_0$	$(16/7)I_0\ldots I_0$	$0\ldots\ g_m$	$\left(4/\sqrt{7}\right)g_{\mathrm{m}}\ldots\ g_m$
$V_{CM}^{nU}<V_{CM}<V_{CM}^{pL}$	I_0	I_0	g_m	g_m
$V_{CM}^{pL}<V_{CM}<V_{CM}^{p}$	$I_0\ldots(16/7)I_0$	$I_0\ldots0$	$g_m\ \ldots\left(4/\sqrt{7}\right)g_{\mathrm{m}}$	$g_m\ldots0$
$V_{CM}^{p}<V_{CM}<V_{CM}^{pU}$	$(16/7)I_0\ldots4I_0$	0	$\left(4/\sqrt{7}\right)g_{\mathrm{m}}\ldots2\ g_m$	0
$V_{CM}^{pU}<V_{CM}<V_{DD}$	$4I_0$	0	$2g_m$	0

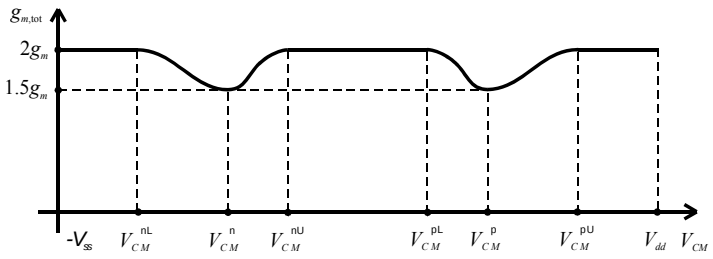

Fig. 8 Constant transconductance RRIS total transconductance variation.

The $g_{m,\mathrm{tot}}(V_{CM})$, given in Fig. 8, has two equal minimums at V_{CM}^{n}, and V_{CM}^{p}

$$g_{m,\mathrm{tot}}^{\min}=\left(4/\sqrt{7}\right)g_m\cong1.5g_m=0.75g_{m,\mathrm{tot}}^{\max} \qquad (15)$$

5. Weak inversion constant $g_{m,\mathrm{tot}}$ RRIS
Weak inversion MOS transistor modeling

In the previous sections, we considered the differential MOS pair biased in strong inversion. Another approach, that has several significant advantages, is to operate the differential pair in the weak inversion region. We start with the EKV model [5], a mathematical best-fit model that describes the MOS transistor both in weak and strong inversion regions. The EKV model equation is:

$$I_D = I_S \ln^2\left[1 + e^{\frac{V_{gs}-V_T}{2V_{th}}}\right] \quad (16)$$

where I_S is a model parameter that includes the transistor geometry and technological parameters and $V_{th}=kT/q$ is the thermal voltage.

If we consider a rather large overdrive voltage, $V_{gs}-V_T>>2V_{th}$, the exponential term becomes much larger than unity and we get the saturation region strong inversion current-voltage equation:

$$I_D \cong I_S\left(\frac{V_{gs}-V_T}{2V_{th}}\right)^2 = \frac{1}{2}KV_{\text{ov}}^2 \quad (17)$$

For $V_{gs}-V_T<<2V_{th}$ using the $ln(1+x)\cong x$ approximation we get the weak inversion current-voltage equation:

$$I_D \cong I_S e^{\frac{V_{gs}-V_T}{V_{th}}} = I_o e^{\frac{V_{gs}}{V_{th}}} \quad (18)$$

6. Weak inversion rail-to-rail input stage

Deriving equation (18), we get the weak inversion MOS transistor g_m:

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{I_o}{V_{th}} e^{\frac{V_{gs}}{V_{th}}} = \frac{I_D}{V_{th}} \quad (19)$$

We note that, in weak inversion, g_m is proportional to the drain current and not to the drain current square root, as in strong inversion [see equation (5)].

For the weak inversion rail-to-rail input stage (WI-RRIS) we use the same circuit topology as for the CT-RRIS (see Fig. 5), with two major differences. First, the differential pair transistors are designed to work in weak inversion. This can be assured by choosing a large W/L transistor size. Second, the two bias transistors, MP5 and MN6 provide a bias current of $4I_0$, instead of $8I_0$.

The circuit operation is similar to the CT-RRIS, except that now, to double the transconductance, we only need to double the drain current. When both pairs are on, each differential transistor current is I_0 and the Zener diode takes the supplementary $2I_0$. When one differential pairs turns off, the Zener diode also turns off and its current is redistributed to the other differential pair, doubling its g_m.

7. Summing Circuit
Basic description

We shall use a summing circuit to transform the RRIS two differential current outputs into a single asymmetric current output. The summing circuit used in this paper is presented in Fig. 9. MP7 and MP8 act as current sources and generate the stage bias current, I_b. MN11 and MN12 form a current mirror, $I_{D11}=I_{D12}=I_S$. MP9 – MN14 are □ascade transistors.

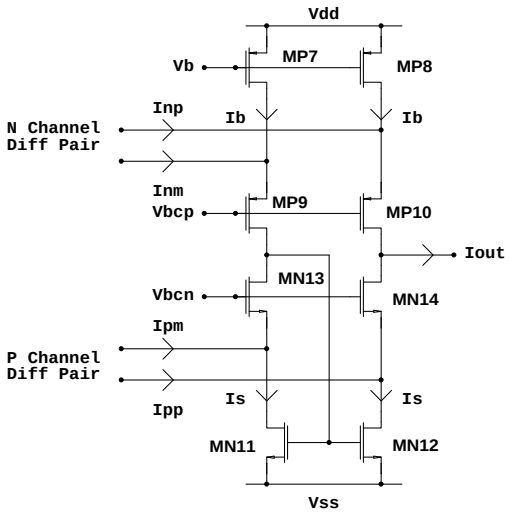

Fig. 9 Summing circuit

The stage operation is described by the following equation:

$$I_S = I_b + I_{nm} + I_{pm}\,,\; I_S = I_b + I_{np} - I_{out} + I_{pp} \qquad (20)$$

The output current result

$$I_{out} = \left(I_{np} - I_{nm}\right) + \left(I_{pp} - I_{pm}\right) \qquad (21)$$

Taking into account that $I_{dn}=I_{np}-I_{nm}$ is the *n* pair differential output current and $I_{dp}=I_{pp}-I_{pm}$ is the *p* pair differential output current, we get

$$I_{out} = I_{dn} + I_{dp} \qquad (22)$$

The bias current, I_b, assures that all transistors work at a reasonable drain current and do not enter the linear region. For this reason, I_b must be larger than the maximum input current (otherwise the output stage may run out of current).

The RRIS output currents are in fact the differential pairs drain currents:

$$I_{np} = -I_{D2} \qquad I_{nm} = -I_{D4}, \quad I_{pp} = I_{D1} \qquad I_{pm} = I_{D3} \tag{23}$$

8. Output resistance

The rail-to-rail unloaded amplifier voltage gain is equal to the input stage $g_{m,\mathrm{tot}}$ multiplied by the summing stage output resistance:

$$A = g_{m,\mathrm{tot}} R_{out} \tag{24}$$

A constant $g_{m,\mathrm{tot}}$ does not guarantee a constant voltage gain versus common mode voltage, V_{CM}. We have to take into account the output resistance and its V_{CM} dependence. The output resistance is given by parallel connected cascodes' stages output resistances MP8 – MP10 and MN12 – MN14.

$$R_{out} = R_{on} \,||\, R_{op} \tag{25}$$

where [2, 3]

$$R_{on} = g_{m14} r_{o12} r_{o14} \tag{26}$$

$$R_{op} = g_{m10} r_{o8} r_{o10} \tag{27}$$

The transistor output resistance is given by [2, 3]

$$r_o = \frac{1}{\lambda I_D} \tag{28}$$

where

$$\lambda = \frac{1}{L} \frac{dX_d}{dV_{ds}} \tag{29}$$

By choosing the transistor lengths so that

$$L_n \left(dX_d / dV_{ds} \right)_p = L_p \left(dX_d / dV_{ds} \right)_n \tag{30}$$

all transistors have the same λ.

We design MN14 and MP10 to have

$$K_{10} = K_{14} = K \tag{31}$$

We get

$$R_{on} = \frac{\sqrt{2KI_{D14}}}{\lambda^2 I_{D12} I_{D14}} \quad (32)$$

$$R_{op} = \frac{\sqrt{2KI_{D10}}}{\lambda^2 I_{D8} I_{D10}} \quad (33)$$

Using the R_{on} and R_{op} to express the output resistance [eq. (25)], we get:

$$R_{out} = \frac{\sqrt{2K}}{\lambda^2} \frac{1}{I_{D12}\sqrt{I_{D14}} + I_{D8}\sqrt{I_{D10}}} \quad (34)$$

Using the Fig. 9 notations we have

$$I_{D8} = I_b \quad (35)$$

$$I_{D10} = I_{D14} = I_b + I_{np} \quad (36)$$

$$I_{D12} = I_b + I_{np} + I_{pp} \quad (37)$$

The output resistance results:

$$R_{out} = \frac{\sqrt{2K}}{\lambda^2} \frac{1}{(2I_b + I_{np} + I_{pp})\sqrt{I_b + I_{np}}} \quad (38)$$

9. Output resistance for different input stage topologies

In this section, we estimate the summing stage output resistance versus common mode input voltage dependence for the three presented RRIS topologies.

Firstly, we have to choose the bias current, I_b. A large I_b reduces the output resistance variation but it also reduces the output resistance value and increase the current consumption. For this reason we will choose the minimum possible bias current value. The bias current, I_b, must always be larger than the RRIS output currents so, we choose I_b=2I_0 for the S-RRIS, I_b=8I_0 for the CT-RRIS and I_b=4I_0 for the WI-RRIS.

We rewrite equation (38) using I_b/I_0, I_{D1}/I_0 and I_{D2}/I_0 ratios [see (23)].

$$R_{out} = \frac{R_b}{\left[2\frac{I_b}{I_0} + \frac{I_{D1}}{I_0} - \frac{I_{D2}}{I_0}\right]\sqrt{\frac{I_b}{I_0} - \frac{I_{D2}}{I_0}}} \quad (39)$$

where R_b stands for

$$R_b = \frac{\sqrt{2K_0}}{\lambda^2 I_0 \sqrt{I_0}} \quad (40)$$

The evaluated R_{out}/R_b ratios for all three RRIS are given in Table 2.

Table 2

V_{CM} domain	S-RRIS [$I_b=2I_0$]			CT-RRIS [$I_b=8I_0$]			WI-RRIS [$I_b=4I_0$]		
	I_{D1}	I_{D2}	R_{out}/R_b	I_{D1}	I_{D2}	R_{out}/R_b	I_{D1}	I_{D2}	R_{out}/R_b
$-V_{ss} < V_{CM} < V_{CM}^{nL}$	I_0	0	0.141	$4I_0$	0	0.018	$2I_0$	0	0.050
$V_{CM}^{nU} < V_{CM} < V_{CM}^{pL}$	I_0	I_0	0.250	I_0	I_0	0.024	I_0	I_0	0.072
$V_{CM}^{pU} < V_{CM} < V_{DD}$	0	I_0	0.333	0	$4I_0$	0.042	0	$2I_0$	0.118

Fig. 10 presents the output resistance dependence of the common mode input voltage (at linear scale). We note that the V_{CM} threshold voltages have different values for different RRIS topologies [see eqs. (6) – (7) and (8) – (13)].

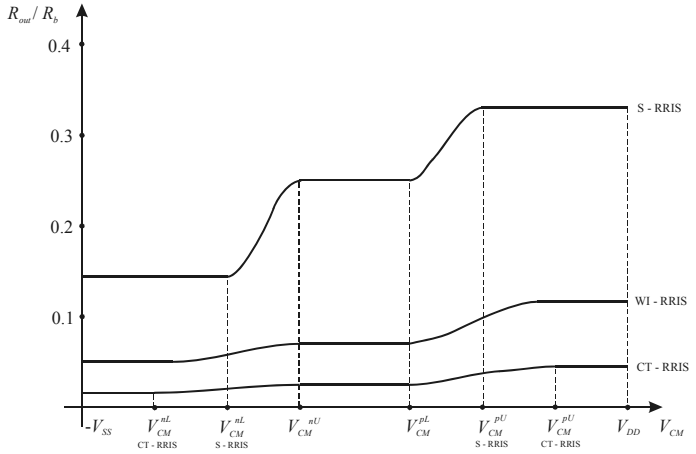

Fig. 10 Output resistance versus input common mode voltage

10. Total Voltage Gain

The total RRIS voltage gain can be estimated as $A=g_{m,\text{tot}}R_{out}$ [see equation (25)]. The S-RRIS $g_{m,\text{tot}}$ [see Fig. 3] is equal to $2g_m$ when both pairs are active ($V_{CM}^{nU} < V_{CM} < V_{CM}^{pL}$) and drops to g_m when either the *n* pair or the *p* pair is off ($-V_{ss} < V_{CM} < V_{CM}^{nL}$ and respectively $V_{CM}^{pU} < V_{CM} < V_{DD}$). For the CT-RRIS and WI-RRIS, the total transconductance [see Fig. 8] only varies during the transition

states and in this analysis it will be considered equal to $2g_m$. The output resistance values can be found in Table 2 [where R_b given by (40)]. The total voltage gain values for all three stages are given in Table 3.

Table 3

V_{CM} domain	S-RRIS [I_b=2I_0]			CT-RRIS [I_b=8I_0]			WI-RRIS [I_b=4I_0]		
	$g_{m,\text{tot}}$	R_{out}/R_b	A/g_mR_b	$g_{m,\text{tot}}$	R_{out}/R_b	A/g_mR_b	$g_{m,\text{tot}}$	R_{out}/R_b	A/g_mR_b
$-V_{ss} < V_{CM} < V_{CM}^{nL}$	g_m	0.141	0.141	$2g_m$	0.018	0.036	$2g_m$	0.050	0.100
$V_{CM}^{nU} < V_{CM} < V_{CM}^{pL}$	$2g_m$	0.250	0.500	$2g_m$	0.024	0.048	$2g_m$	0.072	0.144
$V_{CM}^{pU} < V_{CM} < V_{DD}$	g_m	0.333	0.333	$2g_m$	0.042	0.084	$2g_m$	0.118	0.236

For the S-RRIS, for high common mode input voltages, the transconductance drop compensates the output voltage growth, leading to a small gain change. At low V_{CM} values, both the transconductance and the output voltage decrease, resulting in an important voltage gain drop.

For the CT-RRIS and WI-RRIS, as $g_{m,\text{tot}}$ is practically constant, the voltage gain variation versus V_{CM} follows the output resistance variation.

We underline that this topology is optimized for constant total transconductance, so the total gain variation is significantly larger than the $g_{m,\text{tot}}$ variation.

11. SPICE simulation results

Fig. 11 presents the RRIS $g_{m,\text{tot}}$ simulation results (standard 0.8 μm CMOS process, 3 V single power supply). To get a better view of the $g_{m,\text{tot}}$ variation, the total transconductances were normalized to $g_{m,\text{max}}$. The base current, I_0 is 2 μA for all topologies. For the S-RRIS and CT–RRTS, the differential pairs' transistors were designed for V_{ov} = 0.2 V to operate in strong inversion, g_{m1}=g_{m2}=20 μA/V for both topologies. The WI-RRIS differential pairs works at a much lower overdrive voltage, to assure weak inversion.

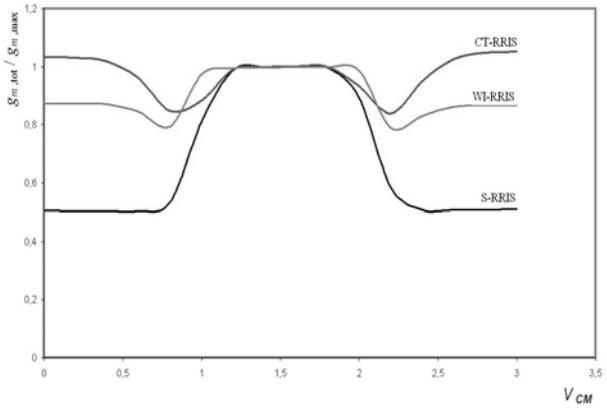

Fig. 11 Output resistance dependence on V_{CM}

12. Comparative analysis of the three RRIS topologies

This paper presents three RRIS topologies, each having different advantages and disadvantages. In this section, we give a comparative analysis of the presented RRIS, from several different perspectives. The purpose of this analysis is not to prove that one topology is better then another, but to help designers choose the best suited RRIS topology for a specific task.

Our main concern is the total transconductance variation over the input voltage common mode range. The S-RRIS has a total transconductance variation of 50% while the CT-RRIS and WI-RRIS have a $g_{m,\mathrm{tot}}$ variation of around 15%.

Another important parameter is the total current consumption. The bias current needed by each stage is given in Table 4.

Table 4

	Input stage current	Summing stage current	Total current
S-RRIS	$2I_0$	$4I_0$	$6I_0$
WI-RRIS	$4I_0$	$8I_0$	$12I_0$
CT-RRIS	$8I_0$	$16I_0$	$24I_0$

This shows that keeping $g_{m,\mathrm{tot}}$ constant comes at the cost of higher current consumption: the CT-RRIS uses a four times larger current than the S-RRIS.

To compare the three RRIS topologies from the output resistance perspective, we refer to Table 2 and Fig. 10. For all three topologies, the output resistance changes by about 57% having the lowest value at low V_{CM} values. For a

given common mode voltage, the S-RRIS has an output resistance around three time larger than the WI-RRIS and nine times larger than the CT-RRIS.

Conclusions

This paper presents a rail-to-rail input stages topologies overview. Three rail-to-rail input stage topologies are analyzed: a simple RRIS (S-RRIS), a RRIS that uses a Zener diode to control the total current through the differential pairs to keep the total transconductance constant (CT-RRIS) and a RRIS based on differential pairs weak inversion operation (WI-RRIS). A summing stage topology is also presented and a simple model, suited for manual analysis is given for its output resistance.

The S-RRIS allows a common mode input voltage rail-to-rail swing, with a total transconductance variation of 50%. It has the smallest current consumption and the largest output resistance from all RRIS topologies.

The CT-RRIS reduces the $g_{m,\text{tot}}$ variation to 15%, but has a much larger current consumption and smaller output resistance than the S-RRIS.

The WI-RRIS uses weak inversion operation of the differential pairs, to reduce the current needed to keep $g_{m,\text{tot}}$ constant. This way, the WI-RRIS has lower total current consumption and higher output resistance than the CT-RRIS. Weak inversion operation provides higher transconductance for a given bias current, I_0. However, the weak inversion models are more complicated than deep inversion ones, so the WI-RRIS manual analysis is difficult. Also, using weak inversion can led to discrepancies between SPICE simulation and actual chip performances.

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