PARAMETERS EXTRACTION FROM SOME EXPERIMENTAL STATIC CHARACTERISTICS OF A PSEUDO-MOS TRANSISTOR

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Unul dintre cele mai investigate dispizitive SOI pentru caracterizarea electrica a plachetelor de tip Siliciu pe Izolator este tranzistorul pseudo-MOS. Acest articol are doua tinte : (1) de a prezenta o metoda noua de extractie a tensiunii de prag si de benzi-netede a unui tranzistor pseudo-MOS, bazata pe anularea derivatei a III-a a curentului de drena ; (2) in consecinta, se va putea extrage doparea filmului din placheta SOI fabricata prin metoda SIMOX. In acest scop, au fost utilizate curbe I_D-I_G, in inversie si acumulare.

One of the most investigated SOI device for the electrical characterization of Silicon On Insulator wafers is the pseudo-MOS transistor. This paper has two goals: (1) to present a new method for the threshold and flat–band voltage extraction of a pseudo – MOS transistor, based on the third order derivative zeroing of the drain current; (2) as a consequence of previous result, to extract the film doping in a SOI wafer manufactured by SIMOX technique. In this scope, experimental curves I_D-I_G, in inversion and accumulation were used.

Keywords: SOI device, parameters extraction, superior derivative

1. Introduction

The pseudo-MOS transistor is essentially a test device for in situ electrical characterization of the SOI wafers (Silicon On Insulator). This transistor is based on the upside-down MOS structure, that is inherent in all SOI materials.

In this paper, a square sample, 12 mm length, from a SOI wafer made in SIMOX technique, was used for the pseudo-MOS transistor. This technological technique is starting from a p-type substrate, and by Oxygen implantation, a n-type film even with a higher doping concentration is producing. This is related to the residuals O^- ions in film that acts like donors centers [1]. The final scope of this paper is to estimate the film doping.

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2. The transfer experimental characteristics

Fig. 1 presents the pseudo-MOS transistor, used in experiments. The gate terminal is the metal support at the wafer bottom. For a n-type film, a positive (respectively negative) voltage must to be applied on the gate to induce an accumulation (respectively inversion) channel at the film bottom. Since to produce I_D-V_G curves in all regimes, the gate voltage was scanned from –10V up to +10V.

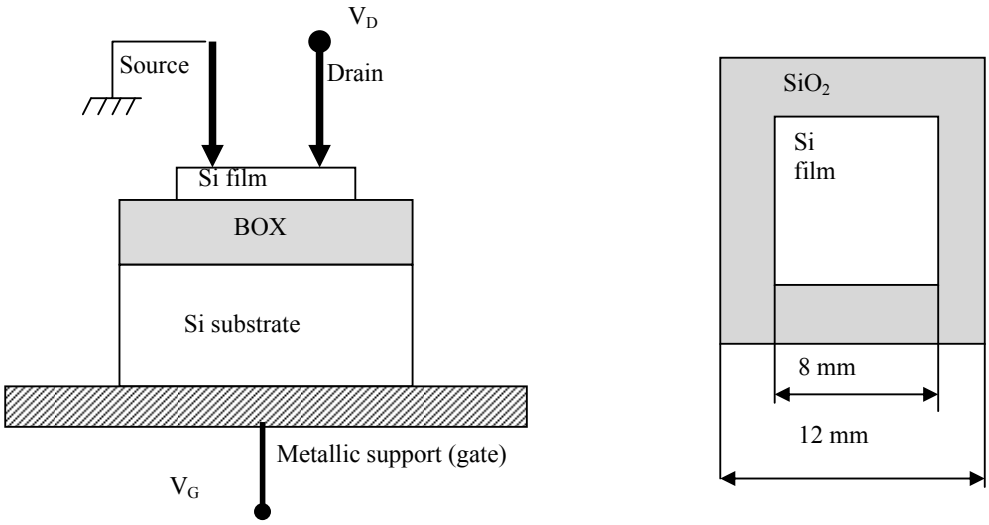


Fig.1. The pseudo-MOS transistor used in experiments.

The SOI wafer has: p-substrate with 10^{15} cm^{-3}=N_{A2} doping, the buried oxide thickness, x_{BOX}=0.4 μm; the film thickness, x_{S1}=0.2 μm, n-type film with unknown doping at this moment, N_{D1}.

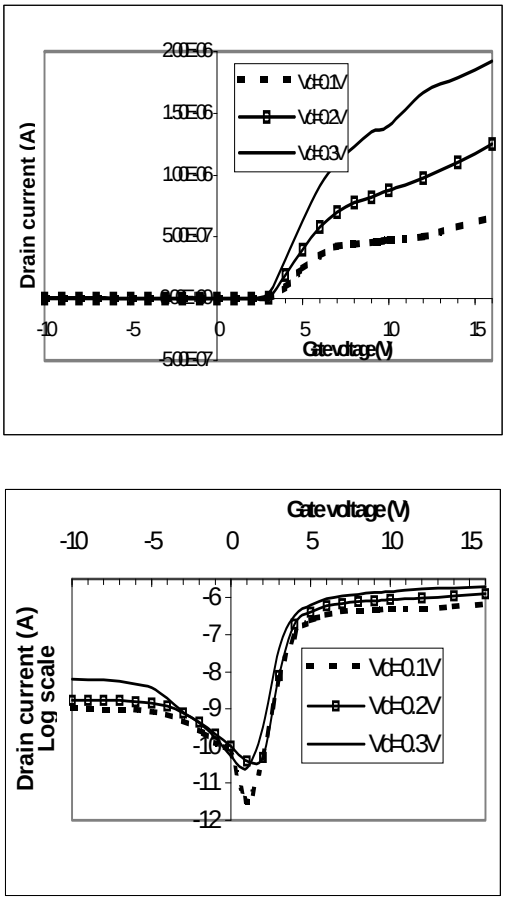


Fig. 2 The I_D-V_G characteristics at (a) linear, (b) logarithmic scale.

The source and drain contacts (that are two wires of a TAC), placed on the top of the film, were connected to the measuring system. The currents were read from a Keithley 236 picoampermeter. The source was grounded, while the drain was maintained at: +0.1V, +0.2V, +0.3V. The I_D-V_G experimental curves, achieved in this technique are available in fig.2. The sub-threshold conduction is more visible at logarithmic scale, fig. 2.b.

3. The threshold and flat–band voltages extraction

The threshold or flat-band voltage represents the boundary value for the strong inversion or strong accumulation onset [1]:

$$I_{Dinv/ac} = \frac{\mu_o f_g C_{BOX}(V_G - V_{T/FB})V_D}{1+\theta_{inv/ac}(V_G - V_{T/FB})} \quad (1)$$

where μ_o is the holes/electrons mobility at low fields, f_g is a geometrical factor, $C_{BOX}=\varepsilon_{BOX}/x_{BOX}$ is the buried oxide specific capacitance, $\theta_{inv/ac}$ is the attenuation mobility factor in transversal electric fields for the inversion /accumulation channels, V_T is the real threshold voltage, V_{FB} is the flat-band voltage, V_G is the gate voltage. The I_D-V_G logarithmic curves are more suitable for the non-linear conduction theorem applying [2]. Because V_T, V_{FB} represents some "knee" points of log I_D-V_G curve, they were extracted by the third order derivative zeroing method. The simulation results of the third order derivative drain current, are available in fig. 3.a.

The values: V_T = -2.16V, V_{FB} = 4.24V were computed by averaging the values extracted from fig. 3.a (there are three curves). The other value: +1.2V, that cancel the third order derivative must be the boundary between fully-depleted regime and strong inversion regime. The positive values of V_{FB} mustn't surprise in a SOI device. The flat-band voltage compensates: the positive electric charges from the buried oxide, the metal-semiconductors work-functions, the semiconductor-semiconductor work function (positive), the negative electric charges from depleted substrate (a positive quantity).

As in the case of a bulk device, the real threshold voltage, V_T, is a superposition of the real effects (included in V_{FB}) over an ideal threshold voltage value V_{Tid}:

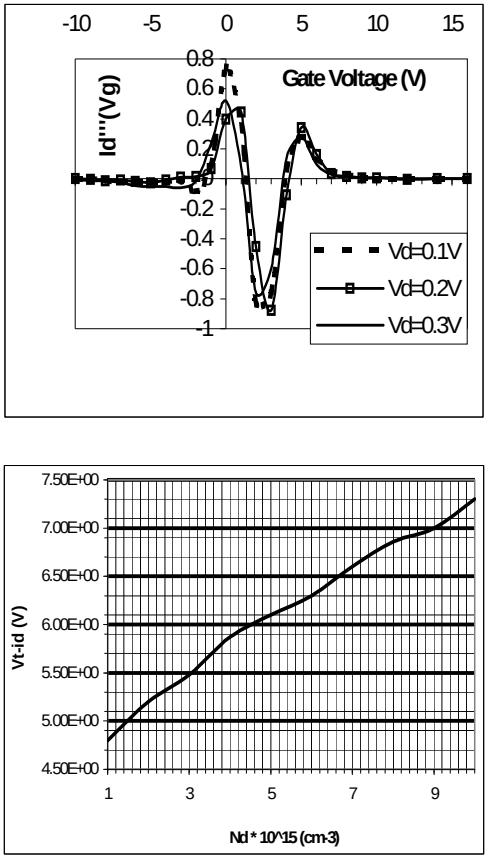
$$V_T = V_{Tid} + V_{FB} \Rightarrow V_{Tid} = -6.4V \quad (2)$$

4. The film doping estimation

In a general manner, the analytical model for the ideal threshold voltage of a fully depleted pseudo-MOS transistor is given by, [3, 4]:

$$V_{Tid} = -2\phi_{F1}\left(1+\frac{\varepsilon_{SI}}{\varepsilon_{BOX}}\frac{x_{BOX}}{x_{SI}}\right) - \frac{qN_D}{q\varepsilon_{BOX}}x_{SI}x_{BOX} - 2\phi_{F2} \quad (3)$$

where $\Phi_{F1,2}$ is the Fermi potential in film/substrate; $\varepsilon_{Si,BOX}$ is the silicon /oxide dielectric permittivity; N_D is the film doping concentration.



(a) (b)

Fig. 3. (a) The third order derivative for I_D-V_G experimental curves; (b) a graphical solution of eq.(3), representing V_{Tid}-N_D dependence.

Equation (3) represent a non-linear relationship between the ideal threshold voltage value, V_{Tid}, and the doping N_D. The others constants are know from the SIMOX process – see 2 paragraph. Solving this equation in a graphical manner (see fig. 3.b), the film doping was extracted: $N_D=5{,}9x10^{15}cm^{-3}$. This value is in agreement with the specialty literature [1], higher versus the substrate doping concentration.

5. Conclusions

SOI wafer made by SIMOX process was the physical support for a pseudo-MOS transistor. The experimental curves, I_D-V_G, provided the threshold and flat-band voltages by third order derivative zeroing method.

On the other hand, the I_D-V_G experimental curves demonstrated the transistor-like behavior of this type of transistor both in inversion and accumulation. The film doping was estimated at $N_D=5,9\bullet10^{15}cm^{-3}$, higher than substrate doping, that is in accordance with specialty literature.

R E F E R E N C E S

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