SPECIAL SOLUTION PLANNING PROGRAMMED HYBRID DPWM ALGORITHM FOR THREE-LEVEL INVERTER BASED ON V-S BALANCE PRINCIPLE

Yi LIU[1], Xiuyuan PING[2]

To simplify the control algorithm, balance the neutral point potential and reduce the switching loss, a novel hybrid DPWM algorithm is proposed with the advantages of carrier modulation and voltage space vector. The three-dimensional switching sequence is calculated by the voltage space vector method. Then, a general special solution planning programmed DPWM based on voltage-second balance principle is proposed to calculate the switching action time, which can overcome the complicated calculation of the traditional voltage space vector method and overcome the complicated problem of the traditional carrier modulation zero-sequence voltage calculation. In addition, a neutral potential hysteresis control method is proposed by controlling the zero-sequence voltage component to achieve the control of the midpoint current. Simulation and experiments show the effectiveness of the proposed algorithm.

Keywords: hybrid DPWM; three-level inverter; V-S balance; zero-sequence voltage

1. Introduction

Multilevel inverters have the advantages of closer output voltage to sinusoidal wave, lower voltage withstanding level of devices, and lower harmonic content of output voltage and current [1], [2]. Neutral point clamped three-level inverters (NPC-TLI) have more application prospects because of its simple structure and no need of complex transformers. It has been widely studied and applied in the fields of reactive power compensator of power grid and speed regulation of medium and high voltage motor [3-7]. And with the improvement of the output waveform quality requirements, NPC-TLI are gradually applied in low-voltage applications, especially in the field of new energy automotive motor controllers.

Since switching losses often determine the thermal stability of critical power devices in the system and have a decisive role in system reliability and service life, Discontinuous Pulse-Width Modulation (DPWM) has unique

[1] School of Electrical Engineering and Automation, Henan Institute of Technology, China, e-mail: flamepearlly@126.com
[2] Jiangsu Engineering Research Center for Electrical Driver and Control, China

advantages in high-power applications [8]. Usually, DPWM can be realized in two ways, namely the method of space voltage vector and the method of carrier modulation [9], [10]. The method of space voltage vector needs to calculate the large and small sectors of the reference voltage position and calculate the action time of different space voltage vectors. Due to the complexity of the space voltage vector diagram, this requires a lot of calculation time. However, the carrier modulation method can effectively reduce the calculation time. Compared with the method of carrier modulation and space voltage vector, the difficulty lies in the calculation of zero-sequence voltage. The calculation method of zero-sequence voltage under different switching sequences is different, and the physical meaning is not clear, and the control of mid-point potential is difficult.

According to the different clamping modes, four kinds of DPWM suitable for NPC-TLI were proposed, namely DPWM I to DPWM IV [11], [12]. Under different power factors, the above DPWM has different switching loss reduction ability. An improved DPWM is proposed, in which the clamping interval varies with the load power factor [13]. The ability to reduce the switching loss is more significant when the modulation is high. A generalized DPWM is adopted [14]. Switching loss reduction ability can be maximized by clamping the phase with the maximum current value to the neutral line. However, this method is only applicable to the case where the modulation degree is less than 0.5. Although DPWM can effectively reduce the switching loss, it has some shortcomings in the control of neutral point voltage. National scholars have proposed a number of software-based PWM strategies to suppress midpoint voltage offset [15]. An extended discontinuous pulse width modulation (EDPWM) is proposed, which can balance NP voltage under the full range of modulation index and power factor [16]. In order to control the neutral point voltage, a new DPWM based on clamp mode dynamic switching is proposed [17]. However, there are some additional switching action when switching between different clamping modes. A hybrid modulation strategy of DPWM and CBPWM is proposed [18]. Two PWM strategies are switched by hysteresis control. Due to the use of CBPWM in some areas, the total switching loss reduction capability is weakened. The method of switching clamping mode is adopted to realize the effective control of neutral point voltage [19]. In addition, in order to avoid introducing additional switching action when switching different clamping modes, a novel pulse sequence DPWM that can realize seamless switching of clamping mode is proposed [20]. A minimum fluctuation reference DPWM technique is proposed, the reference of modulation technique injects the least zero sequence signal of DPWM IV [21]. The polarity of the twice common mode voltages injection is regulated according to the polarity of the proportional allocation factor to realize the neutral-point voltage balancing [22]. Through theoretical analysis, the technology can make the inverter have high DC voltage utilization ratio, and improve the performance

index of common-mode voltage, voltage distortion and switching loss of the inverter. However, some of these DPWM method still needs a lot of trigonometric function operation, the calculation is more complex.

In order to simplify the control algorithm, balance the neutral point potential and reduce the switching loss, from the perspective of combining the advantages of carrier modulation and voltage space vector, a novel DPWM algorithm based on hybrid method is studied in this paper. Through the idea of special solution planning and trigger pulse distribution, the method of large sector division is proposed by the voltage space vector, and then a general special solution planning programmed DPWM based on voltage-second(V-S) balance principle is studied to calculate the switching action time, which can overcome the complicated calculation of the traditional voltage space vector method and overcome the complicated problem of the traditional carrier modulation zero-sequence voltage calculation. In addition, a neutral potential hysteresis control method is proposed by controlling the zero-sequence voltage component to achieve the control of the midpoint current. Thus, the charging and discharging of the neutral point can be controlled orderly. Finally, simulation and experiments are used to verify the validity of the proposed algorithm.

The rest of the paper is structured as it follows: in section 2, the hybrid DPWM algorithm based on V-S balance principle is analyzed in detail; section 3 shows the simulation and experimental results of hybrid DPWM algorithm proposed; and finally conclusions are drawn in section 4.

2. Hybrid DPWM algorithm based on V-S balance principle

2.1 Judgement method for the lager sector

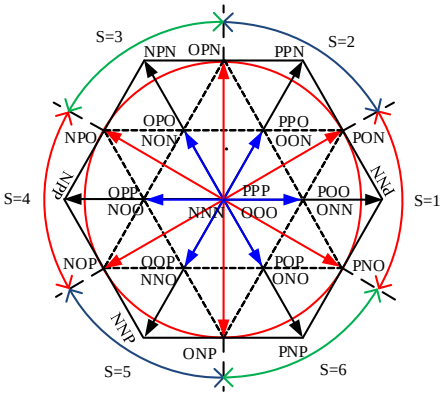


Fig. 1. Sector division for the proposed hybrid DPWM

The large sector partitioning method of DPWM is first given. The proposed method of large sector division refers to the way of voltage space vector.

It is used to determine the three-phase switching sequence of DPWM, as shown in Fig.1. The expression of the three-phase sinusoidal voltage is given as Eq. (1), where m is the degree of modulation, θ is the position of the reference voltage space vector, and U_{dc} is the DC bus voltage.

$$\begin{cases} u_{\mathrm{a}}^{\mathrm{ref}} = mU_{dc}\cos(\theta) \\ u_{\mathrm{b}}^{\mathrm{ref}} = mU_{dc}\cos(\theta - 2\pi/3) \\ u_{\mathrm{c}}^{\mathrm{ref}} = mU_{dc}\cos(\theta + 2\pi/3) \end{cases} \tag{1}$$

The sector judgment defined in Fig.1 is based on the polarity of three-phase sinusoidal modulation wave, as shown in Table 1.

Table 1

Judgement method for the sector

Phase	Sector					
	1	2	3	4	5	6
a	+	+	-	-	-	+
b	-	+	+	+	-	-
c	-	-	-	+	+	+

After calculating the large sector, the DPWM proposed in this paper is different from that of the voltage space vector, so there is no need to further calculate the small sector where the reference voltage vector is located.

2.2 Special solution planning programmed DPWM

The control objectives of NPC three-level converter mainly include output harmonic optimization, neutral point potential balance, low-frequency pulsation suppression, switching loss and so on. The realization of the above objectives is based on the V-S balance principle. Therefore, for PWM with fixed carrier frequency, the optimal control of each control objective is actually the process of planning the special solution of V-S balance equations.

The V-S balance equations of general three-phase PWM converter are as follows:

$$\begin{cases} (u_{\mathrm{a}}^{\mathrm{ref}} + u_z)T_s = (T_{\mathrm{ap}} - T_{\mathrm{an}})U_{dc} \\ (u_{\mathrm{b}}^{\mathrm{ref}} + u_z)T_s = (T_{\mathrm{bp}} - T_{\mathrm{an}})U_{dc} \\ (u_{\mathrm{c}}^{\mathrm{ref}} + u_z)T_s = (T_{\mathrm{cp}} - T_{\mathrm{cn}})U_{dc} \end{cases} \tag{2}$$

The constraints of V-S balance equations are as follows

$$\begin{cases} 0 \le T_{\mathrm{jp}} \le T_s \\ 0 \le T_{\mathrm{jn}} \le T_s \\ 0 \le T_{\mathrm{jp}} + T_{\mathrm{jn}} \le T_s \end{cases} \tag{3}$$

where, j = a, b, c; the physical meaning of T_{jp} and T_{jn} are shown in Fig.2.

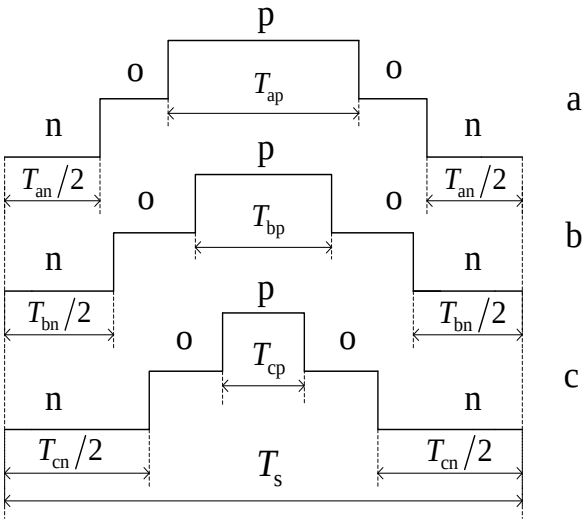


Fig. 2. Action time of three phase switch state for PWM

Different kinds of PWM can be realized by carrier PWM. The difference lies in the difference of three-phase modulation waveform.

Taking the first large sector as an example, the voltage space vectors contained in this sector are: large vector (PNN), zero vector (OOO, PPP, NNN), medium vector (PON, PNO) and small vector (POO, ONN). In practical systems, in order to reduce the common mode voltage, only the zero vector OOO is often used to synthesize the reference voltage vector. According to the three-phase state in the six voltage space vectors, the switching state of the phase a can be switched between O and P, and the switching states of the b and c phases are switched between N and O. Under the new large sector partitioning method, the three-phase switching sequence can be obtained according to the large sector label as shown in Table2.

Table 2

Switching sequence for each sector

Phase	Sector					
	1	2	3	4	5	6
a	O-P	O-P	N-O	N-O	N-O	O-P
b	N-O	O-P	O-P	O-P	N-O	N-O
c	N-O	N-O	N-O	O-P	O-P	O-P

Therefore, the V-S balance equations can be further sorted out.

$$\begin{cases} \left(u_{\mathrm{a}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}=u_{\mathrm{c1}}*t_{\mathrm{a}} \\ \left(u_{\mathrm{b}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}=-u_{\mathrm{c2}}*\left(T_{\mathrm{s}}-t_{\mathrm{b}}\right) \\ \left(u_{\mathrm{c}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}=-u_{\mathrm{c2}}*\left(T_{\mathrm{s}}-t_{\mathrm{c}}\right) \end{cases} \tag{4}$$

where, u_{c1} and u_{c2} are voltages of upper and lower supporting capacitors of DC bus in NPC three-level topology.

The switching time of the three phases is obtained as follows:

$$\begin{cases} t_{\mathrm{a}}=\left(u_{\mathrm{a}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}/u_{\mathrm{c1}} \\ t_{\mathrm{b}}=T_{\mathrm{s}}+\left(u_{\mathrm{b}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}/u_{\mathrm{c2}} \\ t_{\mathrm{c}}=T_{\mathrm{s}}+\left(u_{\mathrm{c}}^{\mathrm{ref}}+u_{\mathrm{z}}\right)*T_{\mathrm{s}}/u_{\mathrm{c2}} \end{cases} \tag{5}$$

Considering the physical meaning of t_{j} (j = a, b, c), its numerical value must satisfy the equation.

$$0\le t_{\mathrm{j}}\le T_{\mathrm{s}} \qquad \mathrm{j=a,\ b,\ c} \tag{6}$$

The injected zero sequence voltage shall meet the following equation:

$$\begin{cases} -u_{\mathrm{a}}^{\mathrm{ref}}\le u_{\mathrm{z}}\le -u_{\mathrm{a}}^{\mathrm{ref}}+u_{\mathrm{c1}} \\ -u_{\mathrm{b}}^{\mathrm{ref}}-u_{\mathrm{c2}}\le u_{\mathrm{z}}\le -u_{\mathrm{b}}^{\mathrm{ref}} \\ -u_{\mathrm{c}}^{\mathrm{ref}}-u_{\mathrm{c2}}\le u_{\mathrm{z}}\le -u_{\mathrm{c}}^{\mathrm{ref}} \end{cases} \tag{7}$$

The maximum and minimum of zero sequence voltage vector are defined. In order to keep generality, DC bus voltage U_{dc} is introduced to further limit zero sequence voltage vector in special solution planning. Therefore, the minimum and maximum values of the zero-sequence voltage injected by the first large sector can be calculated according to Eq. (8)

$$\begin{cases} u_{\mathrm{z}}\ge \max\left(-u_{\mathrm{a}}^{\mathrm{ref}},-u_{\mathrm{b}}^{\mathrm{ref}}-0.5U_{\mathrm{dc}},-u_{\mathrm{c}}^{\mathrm{ref}}-0.5U_{\mathrm{dc}}\right) \\ u_{\mathrm{z}}\le \min\left(-u_{\mathrm{a}}^{\mathrm{ref}}+0.5U_{\mathrm{dc}},-u_{\mathrm{b}}^{\mathrm{ref}},-u_{\mathrm{c}}^{\mathrm{ref}}\right) \end{cases} \tag{8}$$

For the V-S balance equations, the controllable variables include zero sequence voltage, duty cycle of P state and N state, which affect the control objectives of NPC TLI in varying degrees. Different controllable variables can be obtained by selecting different calculation criteria, that is, different special solutions of V-S balance equations. In order to reduce the switch calculation, the zero sequence voltage can be directly selected from $u_{\mathrm{z}}^{\mathrm{min}}$ and $u_{\mathrm{z}}^{\mathrm{max}}$. Taking

$u_z = -u_b^{ref} - 0.5U_{dc}$ as an example, the DPWM switching sequence can be obtained as follows:

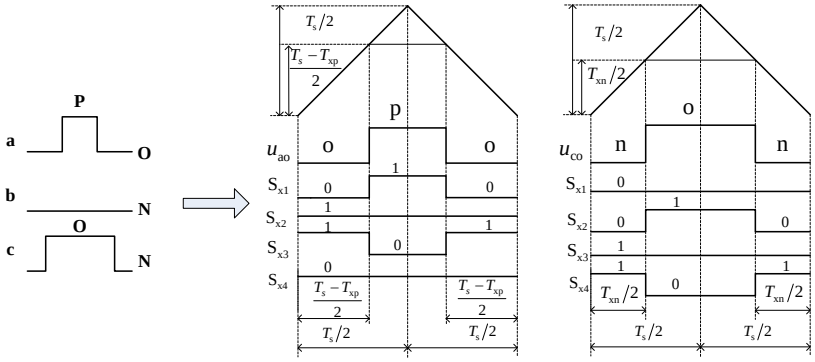


Fig. 3. Switching sequence of section 1 when $u_z = -u_b^{ref} - 0.5U_{dc}$

According to the different values of the zero sequence voltage component of DPWM, it can be found that there are three different bus clamping conditions in the switching sequence of DPWM, which is, clamping to the neutral point, clamping to the negative bus and clamping to the positive bus. However, no matter what kind of clamp, one phase switch does not operate in the whole carrier cycle, so it can effectively reduce the switching loss. Therefore, after the special solution of the V-S balance equations is obtained, the pulse distribution can be directly carried out according to the method shown in Fig.3. The software and hardware implementation is very simple.

2.3 Neutral potential hysteresis control

Different zero-sequence voltage components are selected, which have different effects on the midpoint potential. In order to control the midpoint potential of the three-level diode clamp type three-level inverter, a reasonable zero-sequence voltage component must be selected. In essence, the control of the midpoint potential is achieved by adjusting the midpoint current. The expression of the amount of charge flowing through the midpoint is shown in Eq. (9).

$$\Delta Q = (i_{c1} - i_{c2})T_s = C\frac{d\left(u_{c1} - u_{c2}\right)}{dt}T_s \tag{9}$$

The condition of neutral point potential balance is that the charge quantity $\Delta Q = 0$ in a single carrier period has a solution. However, the condition of Eq. (9) is that the three-phase current remains unchanged in a single carrier period, and the capacitance parameters of upper and lower buses are identical. But, the capacitance parameters of the upper and lower buses often have certain deviations in the actual system. At the same time, there are also some quantization errors in the digital processing system, so the hypothesis of Eq. (9) cannot be strictly met.

According to the neutral point potential equilibrium condition and the programming special solution group, since phase a and c only contain two output states, the action time of changing O state can only be realized by adjusting zero sequence voltage. The expression of neutral point potential u_o is shown in Eq. (10).

$$u_o = u_{c2} - 0.5(u_{c1} + u_{c2}) = 0.5(u_{c2} - u_{c1}) \tag{10}$$

In order to avoid frequent regulation, hysteresis control is adopted for voltage deviation. Hysteresis output is represented by variable H. If $u_o > \alpha U_{dc}$, then $H = 1$, if $u_o <- \alpha U_{dc}$, then $H = -1$. Bus deviation coefficient α can be set according to actual situation.

If H=1, it is necessary to discharge from the midpoint, that is, to make $\Delta Q < 0$. It is shown that the lower bus voltage is larger than that of the up-bus voltage, so zero sequence voltage components should be appropriate to minimize the continuous charging of the lower bus capacitor. Considering the difference of three-phase switch states and the influence of current direction, taking the first sector (S=1) as an example, the switching state of phase *a* is switched between O and P, and that of phase b and c are switched between N and O. The current coefficient K_j (j = *a*, *b*, *c*) is defined for the convenience of expression. The value of current coefficient K_j is related to the switch state. The switch state of phase *a* is switched between O and P, taking $K_a = 1$. The switch states of phase *b* and phase *c* are switched between N and O, taking $K_b = K_c = -1$.

Combining the direction of three-phase current and the different effects of zero-sequence voltage u_z^{min} or u_z^{max}, the zero-sequence voltage selection factor is defined as Γ.

$$\Gamma = K_j * i_j \qquad (j = a, b, c) \tag{11}$$

If $\Gamma > 0$, select the zero-sequence voltage component u_z^{min} with smaller neutral point current to reduce the continuous charging of the lower bus capacitor. If $\Gamma < 0$, select the zero-sequence voltage component u_z^{max} with larger neutral point current to reduce the continuous charging of the lower bus capacitor as far as possible. Similarly, it can be concluded that the selection of zero sequence voltage is the case where the upper bus voltage is larger than the lower bus voltage. Selection of zero sequence voltage is shown in the Table 3.

Table 3

Selection of zero sequence voltage

H	Γ	u_z
1	>0	u_z^{min}
1	<0	u_z^{max}
-1	>0	u_z^{max}
-1	>0	u_z^{min}

When the zero-sequence voltage component u_z is calculated, it can be superimposed on the three-phase sinusoidal reference voltage to generate the corresponding modulation wave. Compared with the triangular carrier wave, the final driving pulse is generated. Obviously, the hybrid DPWM method proposed in this paper calculates the three-phase switching sequence by using the voltage space vector method, and then calculates the switching time and the modulation wave by using the carrier modulation method based on the V-S balance special solution planning. This method can overcome the complexity of the traditional voltage space vector method and the complexity of the traditional carrier modulation zero-sequence voltage calculation.

3. Simulation and experiment

In order to verify the effectiveness of the DPWM proposed in this paper, a three-level converter simulation model is built in Matlab/Simulink as shown in Fig.4, in which the DC bus voltage is set to 540V, the upper and lower DC bus capacitors are both 2000μF, and the carrier frequency is set to 2kHz. The phase resistance-inductance load is 10Ω, 22mH, and the output fundamental frequency is 50Hz.

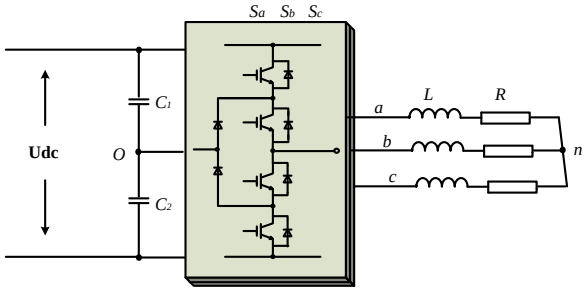
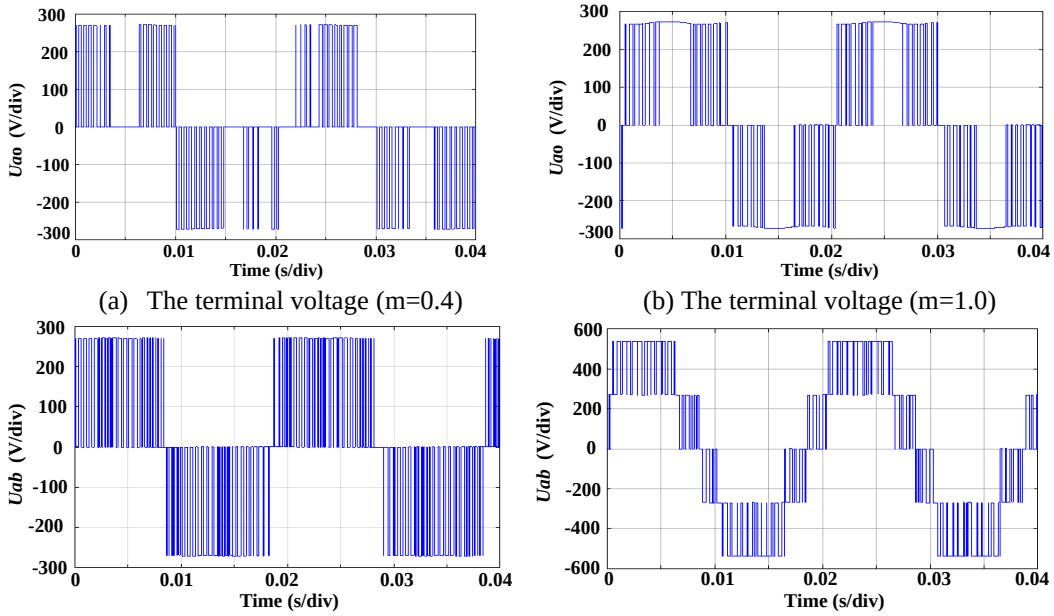


Fig 4. Simulation model of NPC TLI for hybrid DPWM

The terminal voltage waveforms of the hybrid DPWM simulation results with the modulation set to 0.4 and 1.0 are shown in the following Fig.5. The terminal voltage between the output and the neutral at phase are shown in the Fig.5 (a) and (b). The terminal voltage contains three voltage steps, and it is clamped to the middle point of capacitor in a number of switching cycles. During the clamping process, the switching transistor of phase a does not operate, so the switching loss can be reduced. The line voltage waveforms are shown in Fig.5 (c) and (d). In the case of small modulation (e.g. m=0.4), the voltage waveform of the three-level line voltage is three steps. In the case of large modulation (e.g. m=1.0), the three-level line voltage waveform consists of five steps.

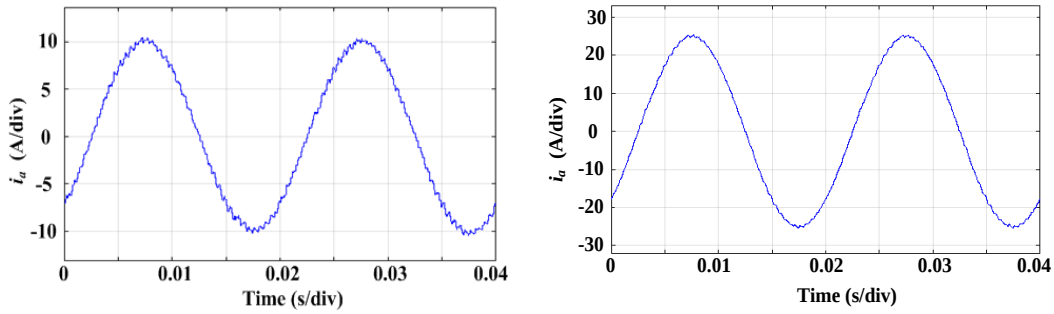


(a) The terminal voltage (m=0.4) (b) The terminal voltage (m=1.0)

(c) The line voltage (m=0.4) (d) The line voltage (m=1.0)

Fig 5. Waveforms of the terminal voltage and line voltage

Current waveforms of phase *a* with the modulation set to 0.4 and 1.0 are shown in the Fig.6. The current waveform has a high sinusoidal degree.



(a) Current waveform (m=0.4) (b) Current waveform (m=1.0)

Fig 6. Current waveforms of phase *a*

In order to verify the effectiveness of the proposed midpoint potential control method, the upper and lower bus-bar capacitor voltages are set to 295V and 245V at the initial time. The waveforms of the upper and lower capacitor voltages are given in Fig.7. During the voltage regulation process, it can be seen that the neutral point potential achieves equilibrium control before 0.03 s, thus verifying the effectiveness of the midpoint potential control proposed in this paper.

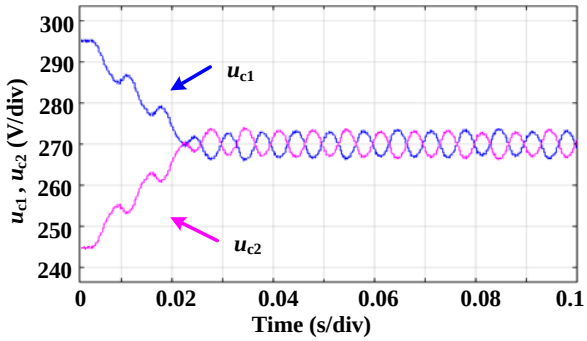


Fig 7. Waveforms of the upper and lower capacitor voltages (m=1.0)

In order to verify the effectiveness of the DPWM proposed in this paper, an experimental platform was built and the algorithm was verified. The main parameters of the experiment are consistent with the simulation parameters. The phase current is observed by the DA module of the control circuit board and the oscilloscope. The terminal voltage waveforms are measured by voltage differential probe.

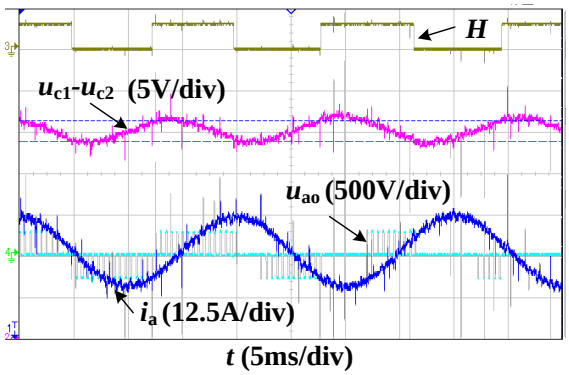


Fig 8. Waveforms of the experimental result with m = 0.4

Fig.8 shows the experimental results when the modulation degree is set to 0.4. The results show that the midpoint potential can be balanced by the hybrid DPWM proposed in this paper. The current has a higher sinusoidal degree. The phase voltage waveform indicates that this condition can be reduced by clamping to the three-level busbar midpoint, thereby reducing switching losses.

The experimental results with the modulation degree set to 1.0 are shown in Fig.9.

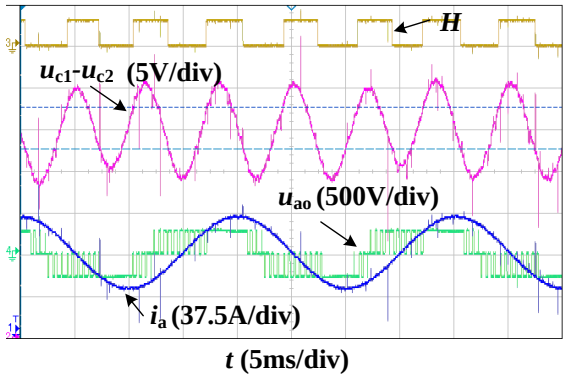


Fig 9. Waveforms of the experimental result with m = 1.0

The results show that the midpoint potential can be balanced by the hybrid DPWM proposed in this paper. The current has a higher sinusoidal degree, and the phase voltage waveform indicates that this condition is clamped to a three-level positive bus or negative bus, which can reduce switching losses.

4. Conclusions

In this paper, a general three-level hybrid DPWM modulation algorithm is proposed through the idea of special solution programming based on V-S balance principle. The physical meaning of the algorithm is clearer, a lot of trigonometric functions are omitted, and the algorithm is more concise. The hysteresis dynamic zero sequence voltage injection strategy is introduced to suppress the neutral point potential unevenness. Simulation and experiment results show that hybrid DPWM strategy proposed has lower switching loss and the same control effect than space vector and carrier modulation.

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REFERENCES

[1]. *K. Wang, Z. Zheng, L. Xu, and Y. Li*, "A generalized carrier-overlapped PWM method for neutral-point clamped multilevel converters," in IEEE Trans. on Power Electron., vol. 35, no. 9, Jan. 2020, pp. 9095-9106.

[2]. *H. Abu-Rub, J. Holtz, J. Rodriguez, and B. M. Ge*, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications". in IEEE Trans. Ind. Electron., vol. 57, no. 8, Aug. 2010, pp. 2581-2596.

[3]. *C. Li, T. Yang, P. Kulsangcharoen, G. L. Calzo, S. Bozhko, C. Gerada, and P. Wheeler*, "A modified neutral point balancing space vector modulation for three-level neutral point

clamped converters in high-speed drives," in IEEE Trans. Ind. Electron., vol. 66, no. 2, Feb. 2019, pp. 910-921.

[4]. *C. Xia, X. Gu, T. Shi, and Y. Yan*, "Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system," in IEEE Trans. Energy Convers., vol.26, no. 1, pp. 18-29, Mar. 2011.

[5]. *P. Madasamy, V.S. Kumar, P. Sanjeevikumar, J. B. Holm-Nielsen, and C. Bharatiraja*, "A three-phase transformerless T-Type- NPC-MLI for grid connected PV systems with common-mode leakage current mitigation," in Energies, vol. 12, no. 12, June. 2019, p. 2434.

[6]. *J. Zhou and P. T. Cheng*, "Modulation methods for 3L-NPC converter power Loss management in STATCOM application," in IEEE Trans. Ind. Appl., vol. 55, no. 5, June. 2019, pp. 4965-4973.

[7]. *X. Xing, X. Li, F. Gao, C. Qin, and C. Zhang*, "Improved Space Vector Modulation Technique for Neutral-Point Voltage Oscillation and Common Mode Voltage Reduction in Three-Level Inverter," in IEEE Trans. on Power Electron., vol. 34, no. 9, Sept. 2019, pp. 8697-8714.

[8]. *S. Mukherjee, S. K. Giri, S. Kundu, S. Banerjee*, "A generalized discontinuous PWM scheme for three-level NPC traction inverter with minimum switching loss for electric vehicles," in IEEE Trans. Ind. Appl., vol. 55, no. 1, Jan/Feb. 2019, pp.516-528.

[9]. *Z. Zeng, Z. Li, and S. Goetz*, "Optimal discontinuous space vector PWM for zero-sequence-circulating current reduction in two paralleled three-phase two-level converter," in IEEE Trans. Ind. Electron., to be published.

[10]. *X. Zhang, X. Wu, C. Geng, X. Y. Ping, S. Chen, and H. Zhang*, "An improved simplified PWM for three-level neutral point clamped inverter based on two-Level common-mode voltage reduction PWM," in IEEE Trans. Power Electron. , vol. 25, no. 10, Oct. 2020, pp.11143-11154.

[11]. *C. Xia, G. Zhang, Y. Yan, X. Gu, T. Shi, and X. He*, "Discontinuous space vector PWM strategy of neutral-point-clamped three-level inverters for output current ripple reduction," in IEEE Trans. Power Electron. , vol. 32, no. 7, July. 2017, pp.5109-5121.

[12]. *A. R. Beig, S. Kanukollu, K. Al-Hosani, and A. Dekka*, "Space-vector-based synchronized three-level discontinuous PWM for medium-voltage high-power VSI," in IEEE Trans. Ind. Electron., vol. 61, no. 8, Aug. 2014, pp.3891-3901.

[13]. *N. V. Nguyen, B. X. Nguyen, H. H. Lee*, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," in IEEE Trans. Ind. Electron., vol. 58, no. 9, Sept. 2011, pp. 3958-3966.

[14]. *S. Bhattacharya, D. Mascarella, and G. Joos*, "Space-vector-based generalized discontinuous pulse width modulation for three-level inverters operating at lower modulation indices," in IEEE J. Emer. Sel. Topics Power Electron., vol. 5, no. 2, June. 2017, pp.912-924.

[15]. *M. M. Hashempour, M. Y. Yang, and T. L. Lee*, "An adaptive control of DPWM for clamped-three-level photovoltaic inverters with unbalanced neutral-point voltage," in IEEE Trans. Ind. Appl., vol. 54, no. 6, NOV./Dec. 2018, pp. 6133-6148.

[16]. *K. Chen, W. Jiang, and P. Wang*, "An extended DPWM strategy with unconditional balanced neutral point voltage for neutral point clamped three-level converter," in IEEE Trans. Ind. Electron., vol. 66, no. 11, Nov. 2019, pp. 8402-8413.

[17]. *S. Yoo, J. S. Lee, and K. B. Lee*, "Novel discontinuous PWM method of a three-level inverter for neutral-point voltage ripple reduction," in IEEE Trans. Ind. Electron., vol. 63, no. 6, June. 2016, pp. 3344-3354.

[18]. *W. Jiang, Y. Gao, J. Wang, and L. Wang*, "A hybrid modulation strategy with reduced switching losses and neutral point potential balance for three-level NPC inverter," in J. Electrical Engineering & Technology, vol. 12, no. 2, Mar. 2017, pp. 738-750.

[19]. *W. Jiang, L. Li, J. Wang, F. Zhai, and J. Li*, "Improved discontinuous pulse width modulation strategy for neutral point clamped three-level inverter," in Automation of Electric Power Systems, vol. 42, no.24, Dec. 2018, pp. 127-134.

[20]. *W. Jiang, L. Li, J. Wang, M. Ma, F. Zhai, and J. Li*, "A novel discontinuous PWM strategy to control neutral point voltage for neutral point clamped three-level inverter with improved PWM sequence," in IEEE Trans. Power Electron., vol. 34, no. 9, Sept. 2019, pp. 9329-9341.

[21]. *J. Huang, Q. Liu, X. Wang, and K. Li*, "A carrier-based modulation scheme to reduce the third harmonic component of common-mode voltage in a three-phase inverter under high DC voltage utilization," in IEEE Trans. Ind. Electron., vol. 65, no. 3, Mar. 2018, pp. 1931-1940.

[22]. *K. Li, M. Wei, C. Xie, F. Deng, J. M. Guerrero, and J. C. Vasquez*, "Triangle carrier-based DPWM for three-level NPC inverters," in IEEE J. Emer. Sel. Topics Power Electron., vol. 6, no. 4, Dec. 2018, pp. 1966-1978.