DESIGN OF DOUBLE-GATE CMOS BASED TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER USING THE UTBSOI TRANSISTORS

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A CMOS operational transconductance amplifier (OTA) has been designed where the sizes of MOSFETs are evaluated through g_m/I_d methodology. Moreover, to implement the low power double-gate (DG)-CMOS OTA, BSIM- IMG model for the UTBSOI transistors has been utilized. Open-loop and unity-gain configurations have been analyzed as a function of DC gain, CMRR, PSRR, and power. Finally, important parameters of the latest reported papers have been taken from different sources and compared with the proposed OTA. Simulation results offered that the power consumption in DG-CMOS OTA has reduced by ≈ 50% from the best-reported paper so far.

Keywords: BSIM-IMG, DG-CMOS, g_m/I_d methodology, OTA, UTBSOI

1. Introduction

In general, the input signals fed to any system's transducer are analog in nature and are too small to provide necessary logic levels to any digital circuits. Thereby amplification of such analog signal is required to drive the prescribed functions. For the amplification purpose, operational amplifiers are highly desirable. An unbuffered (high output resistance) operational amplifier is better described as an operational transconductance amplifier (OTA) [1]. To design an amplifier requires a set of specifications like DC gain, unity-gain bandwidth (UGB), common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), common-mode input range (V_{iCMR}) etc. It may not be possible to satisfy all the specifications in the desired limit, and so there is always

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a trade-off in amplifier design [2]. Generally, single-stage OTAs have better frequency response and are faster compared to multistage OTAs. But, in low voltage application, the attainable open-loop DC gain is not sufficient for further applications [3]. Therefore, researchers are trying to achieve high DC gain by cascading or using multistage topologies operated at low bias current [4,5]. In multistage amplifiers, the output voltage swing can be increased with the penalty of bandwidth [6] along with high power consumption [7]. Therefore, to address these limitations, the number of stages in amplifiers is limited to two or three [3,7].

Many of the reported papers [8−10] on the design of two-stage OTAs are based on cascode topologies which have enhanced the gain and slew-rate. However, for low voltage applications, the cascode topology is less useful because of the limited output swing [11]. Although the papers [8,12] analyzed the circuit using the same topology but have not provided the transistor's dimensions. The work in [13] has evaluated the transistor's dimension using the square-law model, which is not valid for transistors at the sub-micron regime. The works in [10,11] have provided the transistor's dimensions where sizing methodologies of transistors have not been discussed. The presented work in [14] have described the sizing procedure of single-stage OTA using the g_m/I_d methodology [15,16] but has not extended their work for two-stage OTA. A proper elaborate description of sizing procedure of cascaded two-stage OTA in sub-micron technology has not been found so far in the literature.

Nowadays, with the trends on increasing mobility and performance in portable battery-operated devices, reduction in power consumption has become a challenging task for researchers. Miniaturization of the battery-operated devices is achieved through downscaling the technology node. Due to the downscaling, dimensions of the MOSFETs inside the integrated circuits (IC) have entered in nanoscale regimes. In the nanoscale regime, the shorter channel length of the MOSFET is prone to the physical effect known as short-channel effects (SCE). Thus, a large abnormality is observed in the ICs produced by the CMOS. Different advanced architectures of MOSFETs were proposed to overcome the limitations of SCEs [17]. Out of those architectures, the ultra-thin-body silicon-on-insulator (UTBSOI) MOSFET, as shown in Fig. 1 is a promising one for the DG-CMOS [18] technology. Dual gated system of the UTBSOI provides better scalability and superior controllability of gates over the shorter channel region. The back gate also provides the flexibility to attain the multiple threshold voltage control [19], which makes the device suitable for low voltage application [20]. Addition to this, the UTBSOI has a buried oxide layer, which reduces the parasitic junction capacitance, which in turn makes the device faster [20]. Moreover, the latch-up problem is not there in UTBSOI, which makes it superior to the conventional MOSFETs.

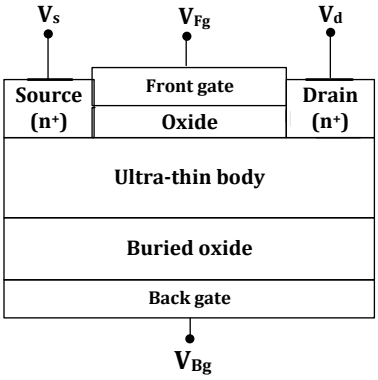


Fig. 1. Schematics showing the cross-sectional view of UTBSOI transistor.

To utilize the benefits of UTBSOI, a fast and accurate model for the device is required in the circuit simulators. The BSIM-independent multi-gate (IMG) [21] is an industry-standard model for UTBSOI which can be successfully adopted in the simulators like specter or spice to design and simulate any DG-CMOS based circuits.

In this paper, a two-stage CMOS OTA [1] has been designed in cascade topology, where the graphical models in [22], extracted through BSIM3v3 [23] have been utilized to size the transistors. Moreover, to solve the graphical models, an algorithm has been proposed and verified in MATLAB through g_m/I_d methodology over some set of specifications. The size of M_1 and M_2 has been evaluated from UGB and gain of the first stage (A_{v1}). The maximum common-mode input voltage $(V_{iCM,max})$ is used to evaluate the size of M_3, and M_4. Similarly, CMRR, PSRR, and minimum common-mode input voltage$(V_{iCM,min})$ are used for M_5, and M_7. The size of M_6 has been evaluated from its transconductance value (g_{m6}) and gain of the second stage (A_{v2}). Moreover, keeping the same transistor's sizes, the OTA topology has been simulated at the schematic level in DG-CMOS technology using the UTBSOI transistors. Simulation is performed using generic process-design kit (gpdk) 180-nm technology to analyze the open-loop and unity-gain configurations [1]. Various performance parameters like open-loop DC gain, phase margin (PM), CMRR, UGB, output-voltage swing, V_{iCMR}, and PSRR are extracted from the simulation. The DG-CMOS OTA [Fig. 2] is able to reduce the power consumption by ≈ 50% with respect to the best-reported paper [8] along with ≈144.2 dB CMRR.

2. Proposed Design of Two-Stage OTA

Fig. 2 shows the schematic of a two-stage OTA which has been considered for implementation in this paper.

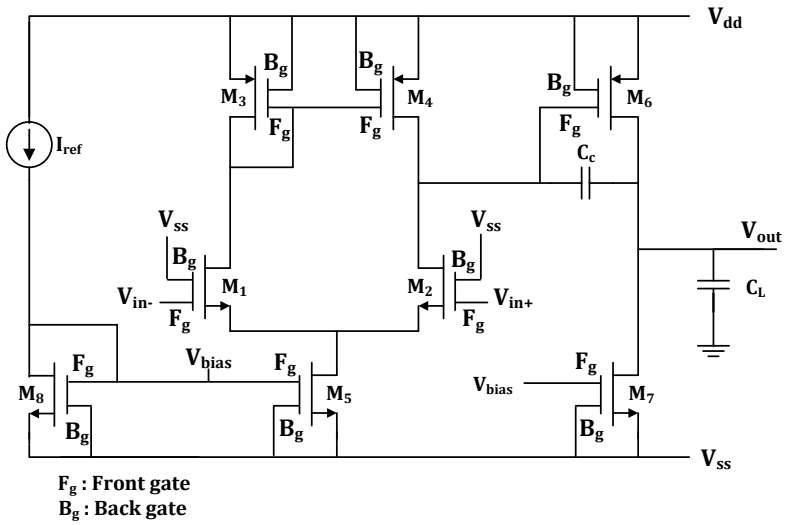


Fig. 2. Schematic of the DG-CMOS based two-stage OTA.

This circuit comprises eight MOSFETs, where each MOSFET are meant for accomplishing specific functions, such as M_1 and M_2 are used for differential gain, M_3 and M_4 are acting as current mirror load, M_5 and M_7 are forming biased-current sink, and finally, M_6 is a common source stage which is acting as a load or sink depending upon the charging or discharging of compensation capacitor C_c. This two-stage OTA topology segregates the gain and output-voltage swing requirement where the first stage provides high gain, while the second stage gives large swings. In this paper, a mostly used circuit of OTA [1] has been considered where the sizing of MOSFETs has been done through g_m/I_d methodology. Desired specifications of the OTA (as given in Table 1) have been taken from different sources [24−26], and mathematical calculations for each transistors ($M_1 - M_7$) have been proposed, to calculate MOSFET's sizing.

Table 1

Desired OTA specifications.

Specifications	**Value**
Technology	180 nm
Supply voltage	1.8 V
UGB	22 MHz
Open-loop DC gain (A_V)	78 dB
PM	60˚
CMRR	90 dB

Slew rate	20 V/µs
V_{iCMmin}	−0.1 V
V_{iCMmax}	0.8 V
Reference current (I_{ref})	20 µA
Load capacitor (C_L)	4 pF

An algorithm has been designed to automate the sizing procedure through MATLAB.

2.1 Compensation Capacitor (C_c)

Simplest frequency compensation technique uses the miller effect by connecting the C_c across the high gain stages. This consequence in pole-splitting which enhances the closed-loop stability [27]. The C_c governs the location of poles and zeros of the amplifier transfer function. To attain 60˚ PM the least possible value of C_c is [1]:

$$C_c \geq 0.22C_L, \tag{1}$$

where C_L is the load capacitance. Substituting the value of C_L in (1) gives the value of $C_c = 0.88$ pF. In this presented work $C_c = 1$ pF is considered.

2.2 Differential Gain Stage (M_1, M_2)

The differential gain stage is comprised of n-channel MOSFETs M_1 and M_2, which determines the gain of the first stage (A_{v1}) and UGB requirement. The transconductance of M_1 and M_2 is obtained as follows [1,2]:

$$\frac{g_{m1,2}}{2\pi C_c} \geq \text{UGB}. \tag{2}$$

Equation (2) yields $g_{m1,2}$=138.2 μS. Since the reference current I_{ref} splits equally between M_1 and M_2. So current flowing through them is $I_{d1,2}$=10 µA and g_m/I_d of M_1 and M_2 is:

$$\left(\frac{g_m}{I_d}\right)_{1,2} \approx 14 \text{ S/A}. \tag{3}$$

The desired DC gain considered is 78 dB. This gain is distributed among the two stages of OTA. The gain of the first stage considered is $A_{v1} = 40$ dB and that of second stage is $A_{v2} = 38$ dB. The gain of the first stage is given by [1]:

$$A_{v1} = \frac{g_{m1,2}}{g_{ds2}+g_{ds4}}, \tag{4}$$

which implies $g_{ds2}+g_{ds4} \leq 1.38$ μS. This inequality is shared equally by M_2 and M_4, i.e. $g_{ds2}=g_{ds4} \leq 0.69$ μS. The intrinsic gain of M_1 and M_2 is constrained by:

$$\left(\frac{g_m}{g_{ds}}\right)_{1,2} \geq 200. \tag{5}$$

Following the g_m/g_{ds} vs g_m/I_d plots for n-channel MOSFETs reported in [22] (for a parametric sweep of L =280 nm: 200 nm: 2.88 μm), at $(g_m/I_d)_{1,2}$ =14 S/A, the plot for $L_{1,2}$=880 nm gives the value $(g_m/g_{ds})_{1,2} \approx 223$, which satisfies the requirement in (5). The channel width is calculated using the I_d/W vs g_m/I_d plot in [22] (for L =880 nm). Using the values of $(g_m/I_d)_{1,2}$ and $L_{1,2}$ gives a current density =2.316 μA/μm, thus the width is given by:

$$W_{1,2} = \frac{I_{d1,2}}{(I_d/W)} \approx 4.31\ \mu\text{m}. \tag{6}$$

2.3 Common Source Stage ($\mathbf{M_6}$)

The current flowing in the second stage determines the transconductance of the p-channel MOSFET M_6. For 60˚ PM, g_{m6} can be determined using the relationship [1]:

$$g_{m6} = 2.2 g_{m1,2} \frac{C_L}{C_c}. \tag{7}$$

The value of g_{m6} is calculated as 1216.16 μS. To achieve slew-rate = 20 V/μs the current flowing through M_6 is kept as I_{d6} = 80 μA [28] which yields:

$$\left(\frac{g_m}{I_d}\right)_6 \approx 15\ \text{S/A}. \tag{8}$$

The gain of the second stage is given by:

$$A_{v2} = \frac{g_{m6}}{g_{ds6}+g_{ds7}}, \tag{9}$$

which implies $g_{ds6}+g_{ds7} \leq 15.20\ \mu$S. This inequality splits equally between M_6 and M_7, i.e. $g_{ds6}=g_{ds7} \leq 7.6\ \mu$S. The intrinsic gain of M_6 is constrained by:

$$\left(\frac{g_m}{g_{ds}}\right)_6 \geq 160. \tag{10}$$

From the g_m/g_{ds} vs g_m/I_d plot for p-channel MOSFETs in [22] (for a parametric sweep of L =230 nm: 100 nm: 1.93 μm), the selected channel length L_6 = 630 nm and from I_d/W vs g_m/I_d plot [22], the value of width is calculated as $W_6 \approx 160\ \mu$m. To keep the number of fingers N_f = 1, the maximum value of W_6 considered is 50 μm and so L_6 is re-calculated using the relation:

$$\frac{160\mu m}{0.630\mu m} = \frac{50\mu m}{L_6}. \tag{11}$$

The relation in (11) yields $L_6 \approx 0.196\ \mu$m.

2.4 Current Mirror Load (M_3, M_4)

The p-channel MOSFETs M_3, M_4, and M_6 form the load structure of the two-stage OTA. It is necessary that g_m/I_d of all these transistors are the same for perfect matching to avoid offset at the output of the first stage [28].

$$\frac{g_{m3,4}}{I_{d5}/2}=\frac{g_{m6}}{I_{d7}}. \tag{12}$$

Equation (12) yields $g_{m3,4}$ = 152.02 μS which results:

$$\left(\frac{g_m}{I_d}\right)_{3,4}\approx 15\text{S/A}. \tag{13}$$

The intrinsic gain of M_3 and M_4 is constrained by:

$$\left(\frac{g_m}{g_{ds}}\right)_{3,4}\geq 220. \tag{14}$$

From the g_m/g_{ds} vs g_m/I_d plots for p-channel MOSFETs in [22] (for a parametric sweep of L =180 nm: 100 nm: 1.98 μm), $L_{3,4}$ = 880 nm is selected. The $(g_m/I_d)_{3,4}$ is also constrained by the $V_{iCM,max}$. Applying KVL across the series of the branch (M_3−M_1−M_5) of Fig. 2, the related voltage equation is written as:

$$V_{dd}+V_{gs3,4}-V_{dsat1,2}-V_{dsat5}=0. \tag{15}$$

Since the transistor $M_{1,2}$ is in saturation, the $V_{dsat1,2}$ in (15) is written as:

$$V_{dsat1,2}=V_{gs1,2}-V_{th1,2}, \tag{16}$$

where $V_{th1,2}$ is the threshold voltage of $M_{1,2}$. Substituting $V_{dsat1,2}$ in (15):

$$V_{dd}+V_{gs3,4}-(V_{gs1,2}+V_{dsat5})+V_{th1,2}=0. \tag{17}$$

Since $V_{gs1,2}+V_{dsat5}=V_{in(-)}$, the final expression for (15) is obtained as:

$$V_{dd}+V_{gs3,4}-V_{in(-)}+V_{th1,2}=0. \tag{18}$$

Substituting $V_{in(-)}=V_{iCM,max}$ in (18) gives the inequality for $V_{iCM,max}$ that can be applied before driving the input pair transistors M_1 and M_2 into the saturation region.

$$V_{iCM,max}\leq V_{dd}+V_{gs3,4}+V_{th1,2}. \tag{19}$$

$V_{th1,2}$ is extracted from the V_{th} vs g_m/I_d plot [22] (for L=880 nm), which is ≈ 0.4915 V. Substituting in (19), the lower bound of $V_{gs3,4}$ is found as:

$$V_{gs3,4}\geq -0.5915\text{V}. \tag{20}$$

By using V_{gs} vs g_m/I_d plot [22] (for L =880 nm), the valid range of $(g_m/I_d)_{3,4}$ due to $V_{iCM,max}$ specification is found as:

$$\left(\frac{g_m}{I_d}\right)_{3,4} \geq 11.4\text{S/A}. \tag{21}$$

As a compromise, $(g_m/I_d)_{3,4}$ = 15 S/A is selected which satisfies both (13) and (21) with adequate margin. The width of $W_{3,4}$ is selected from the I_d/W vs g_m/I_d plot [20], where $(I_d/W)_{3,4} \approx 0.3569\ \mu$A/$\mu$m, thus $W_{3,4} \approx 29\ \mu$m.

Biased-Current Sink ($\mathbf{M_5}$, $\mathbf{M_7}$)

The transistor M_5 sinks the current through differential pair. The size of M_5 is constrained by the PSRR, CMRR, and minimum common-mode input voltage ($V_{iCM,min}$) requirements. The g_{m5} is calculated from the PSRR using the relation [28]:

$$\text{PSRR} = \frac{A_v}{g_{m5}R_{02}}, \tag{22}$$

where $R_{02} = 1/(g_{ds6} + g_{ds7})$. Substituting the required value of PSRR from Table 1 in (22) gives the value g_{m5}=190 μS. The CMRR is given by :

$$\text{CMRR(dB)} = A_{vdc}\text{(dB)} - A_{vdc,CM}\text{(dB)}, \tag{23}$$

where $A_{vdc,CM}$ is the common-mode DC gain. Substituting the data from Table 1 in the following constraint will give the limit of g_{ds5}.

$$A_{vdc,CM} = \frac{2g_{m1,2}g_{ds5}}{2g_{m1,2}+g_{ds5}} \cdot \frac{1}{2g_{m3,4}} \cdot A_{v2} \leq -12\text{dB} \approx 0.251. \tag{24}$$

Therefore, the output conductance of M_5 must satisfy $g_{ds5} \leq 0.94\ \mu$S. The current flowing through M_5 is I_{d5}= 20 μA which yields:

$$\left(\frac{g_m}{I_d}\right)_5 \approx 10\ \text{S/A}. \tag{25}$$

The intrinsic gain is constrained by :

$$\left(\frac{g_m}{g_{ds}}\right)_5 \geq 202. \tag{26}$$

From the g_m/g_{ds} vs g_m/I_d plot for n-channel MOSFETs in [22] (parametric sweep of L =180 nm: 200 nm: 2.98 μm), the selected channel length L_5 = 1.18 µm. The $V_{iCM,min}$ that can be applied before driving the M_5 into saturation region is constrained by:

$$V_{iCM,min} \geq V_{gs1,2} + V_{dsat5} + V_{ss}. \tag{27}$$

Here, $V_{gs1,2}$=0.5898 V (for L = 880 nm). Substituting the required values in (27), the constraint on V_{dsat5} is written as:

$$V_{dsat5} \leq 0.213\text{V}. \tag{28}$$

By using V_{dsat} vs g_m/I_d plot [22] (for L =1.18 μm), the valid range of g_m/I_d due to the input range specification can be written as:

$$\left(\frac{g_m}{I_d}\right)_5 \geq 9.076 \text{ S/A}. \tag{29}$$

As a compromise, g_m/I_d = 10 S/A is selected which satisfies the requirements (25) and (29) with adequate margin. The width of M_5 is selected from the n-channel MOSFET current density plot [22], where $(I_d/W)_5 \approx 4.98\ \mu$A/$\mu$m, thus $W_5 \approx 4.06\ \mu$m. To determine the size of M_7, we consider the ratio:

$$\frac{I_{d7}}{I_{d5}} = \frac{(W/L)_7}{(W/L)_5}. \tag{30}$$

Substituting the required values in (30), the aspect ratio for M_7 is obtained as $(W/L)_7 \approx 14$. Considering L_7=1.18 μm, the width for M_7 is evaluated as $W_7 \approx 16.24\ \mu$m.

Proposed Algorithm for Sizing Procedure

While designing an analog amplifier, the performance of the circuit is controlled by the size of MOSFETs. The systematic sizing procedure using g_m/I_d methodology has been presented so far evaluates the transistor's dimensions by solving mathematical equations using data extracted from graphical models. Regardless of the merit of graphical models, it experiences various drawbacks. First, it is time taking and has to be repeated many times if there is any change in the desired specifications. Second, if the circuit fails to achieve the desired specifications, the sizes have to be re-evaluated. Since the sizing procedure is structured and can be easily retraced, it fits well to automation. Considerable time can be saved by automating the sizing procedure. A MATLAB program is written, where data from graphical models are stored in the form of arrays. For every g_m/I_d value in the array, the program finds for the minimum channel length of transistors which satisfies the desired specifications. The procedure has been coded as per the flowchart as shown in Fig. 3.

3. Results and Discussion

The sizes of the MOSFETs constituting the OTA have been evaluated through solving the graphical models [22] by g_m/I_d methodology and simulated the design in Cadence-spectre using gpdk 180-nm technology. Table 2 summarizes the size of MOSFETs and the current flowing through each transistor in both CMOS (BSIM3v3) and DG-CMOS (BSIM-IMG) OTAs. The DG-CMOS OTA is simulated by connecting the back gates of p-and n-channel UTBSOI transistors to V_{dd} and V_{ss} terminals, respectively [Fig. 2].

3.1 Simulation Results

The designed OTAs have been simulated under a supply voltage of 1.8 V (V_{dd} = 0.9 V, V_{ss} = −0.9 V) and the characteristics in open-loop and unity-gain configurations are examined. The term open-loop indicates that there exists no connection between the input and output terminals of the amplifiers. The valid output-voltage swing observed from DC analysis is ≈−0.9 to 0.89 V for both the OTAs, as shown in Fig. 4.

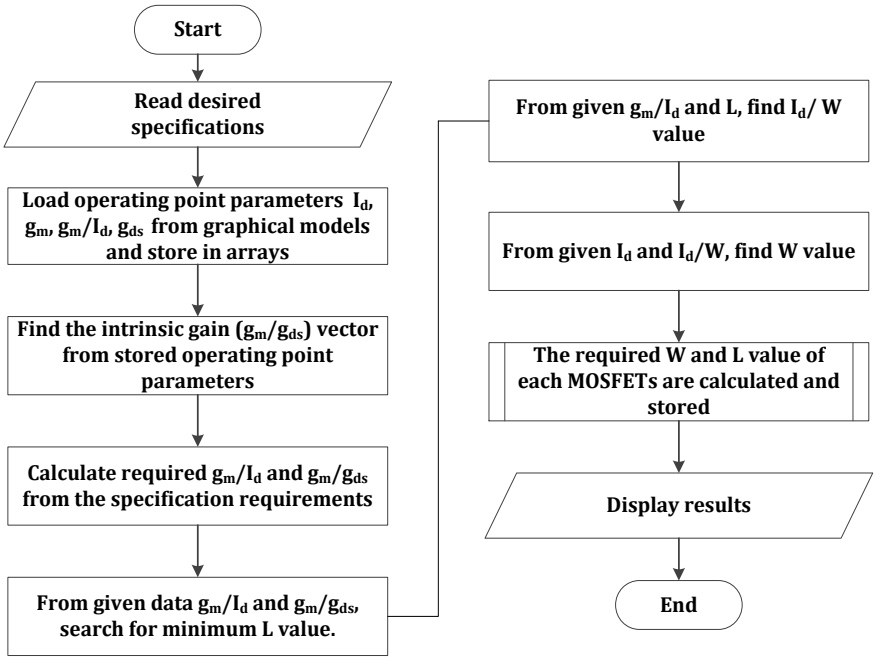


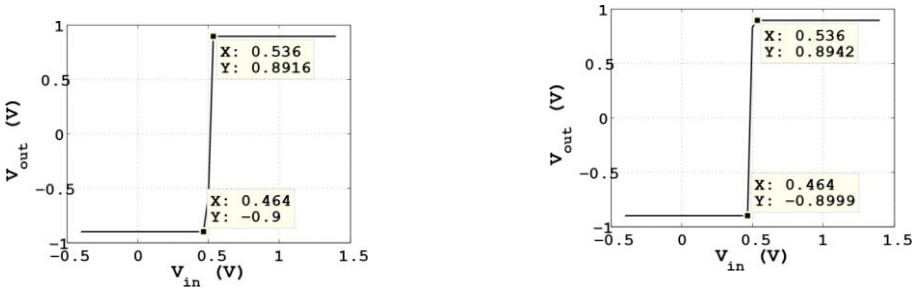
Fig. 3. Flowchart representing the algorithm of design automation procedure

Table 2

Summary of OTA transistor sizing and current through each transistor

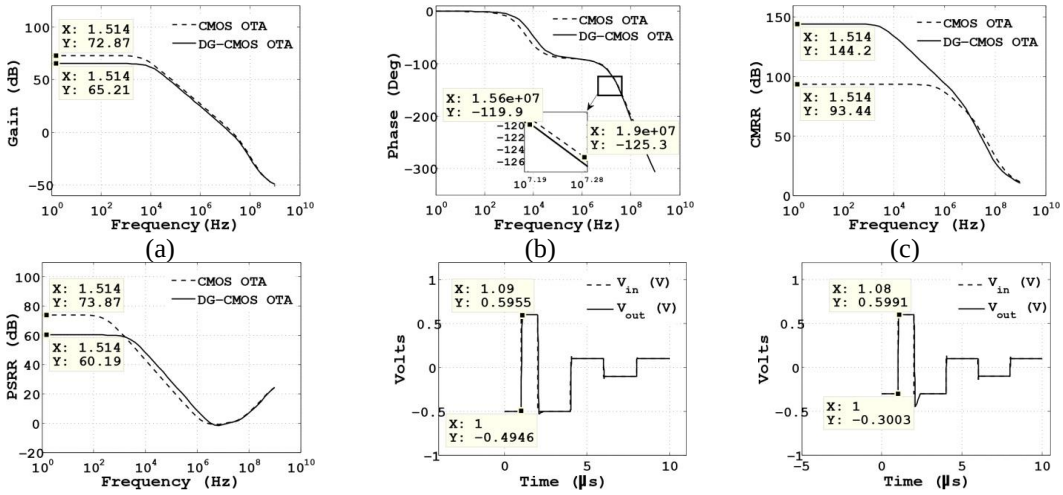
MOSFETs	g_m/I_d (S/A)	L (μm)	W (μm)	CMOS-OTA (μA)	DG-CMOS OTA (μA)
M_1, M_2	14	0.88	4.31	10.00	10.03
M_3, M_4	15	0.88	29.0	10.00	10.03
M_5	10	1.18	4.06	20.01	20.07
M_6	15	0.63	50	85.03	80.97
M_7	–	1.18	16.24	85.03	80.85
M_8	–	1.18	4.06	20.00	20.12

Various characteristics of the OTAs obtained from the AC analysis of open-loop, and unity-gain configurations are shown in Fig. 5. Parameters obtained from the simulation of the open-loop configuration are shown in Fig. 5(a−c).



(a) (b)

Fig. 4. Output voltage swing of (a) CMOS OTA, (b) DG-CMOS OTA.



(a) (b) (c)

(d) (e) (f)

Fig. 5. Simulation results showing (a) open-loop DC gain, (b) phase, (c) CMRR, (d) PSRR, unity-gain transient response of (e) CMOS OTA, (f) DG-CMOS OTA.

3.2 Applications

The DG-CMOS OTA has been tested by using it in the active differentiator and integrator circuits [31] which are widely useful in the analog signal processing applications. The values R=1.59 kΩ, C=0.1μF are chosen so as to generate unity-gain frequency (f_u=1/2πRC) of 1 KHz. The circuits are tested by applying sinusoidal and square wave voltage of different frequencies (f) as shown in Fig. 6. A good differentiation, as well as integration action is clearly seen from the simulation results, which imply that the UTBSOI transistors can be successfully used to design the analog circuits. The applications of the DG-CMOS OTA has also been extended to active filters [32] in which the OTA is used for amplification and gain control. Fig. 7 (a) shows the first-order low-pass filter having cut-off frequency (f_c=1/2πR$_F$C$_F$) of 795.77 Hz with component values R= 20 kΩ, C_F = 1 nF, and R_F = 200 kΩ. The gain vs frequency plot in Fig. 7(c) clearly

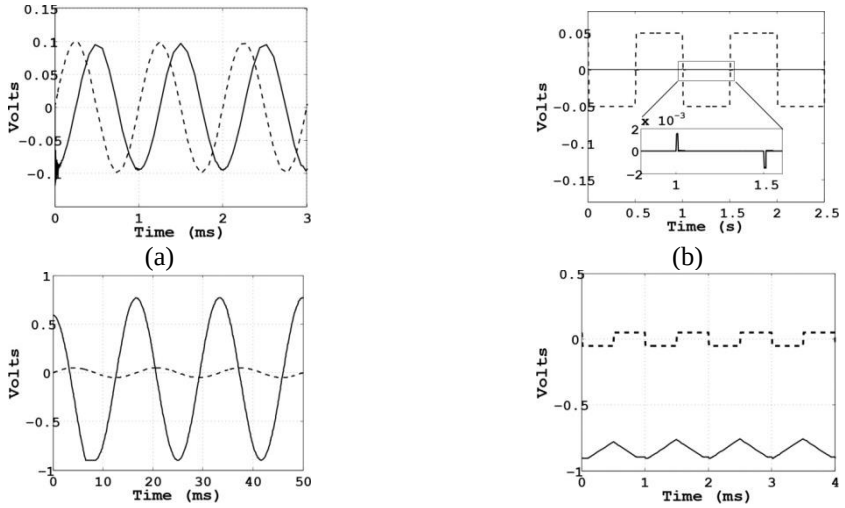


Fig. 6. Transient responses showing applications of the DG-CMOS OTA in (a) differentiator with sinusoidal input voltage of amplitude 100 mV at f = 1 KHz, (b) differentiator with square-wave input voltage of amplitude $\pm$50 mV at f = 1 Hz, (c) integrator with sinusoidal input voltage of amplitude 50 mV at f = 60 Hz, (d) integrator with square-wave input voltage of amplitude ±50 mV at f = 1 KHz. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively.)

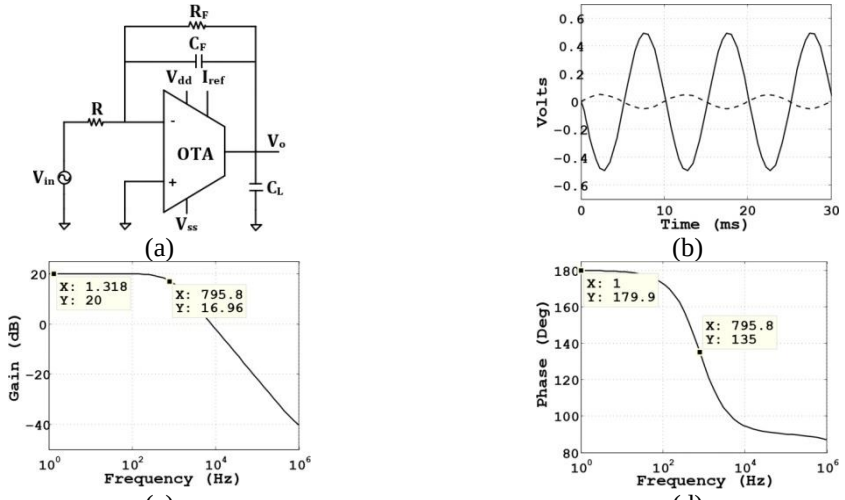


Fig. 7. Application of the DG-CMOS OTA in (a) active low-pass filter, (b) transient response with a sinusoidal input voltage of amplitude 50 mV at f = 100 Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

The extracted value of DC gain, CMRR, PM and UGB of the CMOS OTA are 72.8 dB, 93.4 dB, 54.5˚, and 19.0 MHz, respectively. The same parameters for the DG-CMOS OTA are obtained as 65.2 dB, 114.2 dB, 60˚, and 15.6 MHz, respectively. Simulation results revealed that the DG-CMOS-OTA has resulted in high CMRR value (= 144.2 dB). The power consumption is calculated using the relation: $Power = (I_{d5}+I_{d6})(V_{dd}-V_{ss})$ [1], with I_{d5} and I_{d6} are current through M_5 and M_6, respectively. The parameters such as PSRR, slew-rate, and V_{iCMR} are extracted from the unity-gain configuration. In this configuration, the OTA draws a very small current without disturbing the original circuit and has a voltage gain of unity. Simulation results of the unity-gain configuration are shown in Fig. 5(d−f). Slew-rate of both OTAs has been calculated from the unity-gain transient response, as shown in Fig. 5(e) and (f) which are obtained as 12.11 V/μs and 11.24V/μs for the CMOS and DG-CMOS OTAs respectively. A summary of the simulation results of the OTAs is listed in Table 3.

Table 3

Performance comparison with prior reported works

Specifications	**[8]**	**[10]**	**[11]**	**[12]**	**[13]**	**[28]**	**[29]**	**CMOS OTA**	**DG-CMOS**
Technology (nm)	180	180	130	180	180	180	180	180	180
Supply voltage (V)	1.8	1.2	1.2	1.8	1.8	1.8	1.8	1.8	1.8
Load capacitor (pF)	1.75	15	1	5.6	5.6	1	5	4	4
UGB (MHz)	160	20	4.8	187	134.2	660	88.9	19.0	15.6
PM (˚)	–	63	57	80	70.6	73	98.7	54.5	60
DC gain (dB)	74	111	52	83	60.9	80	82.7	72.8	65.2
Slew rate (V/μs)	26.7	29.5	5	74	94.1	800	8.67	12.19	11.24
$V_{iCM,min}$ (V)	–	–	–	–	–	–	–	–0.07	0
$V_{iCM,max}$ (V)	–	–	–	–	–	–	–	– 0.88	0.88
V_{out} swing	–	–	–	–	–	–	–	– 0.9, 0.89	– 0.9, 0.89
CMRR (dB)	–	145	–	–	–	–	127	93.4	144.2

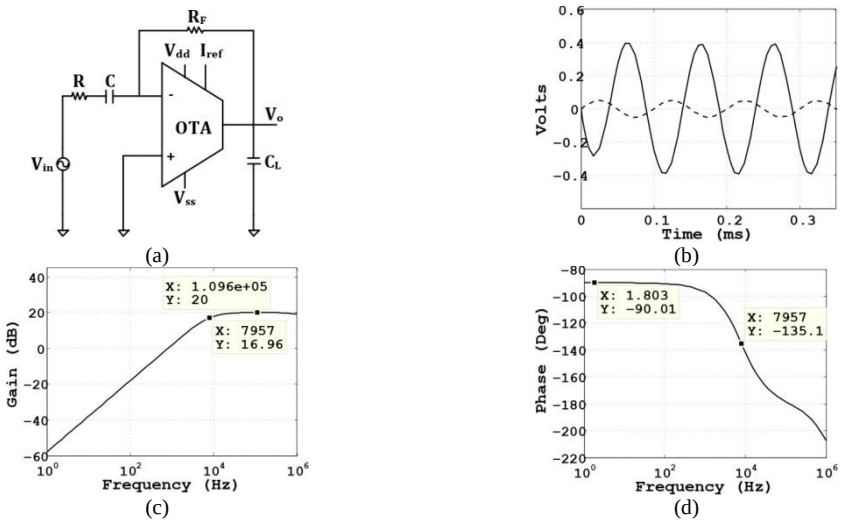


Fig. 8. Application of the DG-CMOS OTA in (a) active high pass filter, (b) transient response with a sinusoidal input voltage of amplitude 50 mV at f =10 KHz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

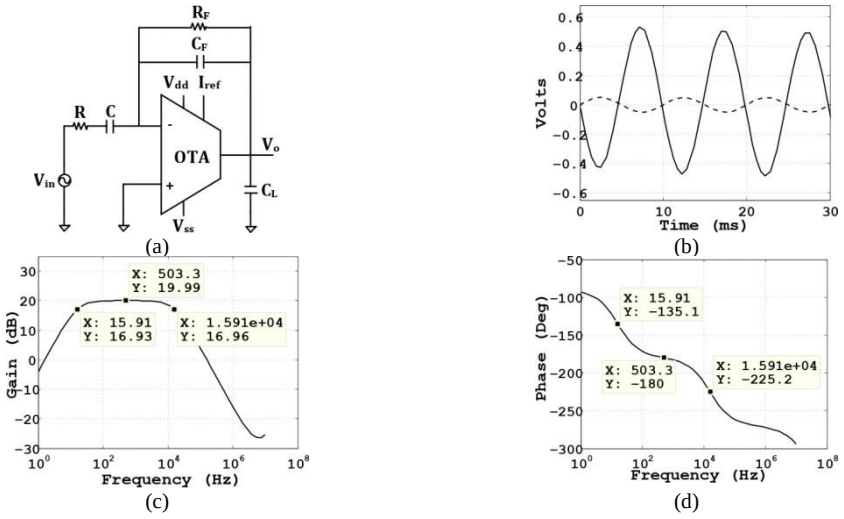


Fig. 9. Application of the DG-CMOS OTA in (a) active band pass filter, (b) transient response with a sinusoidal input voltage of amplitude 50 mV at f = 100 Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

4. Conclusions

In this paper, low power and high CMRR two-stage CMOS and DG-CMOS OTA have been reported. The size of the MOSFETs has been evaluated mathematically and graphically though g_m/I_d methodology to build up such OTA.

A new algorithm has been proposed to verify the MOSFETs sizing. Simulation is performed in Cadence-spectre where BSIM3v3 and BSIM-IMG models have been adopted for MOS and UTBSOI devices. The amplifier is able to show optimum performance, thereby balancing the trade-off between various desired specifications. Open-loop and unity-gain configurations are simulated accordingly to show a comparative analysis between the CMOS and DG-CMOS based OTAs. The CMOS OTA has higher DC gain over the DG-CMOS based OTA, whereas, from the viewpoint of CMRR and PM, the DG-CMOS OTA is superior to CMOS OTA. Observation tables offer that in sub-micron regime (180-nm), UTBSOI transistors can be successfully used to design the analog circuits. Moreover, the DG-CMOS OTA has been verified by using it in differentiator, integrator, and active filter circuits which can show the desired output successfully. Since the process-design kit for the UTBSOI is not available in the existing simulators, so the layout design of the device is an issue. Thus, ideas for creating the process-design kit would be a welcoming research topic to improve the results of analog and mixed-signal circuits further.

Acknowledgments

The authors would like to thank Dr. Shubankar Majumdar, Assistant professor, and Gudmalwar Ashishkumar Prabhakar, Research scholar from the Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, India for their help and useful suggestions. This work was supported in part by the National Institute of Technology Meghalaya and in part by Visvesvaraya PhD Scheme, Government of India.

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