A NOVEL MODULAR SYMMETRICAL MULTILEVEL CONVERTER WITH REDUCED NUMBER OF CIRCUIT DEVICES

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In this paper a novel symmetric multilevel converter structure based on cascaded converter family is proposed. This inverter is likely to be used in low/medium voltage applications. The proposed topology is analyzed and then compared with conventional multilevel cascade converters. Comparison depicts the proposed inverter superiority over the conventional inverters. In this topology, all the desired voltage levels can be obtained using a lower number of devices. The suggested multilevel converter reduces the requirements for circuit elements including switches and their gate drivers. As a result, the total cost is significantly reduced and the control scheme is simpler. Both the simulation and experimental results are provided to demonstrate the practicability and the good performance of the suggested converter. The simulation and experimental results are in good agreement which shows the effectiveness of the proposed inverter.

Keywords: Multilevel Voltage Source Inverter, Symmetric Inverter, Reduction of Circuit Components, cascaded multilevel converter

1. Introduction

Ever increasing attention has been paid on multilevel structures since introduced early in 1980s [1]. Multilevel inverter is used in most of applications because of higher power quality, higher voltage capability, lower harmonic components, better electromagnetic compatibility, higher amplitude of fundamental component, lower switching losses and lower dv/dt. These advantages are due to the staircase waveform of the output voltage. In other words, the key goal of the multilevel inverters is generating output voltage similar to sinusoidal waveform by synthesizing DC input voltages [2, 3]. As the number of levels increases, these merits will be ameliorated. Related to the inverter circuit topologies, the DC sources can be interconnected or isolated [4]. Multilevel

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inverter proved to be one of the significant enabling technologies in flexible AC transmission systems devices [5] and renewable energy resources [6]. Since the initial multilevel inverter has been introduced, several modulation techniques have been developed aiming to increase the quality of the output voltage waveform. The multilevel inverters output voltage waveform is commonly controlled by PWM [7] and SVPWM [8] methods enabling to generate the desired voltage. The multilevel inverter structures are mainly classified in three groups: diode clamped (DCM), flying capacitor (FCM) and cascaded (CHB) multilevel inverters. Despite all the mentioned merits, multilevel inverters have some disadvantages over the traditional two-level structure. In multilevel topologies, an increase in the number of levels results in an increase of the circuit intricacy, which reduces the efficiency and reliability [9-10]. Diode-clamped inverters face with some challenges. While increasing the number of levels, the difficulty to preserve the voltages of DC capacitors balanced increases as well. This voltage imbalance can be the result of many factors such as load power factor, operational conditions and the control technique used. To overcome the mentioned problem, several procedures have been suggested [11]. In flying capacitor, the control scheme upholds the voltage levels of used capacitors at their target values [12]. Among the mentioned topologies, the cascaded multilevel inverter is distinguished because of its modularity, easier controllability and higher reliability. The cascaded multilevel inverters employ several H-bridge units' series connections. Each unit has one DC source and four unidirectional switches and can generate a three-level staircase waveform. The total voltage of the cascaded multilevel inverter is the sum of all bridges output voltages. The major demerits associated with cascaded multilevel inverters, are their circuit complexity requiring a high number of power switches and a great number of auxiliary DC voltages provided either by independent supplies or, more commonly, by a bulky array of capacitive voltage splitters [13]. The high number of components in cascaded inverters is the main concern which in the advanced topologies is considered to be lower. Therefore, reducing the number of circuit devices is the main concern from the point view of design and a lot of efforts have been done by researchers to satisfy this requirement. Several developed topologies have been reported in papers [14, 18]. In this paper a novel symmetric cascaded based multilevel converter is proposed. The proposed topology is analyzed and then comparison is done between the suggested multilevel converter and other conventional converters. The comparison results present the advantages of this modular topology. The number of switches and gate drivers is reduced in the suggested converter. Simulation results are analytically depicted and the results of an implemented prototype of proposed multilevel converter are presented to show the effectivity of the new topology.

2. Suggested topology

Many various topologies have been presented for multilevel inverters. Some of the topologies use isolated DC voltage sources with different values (asymmetric topology) to achieve more output voltage levels. However, providing DC voltage sources with different values can be very costly making the topologies difficult to be realized. But, in the symmetric multilevel inverters, the value of all DC voltage sources are equal leading to easier realization possibility and lower design cost. However, the symmetric topologies can produce lower number of voltage levels in comparison with the asymmetric topologies. Here, in this paper, a novel symmetric multilevel modular cascade converter is proposed.

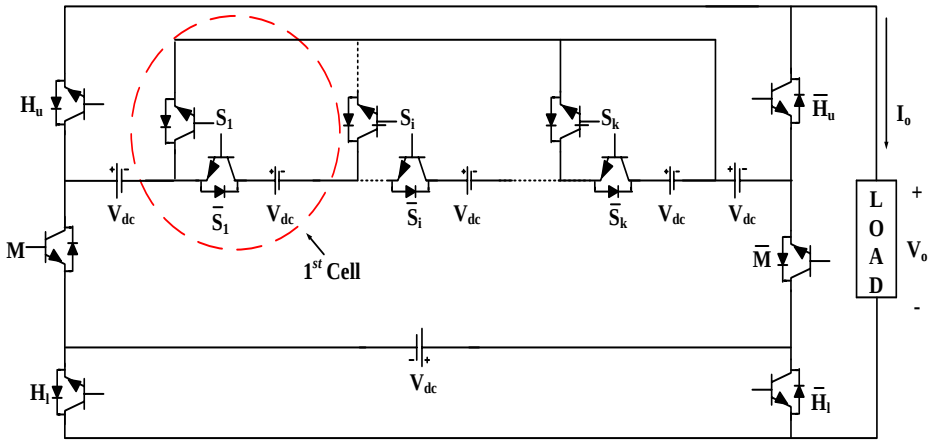


Fig. 1. Proposed multilevel inverter

As illustrated in Fig. 1, the proposed inverter consists of n-isolated DC voltage sources. Because of viability of several isolated DC sources, renewable energy sources such as photovoltaic (PV) panels or fuel cells are such systems where the proposed inverter is suitable to be used. Also, several DC sources can be available with energy storage devices such as capacitors or batteries. Also, when AC voltage is already available, multiple DC sources can be generated using isolated transformers and rectifiers [19]. It's notable that the proposed inverter is a symmetric inverter, so the required DC voltage sources must have the same value. Inequality in DC voltage sources values may impose inverse effect on the output voltage quality and the voltage levels will not be equal, introducing some undesired harmonics in the output voltage. However, it must be mentioned that, providing the balanced DC voltage sources is the same issue for all the symmetric inverters. In some cases, additional circuits are required to be added to symmetric inverters in order to provide the equal DC voltages. For instance, if the PV cells are employed as DC voltage sources, they are already equipped with

DC/DC converters for maximum power point tracking and voltage level adapting goals. Despite the above discussion, the undesired changes in the DC voltage sources can be compensated by complementary modulation strategies [20, 21]. The implementation of these methods needs to manipulate the inverters hardware, by adding some extra devices and circuits, and makes the control scheme more intricate. As the aim of this study is to propose a new topology for the multilevel inverters, the modulation method to compensate the variations of the DC voltages is not taken into account for analysis and comparison. As shown in Fig. 1, the proposed inverter is composed by k-cells. The basic cell of the suggested multilevel structure is illustrated in Fig. 2. This structure contains one DC voltage source and two semiconductor unidirectional switches. As noted before, the values of the DC sources are equal. Each unidirectional switch includes an IGBT and an anti-parallel fast recovery diode.

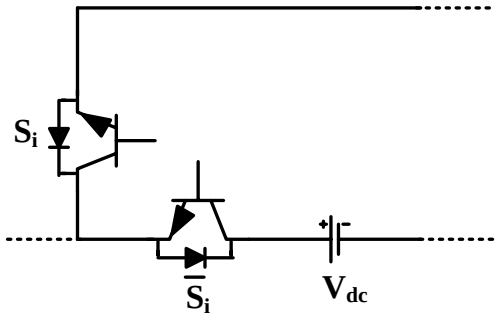


Fig. 2. Basic Cell of Proposed Topology

As deduced from this figure, to prevent short circuit occurrence, the left and bottom corresponding switches should not be turned on simultaneously. So, the switches S_i and $\overline{S_i}$ are controlled in complementary manner. The proposed inverter can generate any specific value of the output levels. An output phase voltage is synthesized by individual voltages of the DC sources. In this study, the same value (V_{dc}) is considered for all the DC voltage sources. Therefore, the proposed topology is called symmetric topology. So, the maximum voltage will be obtained in the output equal to the sum of DC sources amplitudes. Equation (1) represents the maximum output voltage ($V_{o,\max}$) of the proposed topology:

$$V_{o,\max} = \sum_{i=1}^{n} V_i = nV_{dc} \tag{1}$$

where *n* is the number of DC sources.

A typical output voltage of the proposed multilevel inverter is shown in Fig. 3. The output voltage levels from $-nV_{dc}$ to $+nV_{dc}$ can be produced using the different permissible switching combinations of the proposed multilevel inverter.

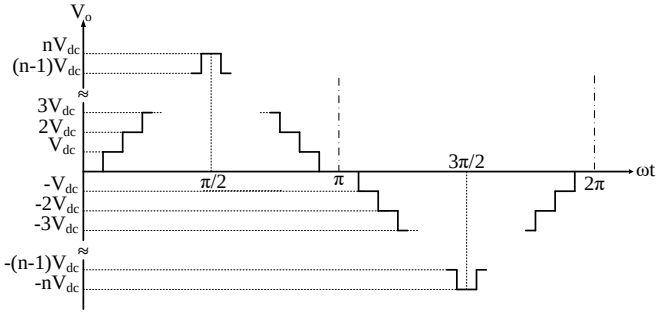


Fig. 3. Typical output voltage of the proposed multilevel inverter

The number of voltage levels (m) is given by the following expression:

$$m = 2\frac{V_{o,\max}}{V_{dc}} + 1 \tag{2}$$

It's obvious that, to generate m-levels in output voltage, n DC sources are needed, where

$$n = \frac{m-1}{2} \tag{3}$$

As discussed before, the proposed inverter includes several cells. In order to increase the output levels to a specific value, the number of cells must be increased. Since each cell includes one DC voltage source, with n DC power supplies k basic cells are necessary, where

$$k = n - 3 \tag{4}$$

The number of switches in the proposed inverter can be obtained from equation (5) :

$$N_{Switch} = 2n \tag{5}$$

The required switching control pulses for the N_{Switch} switches are produced by the N_{Driver} related driving circuit.

$$N_{Driver} = N_{Switch} \tag{6}$$

One important problem in the multilevel inverters is the voltage ratings of switches. The PIV of all switches is calculated by the equation (7):

$$PIV = \sum_{j=1}^{N_{Switch}} PIV_{Switch_j} \tag{7}$$

3. Traditional CHB and suggested inverters in [14-18]

Fig. 4 presents the complete view of the conventional multilevel converters. These inverters are selected to be used in a comparison study. As shown in Fig. 4,

all the mentioned multilevel inverters consist of n DC voltage sources (their voltage values are equal to V_{dc}). So, the total voltage of all mentioned multilevel inverters is the sum of all DC links. In this regard the maximum output voltage and the output voltage level are nV_{dc} and $2n+1$, respectively.

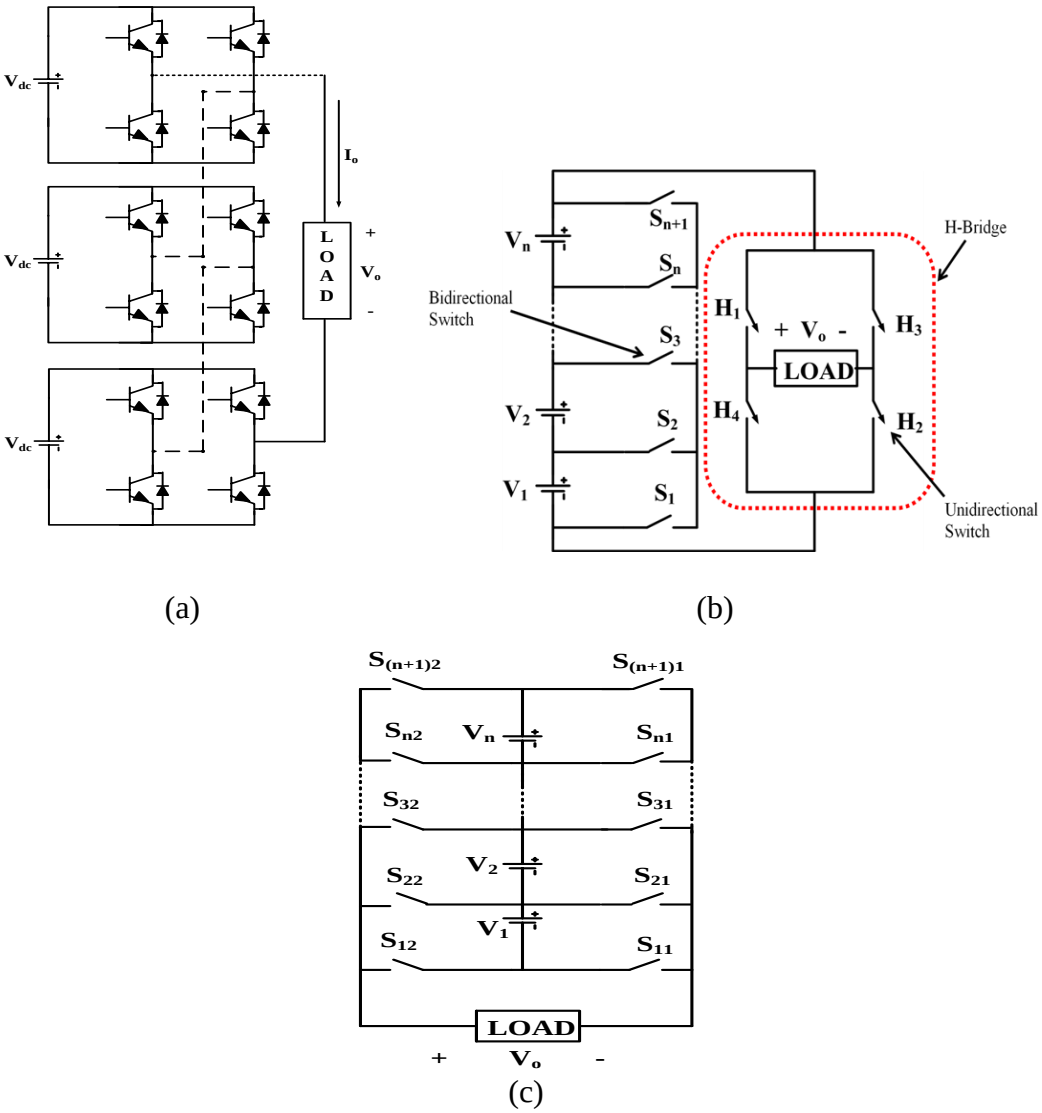


Fig. 4. Multilevel inverters a) Typical CHB inverter, presented inverters in b) [14], c) [15]

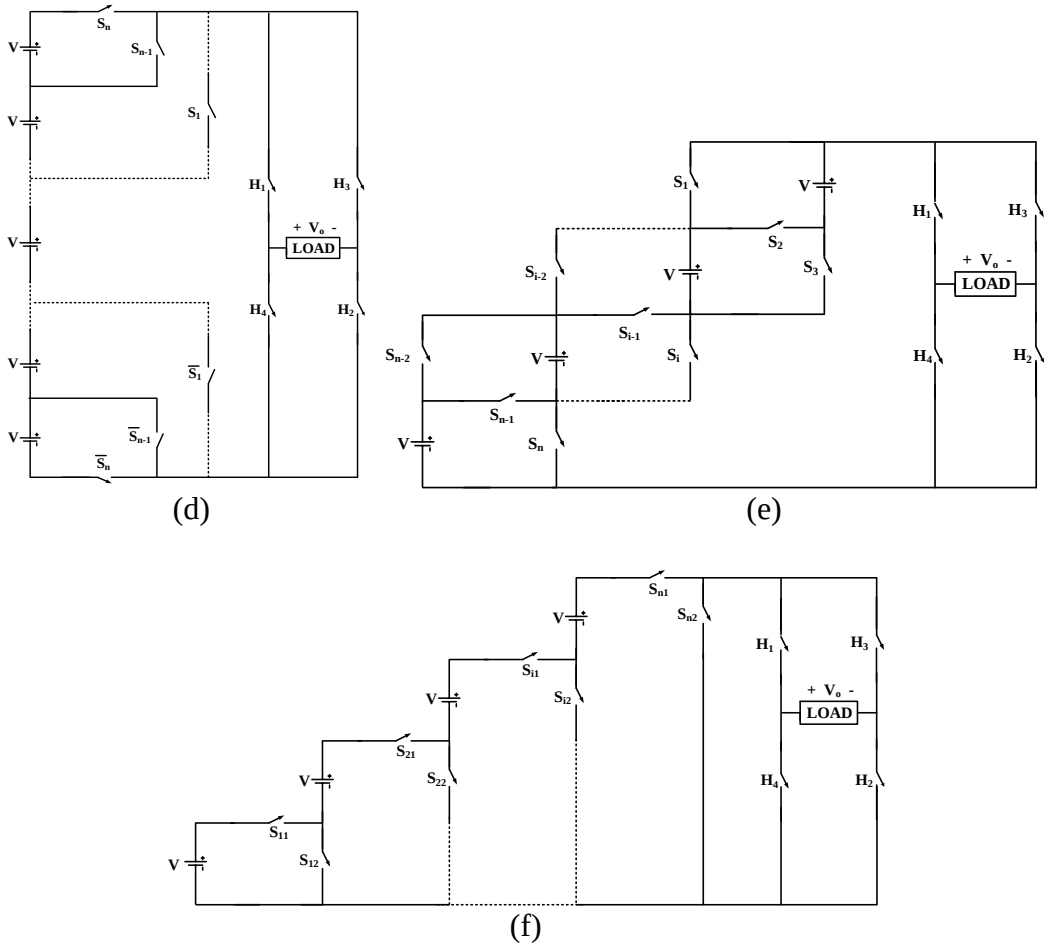


Fig. 4. Multilevel inverters: d) [16], e) [17], and f) [18]

Unidirectional switch Bidirectional switch

Fig. 5. Schematic of unidirectional and bidirectional switches

As shown, the multilevel inverters presented in Fig. 4 (a)-(e) and (f) use unidirectional switches in their topology, whereas the other ones have both unidirectional and bidirectional switches. Bidirectional switches have the capability of blocking voltage and conducting current in both directions. The schematic view of both unidirectional and bidirectional switches is shown in Fig. 5. These arrangements are used in this study.

4. Comparison of the proposed topology with other mentioned topologies

The purpose of this section is the comparison of imperative quantities between the suggested multilevel converter, symmetric CHB and the traditional multilevel converter presented in [14, 18] using the same DC power supplies in both magnitudes and number. To have the same condition, the number of DC voltage sources is equal to n and the value of each DC source is V_{dc}. In this regard the maximum output voltage and the number of output voltage levels are nV_{dc} and $2n+1$, respectively. By supposing that one bidirectional switch includes two unidirectional switches, the comparison is provided. As a result, the number of switches in the proposed inverter is lowest compared to the inverters shown in Fig. 4. Another essential parameter which influences the overall inverter expense is the voltage ratings of the power switches. It's apparent that the ratings of switches applied in low/medium voltage applications have almost the equal value. So, the number of required power switches is more important than the rating of power semiconductor switches in low/medium voltage applications. As clarified before, the proposed inverter is appropriate for low/medium voltage applications. So, taking into account the advantages detailed for the proposed inverter and the nature of the applications where the proposed inverter will be utilized in, a small increase in total PIV of the overall system compared to the traditional CHB inverter can be neglected while a considerable reduction in switches is achieved. The proposed inverter requires a reduced number of switches, so the suggested topology needs fewer related gate drive circuits. Therefore, using less components results in the reduction of the required installation area and of the inverter cost. It makes also, the control scheme easier. Fig. 6 shows the number of IGBTs versus the number of voltage levels. As the figure clearly shows, for any level specific value, the proposed topology uses a lower number of IGBTs in comparison with other mentioned topologies. The comparison of PIV value versus the number of voltage levels is shown in Fig. 7 considering the proposed symmetric topology, CHB and those presented in [14, 18]. As the figure shows, for any specific value of the level, the proposed topology has lower PIV in comparison with structures presented in [14-15, 18]. Also, the PIV value of the proposed inverter is mostly lower or keeps close to the inverters PIV reported in [16, 17]. As clarified before, a small increase in total PIV of overall system compared to the CHB can be neglected while a considerable reduction in circuit devices is achieved in the proposed topology. In this regards, more PIV can not detract from the values of the proposed inverter.

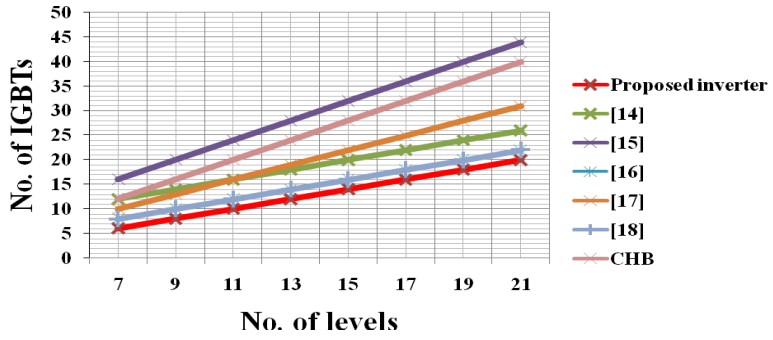


Fig. 6. The number of IGBTs versus output voltage levels for proposed and other multilevel inverters

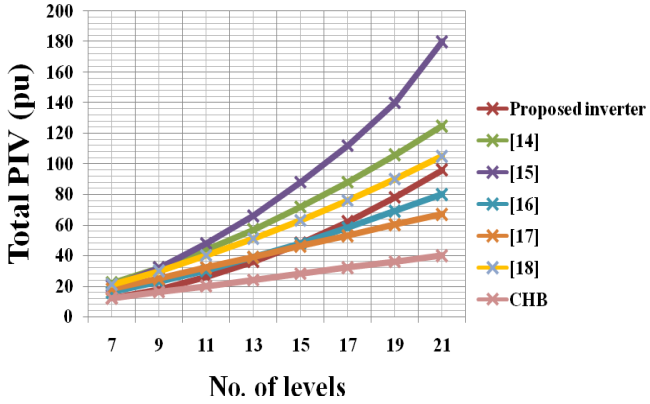


Fig. 7. Total PIV versus output voltage levels for proposed and other multilevel inverters

5. Simulation and experimental results

In order to validate the feasibility of the proposed inverter, simulation studies are provided. Fig. 8 shows the 13-level novel symmetric multilevel cascade converter; it has six DC sources, so n=6 and number of IGBTs according to (5) is 2n which yields 12 IGBTs. The switching states of 13-level proposed converter are illustrated in Table 1 to make the operational principle of DC-AC multilevel converter much more comprehensible. The switch is ON when its state is 1 and is OFF when its state is 0. It can be deduced from Table. 1, that the redundancy (the number of combinations to obtain a desired voltage level) is possible in output levels.

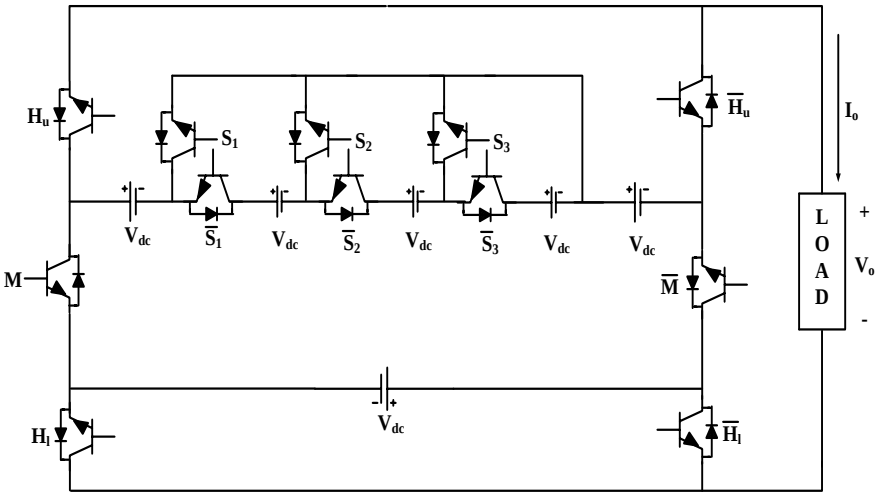


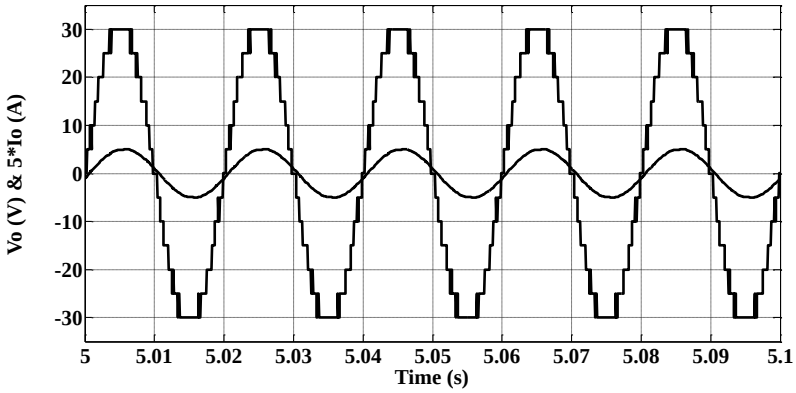
Fig. 8 The schematic of 13-level novel symmetric proposed multilevel converter

Table 1

Switching states of proposed symmetric 13-level inverter

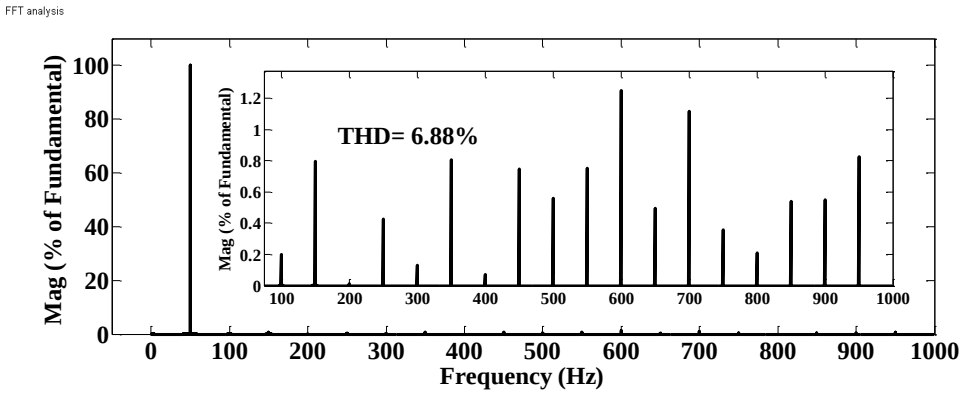
Output Voltage	H_l M S_1 S_2 S_3 H_u
$6V_{dc}$	1 0 0 0 0 1
$5V_{dc}$	0 0 0 0 0 1/1 0 0 0 1 1
$4V_{dc}$	1 0 0 1 - 1/0 0 0 0 1 1
$3V_{dc}$	1 0 1 - - 1/ 0 0 0 1 - 1
$2V_{dc}$	0 0 1 - - 1
V_{dc}	1 0 - - - 0
0	0 0 - - - 0/ 1 1 - - - 1
$-V_{dc}$	0 1 - - - 1
$-2V_{dc}$	1 1 1 - - 0
$-3V_{dc}$	0 1 1 - - 0/1 1 0 1 - 0
$-4V_{dc}$	0 1 0 1 - 0/1 1 0 0 1 0
$-5V_{dc}$	1 1 0 0 0 0/ 0 1 0 0 1 0
$-6V_{dc}$	0 1 0 0 0 0

Fig. 9 (a) shows the simulation results of the output voltage and current for the 13-level proposed symmetric topology under RL load. In the simulation results the DC voltage sources are considered 5V. Therefore, the output voltage waveforms consist of 5V steps. Fig. 9 (b) shows the THD analysis and the magnitudes of different output voltage harmonic components. A series R–L (20 Ω and 18mH respectively) are considered as load parameters.



(a) Output voltage and current

Fig. 9 a) Simulation results of output voltage and current for the 13-level proposed symmetric topology



(b) THD and FFT analysis of output voltage

Fig. 9 b) Simulation results of output voltage and current for the 13-level proposed symmetric topology

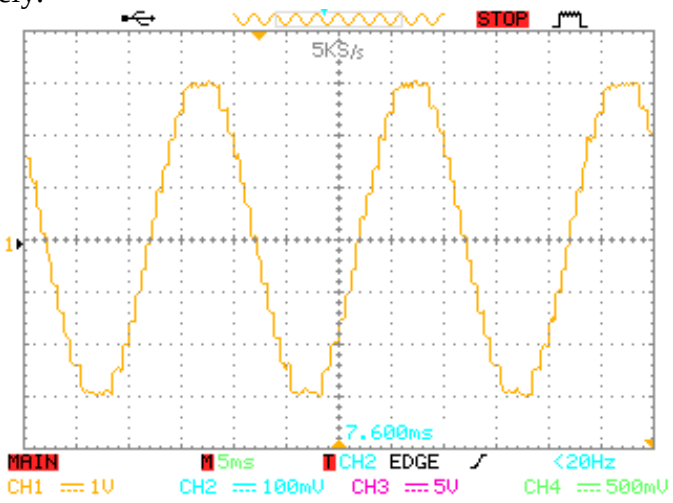
In order to evaluate the performance of the suggested multilevel converter a single-phase 13-level prototype has been modeled and implemented. The implemented circuit's main parameters are given in Table 2.

Table 2

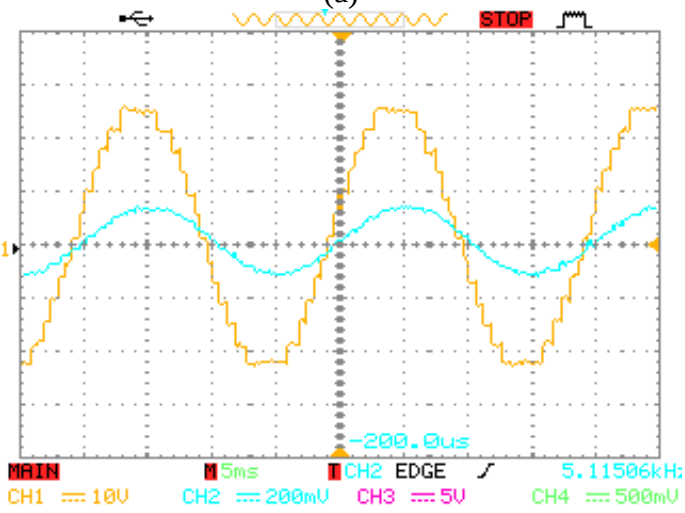
Parameters of implemented inverter

Type of switch	IRF260
Type of MOSFET driver	Hcpl316j
Pulse Generator	DsPIC30F4011
DC Voltage Sources Magnitudes	5V
Load Parameters	(1+19) Ohm & 18mH
Fundamental Frequency	50Hz

Fig. 10 (a)-(b) present the experimental results of the output voltage waveforms for the13-level proposed symmetric topology in no load and under RL load, respectively.



(a)



(b)

b) Output voltage and load resistant voltage (current) (1*10 volt/div)

Fig. 10. Experimental results of implemented 13-level inverter a) Output voltage (no load) (10 volt/div); b) Output voltage and load resistant voltage (current) (1*10 volt/div)

Fig. 10 (a) shows the output voltage of the proposed converter which validates the practicability of the proposed structure to generate the desired levels. Fig. 10 (b) shows the current-voltage waveforms under load condition. As seen in this figure, the simulation and experimental results are saliently matched. Partial

difference between simulation and experimental results is due to the voltage drops on switches in the prototype.

6. Conclusions

In this paper, a new converter topology has been proposed having superior features over conventional topologies. In the proposed topology, less number of components including power switches and gate driver circuits are required compared to conventional converters. To implement the inverter circuit, a lower number of required devices results in total costs substantial reduction and makes the control scheme simpler. In order to validate the feasibility of the proposed inverter simulation results are provided. Also, experimental results of the developed prototype for 13-level converter of the proposed topology are given in this paper.

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