800V BIAS FOR VERY HIGH DENSITY 5KW POWER CONVERTER IN ARTIFICIAL INTELLIGENCE APPLICATIONS

Ionel JITARU[1]

Very high power module, of 5KW operating from 800V to provide 50V with a power density of 135W/cm^3 requires a bias supply to fit in a power module of a surface of less than 40cm^2. That creates a major challenge because available Integrated Circuits (ICs) for such applications do not exist, and the goal is to allocate to the bias supply less than 0.8cm^2 on the power module. The size of the switching devices for voltage of 1000V and above is another challenge forcing us to consider using a 650V device. The paper will present several solutions in addressing such a challenge. A layout is proposed for the chosen solution presented in this paper meeting the proposed target of 0.8mm2. The focus of this article was to offer bias solutions to a very challenging specification for 5KW power converter operating from 800V bus for Artificial Intelligence applications.

Keywords: self-oscillating flyback, low power mode, bias power

1. Introduction

There are several major challenges in such applications. First, the PCB surface allocated for such a bias supply is less than 0.8cm^2. That requires the magnetic core to have a cross-section of less than 0.05cm^2. Though the output power for the bias supply is approximately 1W, to be able to process power in the specified magnetic core, the on time must be less than 200ns, which is the equivalent of 500Khz-1Mhz operation. The second challenge associated with this application is the input voltage of 800V. The power devices that are able to sustain a voltage of 1000V are SiC devices, which are developed for higher power and are relatively large. For example, C3M0065100J is a Silicon Carbide Power Mosfet of 1000V having a 7L D2PAK package which occupies a footprint of 15mm by 17mm, which is 2.55cm2, three times our target area. Another challenge associated with the bias power in such an application is the creepage distance of 12mm. which will carve away a good portion of the surface available for such an application.

Because control ICs are not available for 800V input voltage, I have decided to look into other technologies for bias supply. Such a solution is the use of self-oscillating flyback topology [1], due to the fact that it is a reliable, low component-count circuit

[1] PhD student, Faculty of Electronics, Telecommunications and Information Technology, National University of Science and Technology POLITEHNICA Bucharest, Romania, e-mail: ionel.jitaru@stud.etti.upb.ro, dan.jitaru@rompower.com

and can operate at high frequencies. This solution has been used in the past for low power applications from a 400V bus, which is the voltage obtained from the rectification of the AC input voltage line. In self-oscillating flyback topology, the operation frequency can be tailored to be several hundred Khz.

In this paper I will present several solutions for the operation of self-oscillating flyback.

The first solution is using only one switching device of 650V. The switching device suitable for this application is the N-channel 650V, 1.6 Ohm, 2.3A MDmesh Power Mosfet, STL3N65M2, in 3.3x3.3 HV package. The disadvantage of this solution is low efficiency, of approximately 40% or even lower, though the power dissipation is only 1.5W. In such application for a power module of 5KW wherein the power dissipation is approximately 50W, the dissipation of another 1.5W is not a major concern as long as I can fit the bias supply in the available space of 0.8cm^2.

The second solution which is also feasible for this application and even for higher power is splitting the input voltage into two totem pole 400V sections, wherein each section does have a bias power train using self-oscillating flyback implementation. In such a solution we must ensure that the middle point of 400V does stay in a narrow range, in such way that the tolerances of the middle point will not exceed 100V. To be able to achieve this goal the power processed by the two power trains shall be in between a very narrow range. In the second solution we will use two STL3N65M2 devices, both of these two solutions utilize the same self-oscillating topology.

In this paper I will start doing an analysis of the self-oscillating flyback topology operating in standard mode in Section 2, ZVS mode and low power mode wherein the low power mode is the most suitable for this application. After that I will present two solutions for implementing the 800V bias supply underlining the advantages and limitations of each of the solutions. The final implementation in Section 3 was done using the second solution because of its higher efficiency.

2. Analysis of the self-oscillating flyback operation

The self-oscillating flyback converter operates in critical conduction mode, [1], [2],[3],[4],[5], which is at the boundaries between continuous and discontinuous mode of operation. It uses peak current mode control, and the frequency varies in function of the input voltage and the loading conditions.

In Fig. 1, the basic schematic of a self-oscillating flyback converter is presented. It consists of a transformer Tr, having a primary winding L1, with an inductance Lm, a secondary winding L_2 and a feedback winding L_3. There is a power switch in the primary, M_1, in series with a current sense resistor R_C.

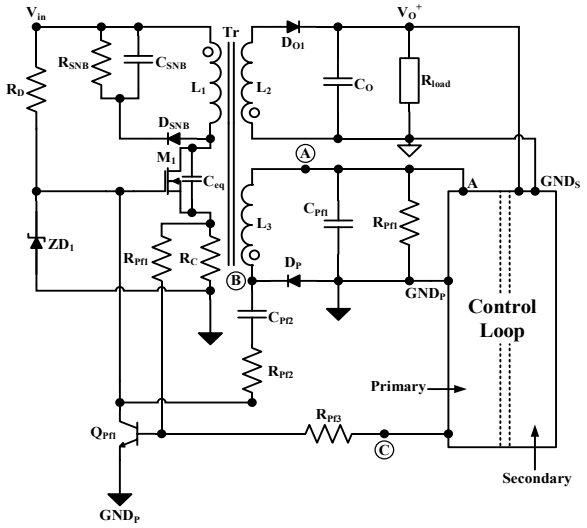


Fig. 1. Self-Oscillating Flyback Converter [1]

In the gate of M_1 there is a Zener, ZD_1, which has the role of limiting the voltage in the gate of M_1. In the secondary section of the converter there is a rectifier D_{O1} and a capacitor C_O across which the output voltage V_O is developed. There is a control loop circuit further detailed in Fig. 2. In the primary there is a switch Q_{pf1} which turns off the primary switch M_1 when the summation of the currents provided by the voltage across R_C via R_{pf1} and the output feedback loop via R_{pf3} reach the turn on amplitude for Q_{pf1}. The feedback winding L_3 creates a voltage in the primary across C_{pf1} and R_{pf1} which emulates the output voltage Vo^+, proportional with the turn ratio between L_2 and L_3. There are two nodes in the primary, which play a key role in the control mechanism. The node C which is connected to R_{pf3} and to the primary side of the control loop which can be also connected to the node A, in a simplified version wherein the accuracy of the V_O^+ amplitude is not critical, and the converter will regulate V_O^+ into some acceptable tolerance.

The secondary section of the control loop is presented in Fig. 2. The information from the output voltage V_O^+ versus GNDs is divided by R_{S1} and R_{S2}, information which applies to the TL431 IC, ZD_1, which has an internal voltage reference. The compensation loop includes a zero produced by C_{sf1} and R_{sf1} and a pole produced by C_{sf2}. The gain is controlled by R_{sf2} and the gain of the optocoupler IC1. The control loop depicted in Fig. 2 is connected to the primary to the nodes (A), and (C) and to the primary ground GNDp.

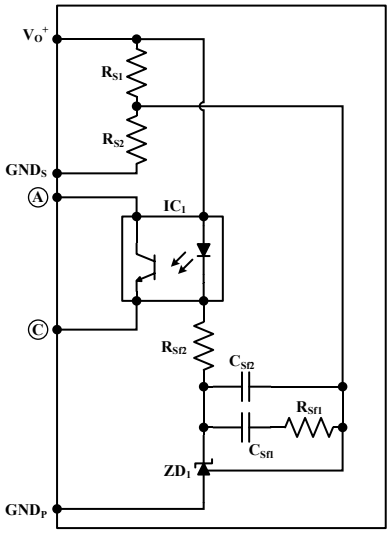


Fig. 2 Secondary Section of the Control Loop [6]

Steady State Operation in the standard mode

In Fig. 3, the key waveforms associated with the circuit from Fig. 1 are presented.

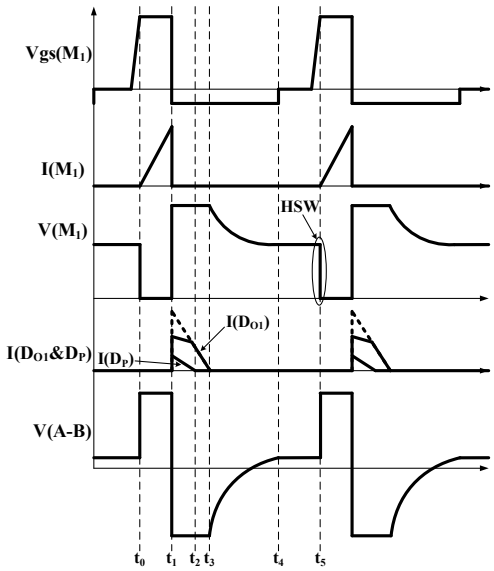


Fig. 3 Key Waveforms of the circuit from Fig. 1 operating in Hard Switching (HSW) mode [6]

In steady state operation in the standard mode of operation, I identified 5-time intervals. From t_0 to t_1 the main switch M_1 turns on and the current will flow via L_1, storing energy in the transformer Tr via the magnetizing current. The current flows also via R_C developing a triangular shaped voltage across it, proportional with the current through M_1. At t_1 the voltage across R_C generates a current via R_{pf1} and together with the additional current through R_{pf3} will reach an amplitude which will turn on Q_{pf1} at t_1. Between t_1 to t_2 and t_3 the energy stored in the Tr will be transferred to L_2 in the secondary via D_{O1} and via L_3 and D_p in the primary side. The resistor R_{pf1} is chosen to have a small current through it and as a result most of the magnetizing energy is transferred to C_O and R_{load}. This is also depicted by the I(Dp) and I(D_{O1}). At t2 the current through Dp reaches zero and further the magnetizing current flows via D_{O1}. At t_3 all the energy stored in the magnetizing current of Tr is depleted and the voltage across M_1 starts decaying with a rate proportional with the parasitic capacitance across M_1 plus the parasitic capacitances reflected across M1 from the secondary side. This transition occurs between t_3 to t_4. At t_4 the voltage in gate becomes zero. At t_5 the positive feedback is initiated, and the voltage (A-B) becomes positive and M_1 is turned on and the following cycle is initiated.

Steady State Operation in ZVS mode

In Fig. 4 the key waveforms are presented associated with the circuit from Fig. 1 operating in Zero Voltage Switching mode. The difference between this mode of operation and the standard mode is the characteristics of Dp. In the case wherein Dp is a diode with a large reverse recovery time, Trr, the mode of operation changes significantly. In this mode of operation, I identify three-time intervals. From t_0 to t_1 the main switch M_1 turns on and the current will flow via L_1, storing energy in the transformer Tr via the magnetizing current. The current flows also via R_C developing a triangular shaped voltage proportional with the current through M_1. At t_1 the voltage across R_C and the additional current through R_{pf3} will reach an amplitude which will turn on Q_{pf1} at t_1. Between t_1 to t_2 the energy stored in the transformer Tr will be transferred to the windings L_2 and L_3. The current through L_2 and L_3 is depicted by D_{O1} and Dp. At t_2 the current through Dp reaches zero. After t_2 due to the reverse recovery of Dp the current will flow in reverse due to the minority carriers in the junction.

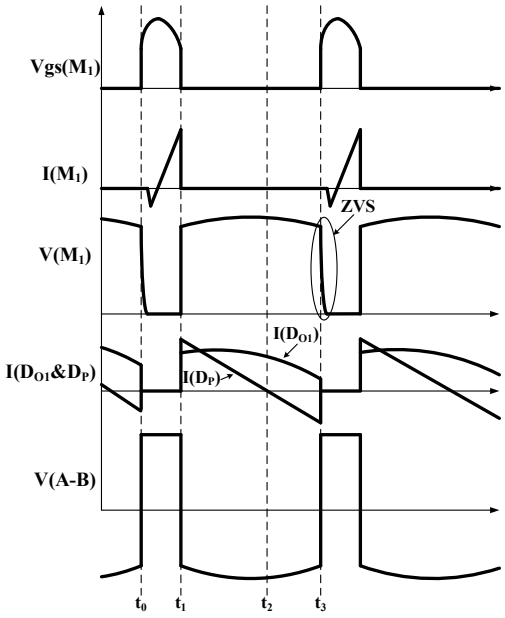


Fig. 4 Key Waveforms of the circuit from Fig. 1
operating in Zero Voltage Switching (ZVS) mode [6]

At t_3 all the carriers in the junction are depleted and the diode Dp will turn off becoming a high impedance device. As a result of the current interruption via Dp, the energy in the leakage and magnetizing inductance will fully discharge the parasitic capacitance reflected across M_1 to zero. The negative current which discharges the parasitic capacitance reflected across M_1 is depicted in $I(M_1)$.
In ZVS mode of operation as previously presented there is a resonant circuit with original conditions which is analyzed in [12]. Based on the analysis mentioned I will apply the following equations. These equations will apply to all the resonant circuits with initial conditions which is the key element in all the Pulse Width Modulation, ZVS topologies.

$$Z_C = \sqrt{\frac{L_m}{C_{eq}}}, \tag{1}$$

where Z_C is the characteristic impedance of the resonant circuit formed by inductance L_m of the winding L_1 of transformer Tr, depicted in Fig. 1, and C_{eq} is the parasitic capacitance reflected across the switching element M1 from Fig. 1.

$$\omega = \frac{1}{\sqrt{L_m * C_{eq}}}, \tag{2}$$

where ω represents the angular frequency.

$$\emptyset = arctan\left(Z_C * \frac{I_m}{V_r - V_{in}}\right), \tag{3}$$

where θ is the phase.

$$V_{SW}(t) = V_r - (V_r - V_{in})\frac{\cos\emptyset - \cos(\emptyset - \omega t)}{\cos\emptyset}, \tag{4}$$

where V_{sw} (t) is the voltage across the switching element M1, from Fig. 1.

$$I_{Lm}(t) = (V_r - V_{in})\frac{\sin(\emptyset - \omega t)}{Z_C * \cos\emptyset}, \tag{5}$$

where I_{Lm} (t) is the current through the primary (L1) of transformer Tr, from Fig. 1. In conclusion in the ZVS operation mode is accomplished by the reverse current flowing through Dp, which is function of the reverse recovery characteristic of the diode. In references [6] and [7] are presented ZVS flyback topologies which do resemble the self-oscillating flyback operating in ZVS mode.

Steady State Operation in very low power mode

In Fig. 5 the key waveforms are presented associated with the circuit from Fig. 1 operating in low power mode. In low power mode the frequency of operation can be very small and consists in narrow pulses with a very large dead time in between.

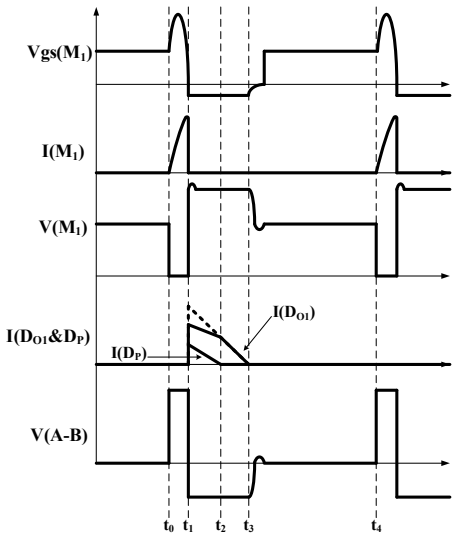


Fig. 5. Key Waveforms of the circuit from Fig. 1 operating in very low power mode [6]

In this mode of operation, I identified four-time intervals. From t_0 to t_1 the main switch M_1 is on and during this time the current through L_1, M_1 and R_S is triangular. The gate of M_1 has a half sinusoidal shape due to the narrow interval between t_0 to t_1, and the effect of the gate capacitance. This mode of operation

applies in very low power applications, in the range of several watts. Between t_1 to t_2 a portion of the energy stored in Tr during t_0 to t_1 is transferred via L_3, via to Dp into the capacitor C_{pf1}. At t_2 the current via Dp reaches zero. The current through D_{O1} will continue to flow until t_3. At t_3 all the energy stored in the magnetizing current of Tr is transferred to C_O and C_{pf1}. In between t_3 to t_4, when the cycle repeats there is the dead time wherein there is no energy extraction from V_{in}. This mode of operation is very suitable with low power, wherein a given quantum of energy is processed by the converter followed by a long dead time. For higher power the repetition frequency can be increased. This mode of operation is very stable, and the repetition frequency can be controlled by the value of R_D and C_{pf2}. The value of the quantum of energy is the function of the value of resistor R_C. For simplicity, in this mode of operation resistor R_{pf3} can be easily connected to node A.

This mode of operation is the most suitable for the application presented in the abstract. It has the advantage of simplicity in a reduced number of parts. The short interval between t_0 to t_1 allows the flux density through the magnetic core of Tr to be very small reducing the core loss and allowing a very small size magnetics. This technology comprises of a low on time which means low flux swing together with a very large dead time which reduces power dissipation in switching losses and leads to good efficiency for low power applications.

The quantum of energy transferred to the secondary in each cycle can be fully controlled by the inductance of the primary winding and the size of the sense resistor. An increase in the quantum of energy will lead to a lower switching frequency which would translate in lower switching losses which lead to higher efficiency. In addition to that the size of the transformer will decrease, allowing a lower cross-section in the magnetic core.

Ideally for such an application it is desirable to have a smaller size Die for the main switch, with lower parasitic capacitance and higher on resistor which in such application it is not a drawback. The proposed part, STL3N65M2, is very suitable for this application.

First solution for 800V bias supply

In Fig. 6A is presented the first solution for implementing a bias supply operating from an 800V bus using 650V switching devices which can be silicon or GaN device.

The implementation depicted in Fig. 6A, [6], is using a NPN bipolar device to maintain V_{in}^+ at a safe voltage level before the bias supply starts working using *operation in very low power mode* previously described. A safe operating mode is when the voltage across the main switching device M_1 from Fig. 1, has a maximum voltage level of DR* V_{ds} max. DR represents the derating voltage, which can vary from 70% to 85% function of the manufacturing guideline. The voltage across the main switching device in the flyback topology is given by V_{in}+n*Vo, wherein “n”

is the turns ratio in the transformer and Vo is the output voltage in the secondary of the converter. In addition to that there may be additional voltage spikes across the main switching device caused by the energy in the leakage inductance. In the self-oscillating flyback topology operating *in very low power mode*, due to the lower power (1W-5W) the leakage spike can be negligible due to an optimized snubber circuit formed by D_{snb}, C_{snb} and R_{snb}.

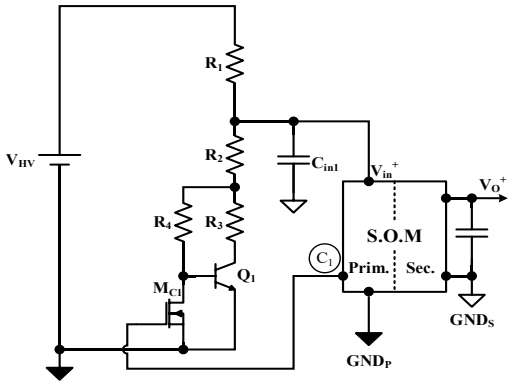


Fig. 6A. The first solution for an 800V bias supply using a 650V switch [6]

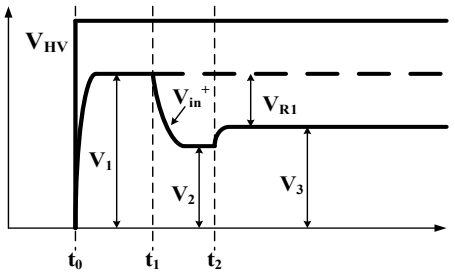


Fig. 6B. The Voltage across S.O.M. during the Stages of Operation [6]

In Fig. 6B the key waveforms on the circuit depicted in Fig. 6A are presented. The voltage V_{in}^{+} which applies to the bias supply is given by eq. (6).
For the circuit depicted in Fig. 6A, I identified three time intervals as depicted in Fig. 6B.
At t_0 when the high voltage source V_{HV} applies, the voltage in V_{in}^{+} is kept to a safe level, for example between 400V and 500V.

$$V_{in}^{+} = V_{HV} \frac{R_2+R_3}{(R_1+R_2+R_3)}, \tag{6}$$

where V^{+}_{in} is the voltage across C_{in1}, which is applied to the S.O.M., and V_{HV} represents the high voltage bus which is 800V and R1, R2 and R3 are the resistors from Fig. 6A.

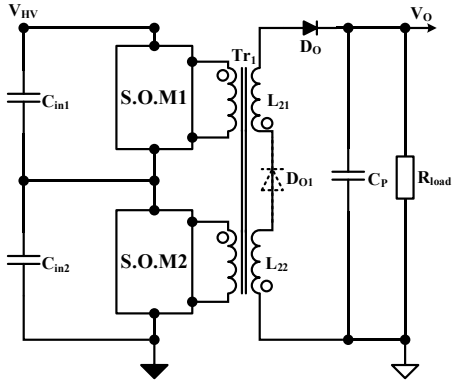
At t_0 when the high voltage source V_{HV} applies, the voltage in V_{in}^{+} is kept to a save level due to Q1 conduction, for example 400V of even 500V function of the derating voltage acceptable and the turns ratio in the transformer.

The bias supply can be activated soon after the V_{HV} applies and at t_1 will soon follow, after the voltage across C_{in1} reaches the steady state level. The voltage in V_{in}^{+} has the voltage level which is a safe voltage for the bias to operate.
At t_1 when the bias supply is turned on the voltage in V_{in}^{+} will drop because bias supply is in parallel with the R_2+R_3, drawing current through R_1.

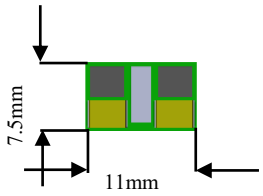
The circuit depicted in Fig. 6A ensures that the voltage in V_{in}^{+} is kept to a level wherein all the devices including the primary switch are under the maximum voltage rated, including the primary switch.
The disadvantage of this circuit is that there is power dissipation on R_1. For example, for the case wherein the bias supply is producing 1W with an efficiency of 70% the power extracted from the 400V bus is 1.42W and the current extracted via R_1 is 3.55mA and the power dissipated on R_1 is also 1.42W. The total power dissipation in R_1=1.42W and in the bias supply is an additional 0.42 W, which means the total power dissipation using this solution is 1.8W dissipated on the PCB. The implementation of the bias supply can have an even lower efficiency which will further increase power dissipation to much higher levels.

Second solution for 800V bias supply

In Fig. 7, the second solution [6] for implementing a bias supply operating from an 800V bus using 650V switching devices is presented.



a) Two self-oscillating modules sharing one transformer Tr1 with secondaries in series [6]



b) A proposed layout wherein there are two primary switchers on top (black) a magnetic core in between and two high voltage capacitors below [6].

Fig. 7. The second solution for an 800V bias supply using two 650V switches [6]

Unlike the solution presented in Fig. 6 which is composed by one self-oscillating flyback converter and a resistor R_1 which emulates a converter in order to split the V_{HV} and limit the voltage across the self-oscillating module (S.O.M.), the arrangement depicted in Fig. 7 is composed by two self-oscillating flyback converters which can share the same transformer and the secondary windings L_{21} and L_{22} are in series. In the event the output voltage is higher, a second diode, D_{O1}, is placed in between the secondary windings. The two self-oscillating flyback

converters can also be implemented with independent transformers as long as the secondary windings are placed in series. In Fig. 7 the second solution of the 800V bias supply is presented, and a suggested layout in 1:1 scale to underline the size challenge. The implementation contains two 650V N-channel switching devices and a small planar transformer wherein the windings are buried inside of the multilayer PCB. The projected dimensions are 7.5mm by 11mm, which means a total area of 0.80cm2.

Placing the secondaries windings in series does have a major advantage. In the discontinuous flyback topology, which is also the case of self-oscillating flyback topologies the current in the secondary via the rectifiers such as Do and function of the implementation also in D_{O1}, will reach zero and the rectifiers become high impedance devices and the secondary opens up triggering the turn off cycle such is t_5 from Fig. 3 or t_3 from Fig. 4 or t_4 from Fig. 5. As a result, each self-oscillating flyback, are synchronized at turn off of the main switch, even if the turn on of the main switch in S.O.M1. and S.O.M2 may not be fully aligned. Both converters can operate in standard mode, ZVS mode or low power mode.

The concept can be generalized in the case wherein "n" self-oscillating flybacks are placed in series splitting the high input voltage and allowing the utilization of lower voltage for main switches in each module. The connection of the secondary windings in series or via an additional output rectifiers will ensure the split of the input voltage equally across each self-oscillating module.

The most suitable solution for the implementation of the self-oscillating flyback is the *very low power mode*. In this mode the on time for the primary switchers can be very small, which reduces the size of the transformer's magnetic core, and the repetition frequency can be kept low, reducing as a result the switching losses on the main switchers in each module. In references [9], [10], [11] are presented technical solutions for very high power and very high-power density power converters in the power range of the application presented in this article.

3. Conclusions

The self-oscillating flyback converter operating low power mode with controlled low repetition frequency is identified as the most suitable topology for low power bias supply operating from 800V input and using 650V switching devices frequency. This paper analyses the self-oscillating flyback topology and underlines three modes of operation. Further the paper presents two novel solutions for designing a low power bias supply operating from 800V and using 650V switching devices, while containing the bias supply on the area of 0.80 cm^2. The bias supply is part of an ultra-high density bus converter of 5KW, operating from an 800V bus to provide a 50V output. The power density of the 5KW bus converter for Artificial Intelligence applications is 135W/cm^3 and reaching an efficiency of

99%. This solution is an intermediary solution until a suitable IC (Integrated circuit) may be developed for such an application if commercially feasible.

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