DECISION LEVELS FOR A MAXIMUM SELECTOR CIRCUIT

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The paper considers an analog circuit intended to find the largest element in a parallel processed list. The list is encoded into input currents with limited amplitude and current dispersion. The winner is decided by signaling the surpass of a certain computable threshold by the output voltages. As a consequence of applications in implantable devices, the circuit uses MOS transistors in subthreshold regime where the currents are under nA. The separation levels of output are exactly computed under restrictions on the input currents, control current, MOS parameters. The circuit resolution is computable in the synthesis phase as well.

Keywords: neural circuits, low-power analog circuits, subthreshold MOS, WTA, maximum rank extractor, Lazzaro circuit

1. Introduction

Computational analog circuits are efficiently used in signal processing. This is true especially for neural circuits where a large number of simple identical cells are interconnected in order to do multi-variable algebraic or logical operations. Beside the ease of VLSI implementation, this kind of circuits are faster than their digital counterparts. Also, neural analog circuits can be enclosed perfectly in biologic or artificial sensor signal processing.

This paper deals with an efficient circuit that finds the maximum of a data list (Winner-Take-All - WTA). It has a small number of interconnections and consists of simple two-MOS cells. This was first introduced by C. Mead, J. Lazzaro and their team, [4]. This kind of circuit is used for artificial retina, perception of movement, classifiers, biologic implants and many other.

This kind of circuit works with voltages of mV and currents of nA and consequently the MOS transistors must operate in subthreshold regime.

The circuit receives data lists consisting of currents characterized by extreme values and relative separation. We infer conditions on the maximum input current and on the control current. The circuit output is a voltage: the winner voltage must be strongly separated from all the other voltages.

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2. MOS model

We use the subthreshold model of MOS well-known in literature [2], [6], [1]:

$$I_{DS} = I_0 \exp\left(k\frac{V_G}{V_t}\right)\left[\exp\left(-\frac{V_S}{V_t}\right) - \exp\left(-\frac{V_D}{V_t}\right)\right] \tag{1}$$

where:

$$I_0 = \frac{W}{L} I_{D0} \exp\left[(1-k)\frac{V_B}{V_t}\right] \tag{2}$$

and

$$I_{D0} = 6.49\times 10^{-6}\left(\frac{V_t}{k}\right)^2 \tag{3}$$

Here, $k \in [0.5,1)$ is the slope factor depending on technology. V_G, V_S, V_D, V_B are the terminal voltages, V_t is the thermic voltage.

The subthreshold conditions are:

$$V_{GS} \le V_T$$
$$V_{DS} \ge 0$$
$$I_G = 0$$

The circuit is shown in Fig. 1.

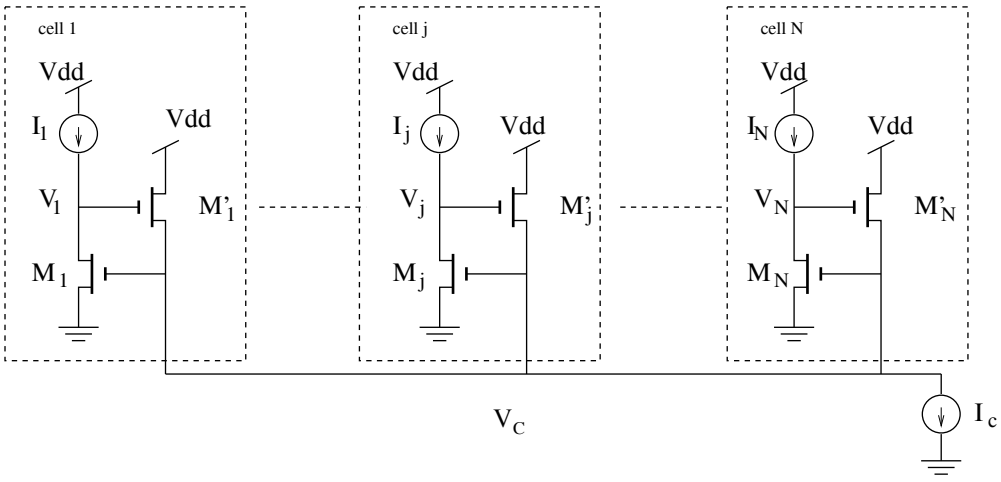

Fig. 1: The WTA circuit studied

By the First Kirchhoff Theorem, in V_j and V_C nodes ([3]) along with (1) above, we find:

$$\begin{cases} I_j = I_0 \exp(kV_c/V_t)\left[\exp(-0/V_t) - \exp(-V_j/V_t)\right] & , \quad j \in \overline{1,N} \\ \sum_{j=1}^{N}\left\{I_0 \exp(kV_j/V_t)\left[\exp(-V_C/V_t) - \exp(-V_{DD}/V_t)\right]\right\} = I_c \end{cases} \tag{4}$$

If we scale all the voltages by V_t and all the currents by I_0, we get:

$$\begin{cases} i_j = \exp(ky)\left[1 - \exp(-x_j)\right], \quad j \in \overline{1,N} \\ i_C = \exp(-y)\sum_{s=1}^{N}\exp(kx_s) \end{cases} \tag{5}$$

where

$$x_j = \frac{V_j}{V_t} \quad , \quad y = \frac{V_c}{V_t} \quad , \quad a = \frac{V_T}{V_t} \quad , \quad d = \frac{V_{DD}}{V_t} \quad , \quad b = \frac{V_B}{V_t} \tag{6}$$

and

$$i_j = \frac{I_j}{I_0} \quad , \quad i_C = \frac{I_C}{I_0} \tag{7}$$

Here we took $\exp(-d)$ as zero in comparison with $\exp(-y)$.
Also we can take

$$\begin{cases} u_j = \exp(x_j) = \exp\left(\dfrac{V_j}{V_t}\right) \\ v = \exp(y) = \exp\left(\dfrac{V_C}{V_t}\right) \end{cases} \tag{8}$$

and the following equations describing the steady state are obtained:

$$\begin{cases} u_j i_j = v^k (u_j - 1) \quad , \quad j \in \overline{1,N} \\ v i_c = \sum_{j=1}^{N} u_j^k \end{cases} \tag{9}$$

3. The input current lists

The WTA filter we are building has N inputs where the currents $I_1, I_2, \ldots I_N$ are coming into. The currents are all positive and distinct with the smallest distance called "separation" $\Delta = \min |I_j - I_i| (i \neq j)$. If I_M is the largest possible current, we denote the relative separation by $z = \frac{\Delta}{I_M}(N-1)$, as in [5].

If σ is the permutation that orders the elements decreasingly, then we can write the list as:

$$I_{\sigma(1)} > I_{\sigma(2)} > \ldots, I_{\sigma(N-1)} > I_{\sigma(N)}$$

and $\Delta = \min(I_{\sigma(j)} - I_{\sigma(j+1)})$.

We write for convenience j instead of $\sigma(j)$, all over bellow. The following bounds can be easily derived:

$$I_{jm} \leq I_j \leq I_{jM} \tag{10}$$

$$I_{jm} = (N-j)\Delta = zI_M \frac{N-j}{N-1} \tag{11}$$

$$I_{jM} = I_M - (j-1)\Delta = I_M\left[1 - \frac{z}{N-1}(j-1)\right] \tag{12}$$

The smaller the separation is, the larger is the overlapping of the intervals $[I_{jm}, I_{jM}]$.

4. WTA Levels

Fig. 2 shows a WTA circuit with $N = 3$ inputs. If we suppose that I^{α} is the incomming list, then the output list should be V^{α}, both shown in Fig. 3.

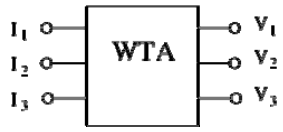

Fig. 2: WTA Circuit with $N = 3$

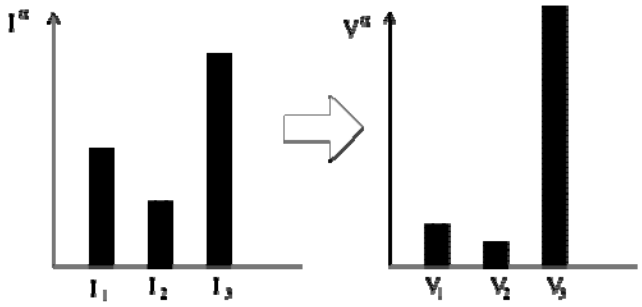

Fig. 3: I^{α} yields V^{α}

The fact that V_3 is the largest voltage in the output list encodes the fact that the current of the same rank i.e. I_3 is the largest one at the input. The WTA should signal the rank 3.

Fig. 4 shows I^{β} input yielding V^{β} output with I_1 and V_1 the largest elements. The WTA should signal the rank 1.

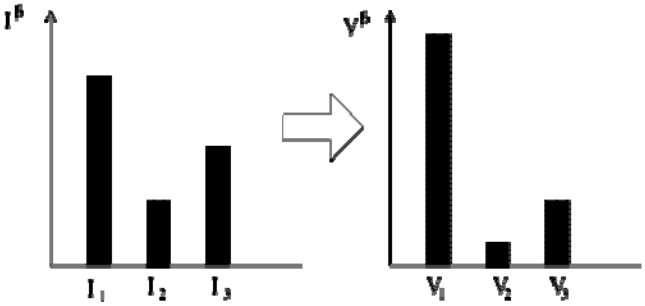

Fig. 4: I^{β} yields V^{β}

If our WTA processes the lists I^{α} and I^{β} following each other and if we take V_{th} as a level of decision, then V_{th} equals the minimum of V_3 in V^{α} and V_1 in V^{β}. Thus the winning rank will be always the only one above V_{th}. All the other elements should be placed under that level.

For accuracy control, we take two thresholds: V_{Hth} and V_{Lth}. If $I_{\sigma(1)} > I_{\sigma(2)} > \ldots > I_{\sigma(N)}$ is one list in the allowed sets of lists, then WTA output should look as:

$$V_{\sigma(1)} \geq V_{Hth} > V_{Lth} \geq V_{\sigma(2)} > \ldots > V_{\sigma(N)}$$

Here σ is the index permutation to write the list in decreasing order.

In order to have $V_{\sigma(1)} > V_{Hth}$ we have to take V_{Hth} as the lowest winner in all possible lists. In order to have $V_{Lth} > V_{\sigma(2)}$ we have to take V_{Lth} as the highest looser. And finally we have to ensure:

$$V_{Hth} > V_{Lth} \tag{13}$$

A measure of *WTA* efficiency is the resolution:

$$R = \frac{\frac{V_{Hth} - V_{Lth}}{V_M}}{\frac{I_{2M} - I_{1m}}{I_M}} \tag{14}$$

where V_M is the largest possible output. We can show that V_M is V_1 for the list $(I_{1M}, I_{2m}, I_{3m}, \ldots, I_{Nm})$. R is a ratio between relative splitting at output versus input. We have $I_{2M} - I_{1m} = I_M\left(1 - z\frac{N}{N-1}\right)$, meaning that $I_{2M} > I_{1m}$. The circuit "turns over" the components: $V_{1m} > V_{2M}$.

5. Restrictions in order to have WTA

Let us consider the steady state equations:

$$\begin{cases} 0 = u_j i_j - v^k (u_j - 1) \quad , \quad j \in \overline{1, N} \\ 0 = -v i_c + \sum_{j=1}^{N} u_j^k \end{cases} \tag{15}$$

This means v is the solution of:

$$v i_C = \sum_{j=1}^{N} \left(\frac{v^k}{v^k - i_j} \right)^k \tag{16}$$

and u_j ($j \in \overline{1, N}$) is:

$$u_j = \frac{v^k}{v^k - i_j} \tag{17}$$

Immediately we observe that

$$u_j - u_s = \frac{v^k}{v^k - i_j} - \frac{v^k}{v^k - i_s} = \frac{v^k\left(i_j - i_s\right)}{\left(v^k - i_j\right)\left(v^k - i_s\right)}$$

which shows that $I_j > I_s$ implies $V_j > V_s$. This means that the input order is kept at the output.

From (16) and (17) we can show that

$$\frac{du_j}{di_j} > 0 \quad , \quad \forall j$$
$$\frac{du_j}{di_s} > 0 \quad , \quad j \neq s \tag{18}$$

By using this, we can prove that $\min u_1(i_1, i_2, i_3, \ldots, i_N)$ occurs when the currents are $(i_{1m}, i_{2m}, i_{3m}, \ldots, i_{Nm})$ (list $\mathcal{L}_1$).

Similarly we can prove that $\max u_2(i_1, i_2, i_3, \ldots, i_N)$ occurs when the currents are $(i_{1M}, i_{2M}, i_{3m}, \ldots, i_{Nm})$ (list $\mathcal{L}_2$).

Finally, the $\max u_1(i_1, i_2, i_3, \ldots, i_N)$ is for the list $(i_{1M}, i_{2m}, i_{3m}, \ldots, i_{Nm})$ (list $\mathcal{L}_3$).

All of above gives:

$$V_{Hth} = V_t \log(u_1(\ list\ \mathcal{L}_1)) \tag{19}$$
$$V_{Lth} = V_t \log(u_2(\ list\ \mathcal{L}_2)) \tag{20}$$
$$V_M = V_t \log(u_1(\ list\ \mathcal{L}_3)) \tag{21}$$

In order to have the thresholds in the right position (13), it can be shown that it is sufficient that

$$i_M^{\frac{1}{k}} i_C > \frac{z_{min} N(2-k) + kN(N-1)}{2 z_{min}^{\frac{1}{k}+1}} \tag{22}$$

This gives a computable relation between the maximum admissible current at input and the control current such that the WTA splitting is controllable by V_{Hth} and V_{Lth}

6. Numerical Examples

We consider the MOS transistor with parameters in Table 1.

Table 1

Given parameters

k	V_T [V]	V_t **[V]**	V_B **[V]**	$\frac{W}{L}$	I_{D0} **[A]**	I_0 **[A]**	C_1 **[F]**
0.7	0.75	0.025	-1	1	8.28×10^{-9}	5.09×10^{-14}	10^{-15}

We took $N=10,100,1000$, $k=0.5,0.7$, $z_{min}=0.01,0.1,0.5,0.8$ and went through all the 24 possible combinations. I_M and I_C are taken such as (22) is fulfilled.

Then we compute the special lists $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$ with (11), (12). Then we solve the system (15) with $\mathcal{L}_1$ and extract V_{Hth} as the output first component. We solve again (15) with $\mathcal{L}_2$ and extract V_{Lth} as the output second component. Finally we solve (15) with $\mathcal{L}_3$ and we get V_{1M}.

With this data we compute the resolution (14).

Table 2

Restrictions on I_M and I_C for $k=0.5$

N	I_{Mmax} [fA]	I_{Cmin} [fA]	I_{Cmax} [fA]
10	27	80.335	487
100	8.54	3.35	1540
1000	3.09	33.5	3530

Table 3

Restrictions on I_M and I_C for $k=0.7$

N	I_{Mmax} [nA]	I_{Cmin} [nA]	I_{Cmax} [nA]
10	23.8	82.9	502
100	1.42	829	1000
1000	0.00604	8280	12800

The tables 2 and 3 show the strong dependence of I_M and I_C on the slope factor k. At $k=0.5$, I_M is of [fA] order of magnitude while at 0.7 is [nA]. I_C is generally of 1 to 2 orders of magnitude greater than I_M.

We notice that resolution increases with the separation (see Fig. 5) which is obvious from an intuitive point of view: lists with large disparity are processed more accurate. The resolution at large separations decreases up to 2 times when N increases from 10 to 1000 and is quite constant above $N=100$. For $z<0.5$ the resolution does not depend essentially on separation or number of inputs.

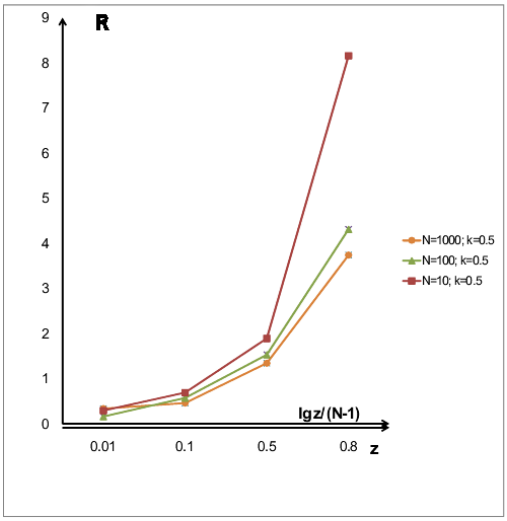

Fig. 5. Resolution R as a function of z ($k = 0.5$)

7. Conclusions

A maximum selector based on the Lazzaro circuit with MOS in subthreshold regime was designed. This kind of circuits finds applications in medical prostheses and sensors, where low-power is essential. Therefore we keep all MOS transistors in their subthreshold region.

The novelty consists in finding exact levels of decision as outputs of predefined lists of inputs. A performance parameter of selection was inferred and verified in various parameter examples.

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