HARMONICS ANALYSIS ON ASYMMETRIC HYBRID MULTILEVEL INVERTER BASED INDUCTION MOTOR DRIVE

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This paper describes the importance of Multilevel inverter technology as a very important alternative in the area of high-power medium-voltage energy control Engineering. The most important topologies like asymmetric hybrid cells and soft-switched multilevel inverters are clearly described in this paper. This hybrid technology is dedicated to the latest applications of these converters. The circuit topology options are also presented. This paper deals with performance of voltage source multilevel inverter-fed induction motor drive. A second highest multilevel Voltage Source Inverter-fed induction motor drive is modeled and simulated using MATLAB/SIMULINK. The Harmonics analyses are discussed by using FFT spectrum for the outputs.

Keywords: Multilevel Inverter, Asymmetric Hybrid Cell, Multilevel inverter fed IM Drive

1. Introduction

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the

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three-level inverter generates three voltages, and so on. Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is $k = 2m+1$and the number of steps p in the phase voltage of a three-phase load in wye connection is $p = 2m-1$.

The term multilevel starts with the three-level inverter topolology. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: Diode-Clamped (neutral-clamped), Capacitor-Clamped (flying capacitors) and Cascaded Multi cell with separate DC sources [1]. The most attractive features of multilevel inverters are as follows:

1. They can generate output voltages with extremely low distortion and lower voltage transient.
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [8].
4. They can operate with a lower switching frequency.

The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. An early traceable patent appeared in 1975, in which the cascade inverter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived. The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. The application of the NPC inverter and its extension to multilevel converter was found in literature. Although the cascade inverter was invented earlier, its applications did not prevail until the mid–1990s. Two major patents were filed to indicate the superiority of cascade inverters for motor drive and utility applications. Due to the great demand of medium-voltage high-power inverters, the cascade inverter has drawn tremendous interest ever since. Several patents were found for the use of cascade inverters in regenerative-type motor drive applications. The last entry for U.S. multilevel inverter patents, which were defined as the capacitor-clamped multilevel inverters, came in the 1990s. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors,

pumps, fans, blowers, compressors, and so on. This paper presents state-of-the-art multilevel technology, considering well-established and emerging topologies as well as their modulation and control techniques. Special attention is dedicated to the latest and more relevant industrial applications of these converters. Finally, the possibilities for future development are addressed.

2. The inverter

A. Power Circuit

The power circuit of the Asymmetric Cascaded H-Bridge Inverter is illustrated in Fig. 1. The inverter is composed by the series connection of two or more H-bridge inverters fed by independent dc-sources provided by individual secondaries of a transformer or batteries. These sources are not equal, i.e.V_{i1}<V_{i2}<……V_{im} for each phase *i*=a,b,c

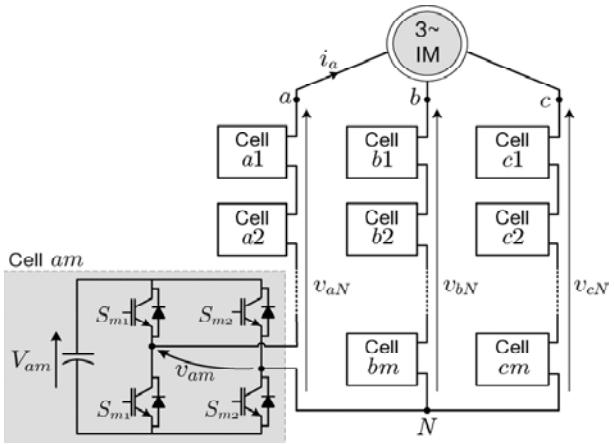

Fig. 1. Asymmetric cascaded H-bridge multilevel inverter.

The use of asymmetric input voltages can reduce, or when properly chosen, eliminate redundant output levels, maximizing the number of different levels generated by the inverter. Therefore this topology can achieve the same output voltage quality with less number of semiconductors. This also reduces volume, costs, losses and improves reliability. When cascading three level inverters like H-bridges (output levels:-V_{dc} , 0 and +V_{dc}, the optimal asymmetry is obtained by using voltage sources scaled proportional to the power of three. Applying this condition to the voltage sources illustrated in Fig. 2, optimal design leads to

$$[V_{i1}, V_{i2} \dots \dots \dots V_{im}]^T = [3^0, 3^1 \dots \dots \dots \dots 3^{(m-1)}]^T \quad \text{---------- (1)}$$

for phase *i*=a,b,c and m the number of cells per phase.

B. Output Voltage Generation

Since the power cells are connected in series, the total phase voltages generated by the inverter can be expressed as

$$V_{iN} = \sum_{j=1}^{m} V_{ij} = \sum_{j=1}^{m} V_{ij}(S_{j1} - S_{j2}) \; i \in \{a, b, c\} \quad \text{----------} \quad (2)$$

Where V_{iN} is the total output voltage of phase (respectively, the neutral of the inverter N), V_{ij} is the output voltage of cell j of phase i, and (S_{j1}, S_{j2}) the switching state associated to cell j.

Note how the output voltage of one cell V_{ij} is defined by one of the four binary combinations of the switching state, with "1" and "0" representing the "On" and "Off" states of the corresponding switch, respectively. The voltage levels generated by the inverter can be calculated by replacing (1) into (2), and considering all the possible combinations of the switching states. The inverter generates 3^m different voltage levels (e.g. an inverter with m=4 cells can generate 3^4=81 different voltage levels). When using three-phase systems, the number of different voltage vectors is given by $3.n_l.(n_l-1)+1$, where n_l is the number of levels. For example, for the case with 81 levels there are 19.441 different voltage vectors (huge difference compared to the nine levels and 217 vectors obtained with a 4-cell symmetric-fed cascaded inverter)

Table 1 summarizes the output levels for an asymmetric nine level inverter using only m=2 cells per phase (only phase α is given). An example of the voltage waveform generation for an asymmetric nine-level inverter is illustrated in Fig. 2.

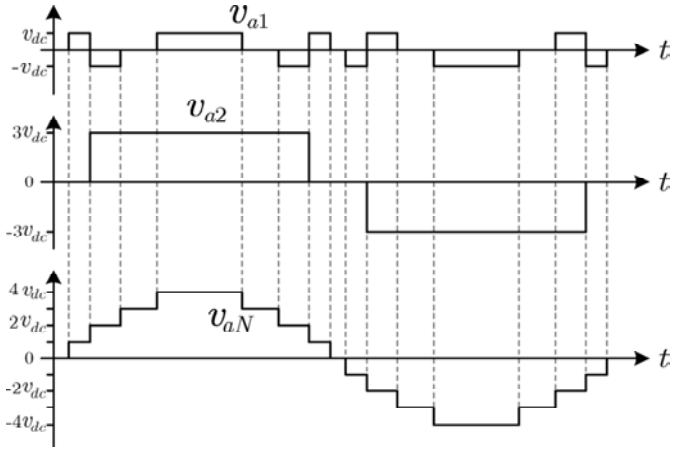

Fig. 2. Output voltage generation with asymmetric inverter

Table 1

Nine-level asymmetric cascaded inverter switching states

	Cell1			Cell 2			Total
#	S11	S12	V_{a1}	S21	S22	V_{a2}	VaN
1.	1	0	V_{dc}	1	0	$3V_{dc}$	$4\ V_{dc}$
2.	0(1)	0(1)	0	1	0	$3V_{dc}$	$3\ V_{dc}$
3.	0	1	$-V_{dc}$	1	0	$3V_{dc}$	$2\ V_{dc}$
4.	1	0	V_{dc}	0(1)	0(1)	0	V_{dc}
5.	0(1)	0(1)	0	0(1)	0(1)	0	0
6.	0	1	$-V_{dc}$	1(0)	1(0)	0	$-\ V_{dc}$
7.	1	0	V_{dc}	0	1	$-3V_{dc}$	$-2V_{dc}$
8.	1(0)	1(0)	0	0	1	$-3V_{dc}$	$-3V_{dc}$
9.	0	1	$-V_{dc}$	0	1	$-3V_{dc}$	$-4V_{dc}$

3. Simulation of Asymmetric Inverter

The method was tested using an 27-level asymmetric inverter-fed induction motor drive. The inverter simulation diagram is shown in Fig.3 and the motor parameters are given in Table 2.

Table 2

Motor Parameter

Parameter	R_S	L_S	Rr	Lr	Lm
Value	0.435	0.002	0.43	0.002	69.31e-3
Parameter	J	F	P	Normal power	
Value	0.089	0.005	2	2238	

In Table 2, the following parameters are presented: R_S=Stator Resistance in Ohms, L_S=Stator Inductance in Henry, R_r=Rotor Resistance in Ohms, L_r=Rotor Inductance in Henry, L_m=Mutual Inductance in Henry, J=Motor moment of inertia in Kg.m^2, F=Friction Factor in N.m.s, P=Pole Pair.

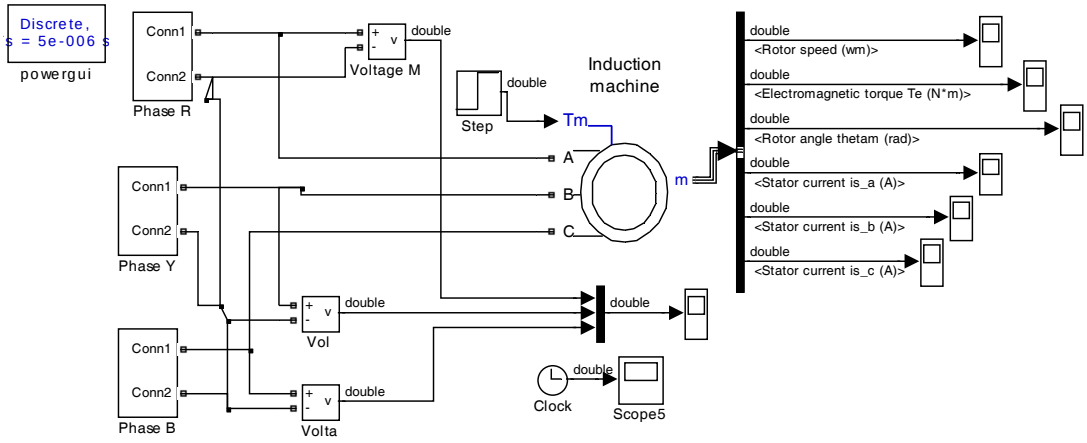

Fig. 3. Simulation diagram

Simulation diagram of 27-level asymmetrical multilevel inverter three phase inverter fed induction motor drive is shown in Fig.3. This three phase Induction motor drive system consist of three cells, each cells consists of four H-bridge circuit to form a single phase system and combined with three cells for create a three phase 27 level inverter. The induction motor is fed from 27-level inverter. The circuit of 27-level inverter is single phase simulation leg is shown in Fig. 4. In the open loop analysis 27 level inverter output obtained through a switching pattern of each cell gate signals generation in the corresponding format by means of literature survey. The output voltage waveforms of the inverter are shown in Fig.5. The output voltage of this 27 level inverter having a staircase pure sinusoidal waveform with acceptable spurious signals. The stator current waveforms are shown in Fig. 6. The stator current gives about maximum percentage of pure sinusoidal signal. Speed response of the induction motor drive is shown in Fig.7. The speed response gradually increases with respect to the applied field. The rotor speed increases and settles at1470 rpm. The frequency spectrum for the output of 27-level inverter is shown in Fig.8. The THD in 27-level inverter is found to be 9.80.

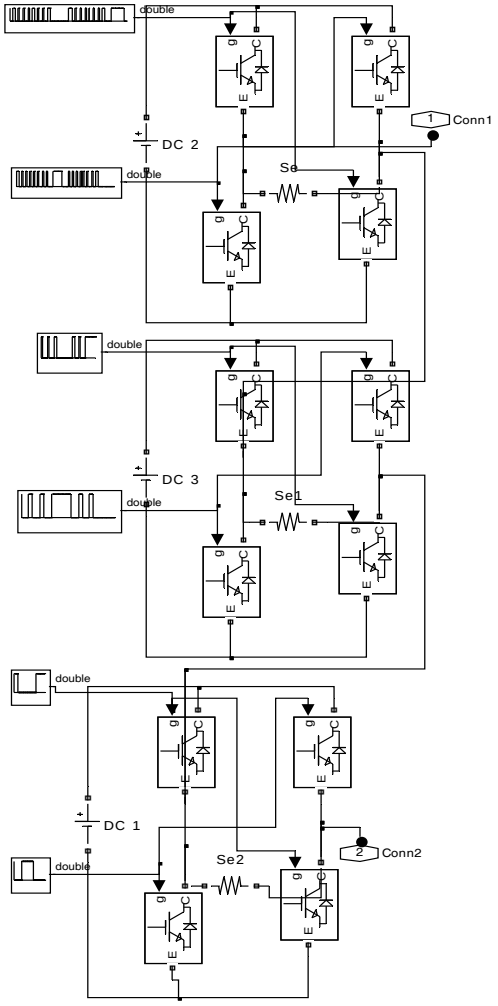

Fig. 4. Simulation diagram of Single phase

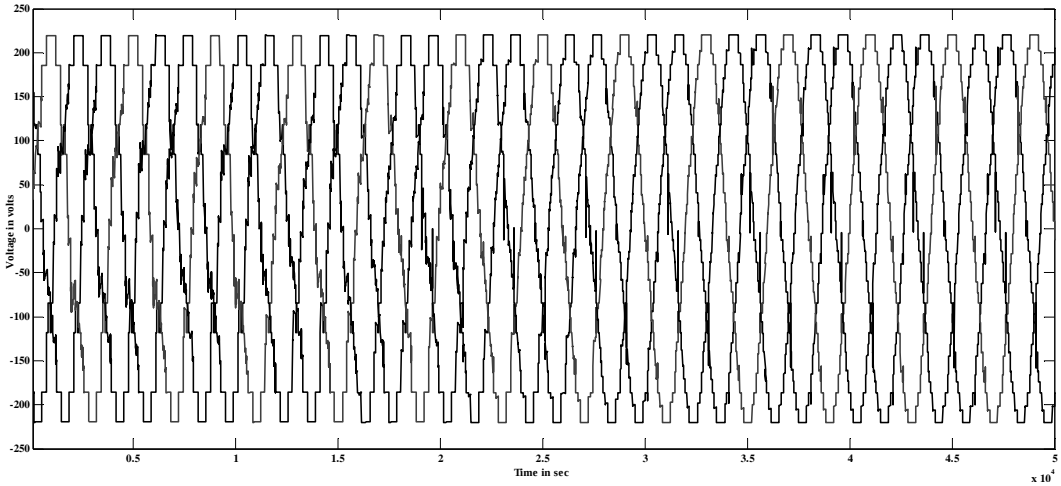

Fig. 5. Output Voltage waveform

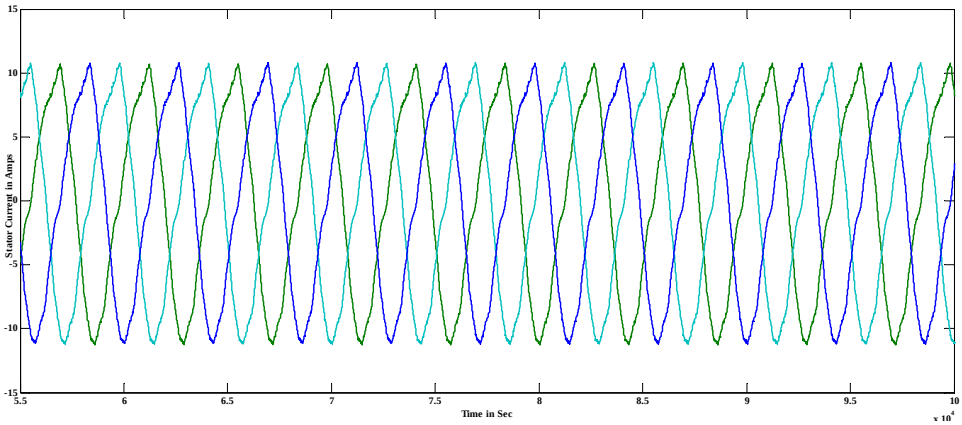

Fig. 6. Stator current waveform

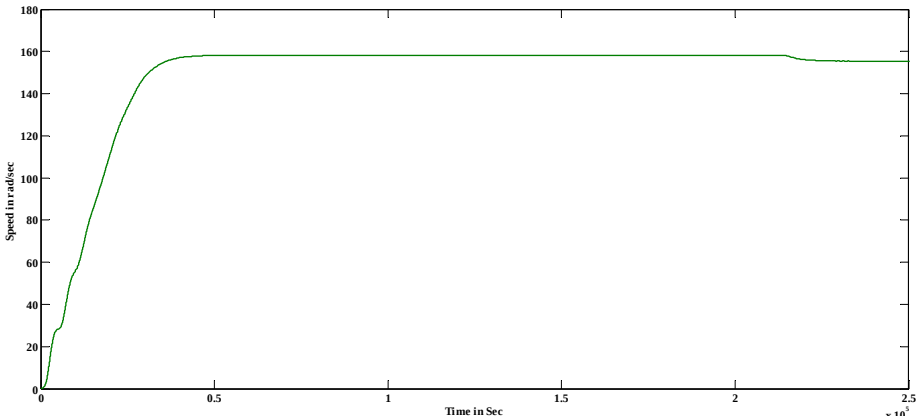

Fig. 7. Motor speed response

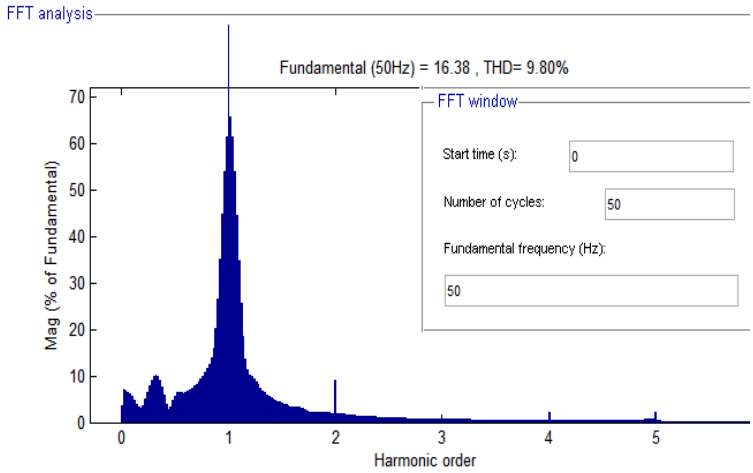

Fig. 8. Motor output voltage FFT analysis of eleven level

4. Conclusion

This paper has provided a cascaded multilevel inverter can be traced back to 1975. However, the commercial products that utilize this superior circuit topology were not available until the mid-1990s. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of asymmetrical multilevel inverters has been introduced systematically. The results of multilevel inverter systems are compared with the results of VSI based drive system. It is observed that the total harmonic distortion produced by the 27-level inverter system is less than that of a 9-level VSI fed drive system. Therefore the heating due to 27-level inverter system is less than that of a 9-level VSI fed drive system. The simulation results of voltage, current, speed and spectrum are presented. This drive system can be used in industries where adjustable speed drives are required to produce output with reduced harmonic content. The scope of this work is the modeling and simulation of 27-level and 9- level inverter and VSI fed induction motor drive systems. Experimental investigations will be done in future.

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