DEVELOPMENT OF A HIGH-PRECISION FREQUENCY SOURCE BASED ON FREQUENCY DIVISION TECHNOLOGY

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A high-precision frequency signal source plays a crucial role in circuit testing and instrument design, providing reference signals for accurate frequency and time calibration. However, modern signal generators used in calibration are limited by their frequency resolution, typically regulated only to 1 μHz, particularly for frequencies below 100Hz. This paper addresses this constraint by developing a high-precision frequency source based on frequency division technology. The proposed frequency multiplication followed by frequency division technology is theoretically derived. To evaluate the constructed high-precision frequency source, we employ a high-precision frequency counter based on an atomic clock to measure the frequency of the output signal generated by the designed signal source. The measurement uncertainty of the experimental data is examined. Experimental results demonstrate that the high-precision frequency source generates a stable square wave frequency signal within a range of 1Hz to 10MHz, offering remarkable, nine adjustable frequency digits.

Keywords: High-precision frequency signal source, Frequency resolution, Frequency multiplication, Frequency division technology, Measurement uncertainty, Square wave frequency signal

1. Introduction

A signal generator is a kind of equipment that can generate electrical signals with varying frequencies, waveforms, and output levels. With the fast development of electronic technology, signal generators are being more extensively employed in critical industries such as aerospace, communication, navigation, radar, instrument, measurement, and detection, and research on signal generators is becoming more significant. Diouri et al. performed a comparative study of hardware architecture performance between Field-Programmable Gate Array (FPGA) and Digital Signal Processing (DSP) chips and demonstrated the benefits of FPGA in signal processing [1]. Researchers analyzed and created the structure of a programmable signal generator based on the microcontroller and FPGA and suggested a digital approach to produce the customized waveform [2].

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Firmansyah et al. investigated a chirp signal generator utilizing an OpenCL design based on an FPGA circuit [3]. A FPGA circuit was also implemented in the multi-channel position measuring system to improve measurement accuracy [4]. Ultra-wideband radar signals-generated technology was proposed using a two-channel signal generator [5]. Machacek et al. presented a direct digital synthesis-based function generator [6]. Programmable signal generation was studied, and the onboard Digital-to-analog Converters (DACs) were applied to produce programmable sinusoidal outputs for the Nuclear Magnetic Resonance (NMR) device [7]. In addition, research on a signal generator based on the Direct Digital Synthesizer (DDS) chip has been carried out [8,9]. In the field of medical equipment development, researchers created a signal generator for evaluating the electrocardiogram signal processing system [10]. In the field of microelectronics, researchers have developed a four-slope operational square wave/triangular wave generator based on the current feedback operational amplifier (CFOA) [11]. The circuit's properties are that the duty cycle of the output waveform may be modified by current or voltage control, and the oscillation frequency can be regulated separately via external resistors. The signal generator is frequently utilized as a standard signal source in the area of instrument detection, particularly in power detection. Researchers investigated the signal generator of transient power quality and developed a detection platform based on virtual instrument technology [12]. Furthermore, using virtual instrument technology, researchers proposed a computer-based power quality signal generator [13]. Measurements at ultra-low frequencies were investigated, and a laser calibration system based on a PULSE Fast Fourier Transformation (FFT) Analyzer for accelerometer frequency measurement was developed [14]. Researchers in the realm of Micro Electronic Mechanical System (MEMS) have simulated and produced an ultrasonic signal generator based on the electrostatic cantilever of MEMS [15]. Furthermore, the signal generator has vital applications in time and frequency detection and calibration, particularly in the area of clock and crystal oscillator calibration [16]. Time and frequency calibration technology is an essential area of electronic measuring technology. High-precision time and frequency calibration technology are strongly connected to the subject of engineering technology. Currently, the frequency resolution of a signal generator employed in the area of time calibration can only be adjusted to 1μHz, particularly when the frequency is less than 100Hz, limiting the use of signal generators.

In this study, a high-precision frequency source based on the DDS chip and FPGA circuit is designed to improve the frequency resolution and stability of the signal generator at low frequencies. The signal source may create a high-precision square wave signal by using a rubidium atomic clock as the standard clock signal. The technique for improving the device's frequency resolution is theoretically examined and deduced, and the device's circuit design theory is

described. A high-precision frequency counter is used to experimentally verify the device's frequency signal. The experimental results show that the designed frequency source has outstanding accuracy in the frequency range of 1Hz to 10MHz and that the high-resolution control function of a low-frequency signal is achieved by assessing the measurement uncertainty of the frequency source. In this paper, the approach of signal frequency multiplication followed by frequency division is applied to the proposed high-precision frequency source, allowing the frequency resolution to be increased to 1nHz at 1Hz. This is a significant improvement compared to the typical resolution of 1 μHz found in function signal generators available in the market. Furthermore, the theory of frequency multiplication followed by frequency division is first deduced to demonstrate how this method achieves outstanding accuracy for low-frequency square wave signals.

This paper is organized as follows: Section 2 deduces the theory of frequency multiplication followed by frequency division. Section 3 describes the principles of the high-precision frequency signal generator and explains the operational flow chart of the device. Sections 4 and 5 present the proposed high-frequency signal generation circuit and the control circuit for frequency division, respectively. Section 6 demonstrates the measurement results and uncertainty analysis to verify the frequency accuracy of the proposed technique. Lastly, Section 7 provides the obtained conclusions and discusses future works.

2. Theoretical derivation

The optimal resolution of a commonly used function signal generator is 1 μHz, particularly when the low-frequency signals are produced, which restricts the application range of the signal generator to a certain extent. To increase the accuracy of the output signal of the signal generator, we apply the approach of signal frequency multiplication and then frequency division to generate the high-precision low-frequency signal [16]. The atomic clock is utilized as the standard clock in this article to drive the DDS chip, which generates a high-frequency signal. Then the FPGA frequency division circuit is used to realize the output of the high-precision low-frequency signal. The circuit allows the frequency of the output low-frequency square wave signal to be regulated in the 9th significant digit, which increases the low-frequency signal's frequency resolution and accuracy. The exact theoretical derivation approach of this technique is proposed for the first time in this section. Let the frequency of a low-frequency signal be F_L and the frequency of the other high-frequency signal be F_H. The frequency expressions for the two signals are as follows:

$$F_H = f_H(1 \pm U_{arel}) \tag{1}$$

$$F_L = f_L(1 \pm U_{brel}) \tag{2}$$

where f_H and f_L represent the frequency standard values of the high-frequency and low-frequency signal, respectively, while U_{arel} and U_{brel} represent the relative extended uncertainty of the two signals, respectively. Let $F_L = \frac{F_H}{N}$, that is, F_H is the *N* times that of F_L, which gives

$$F_L = \frac{F_H}{N} = \frac{f_H(1 \pm U_{arel})}{N} = \frac{f_H}{N} \pm \frac{f_H U_{arel}}{N} = f_L \pm f_L U_{arel} \tag{3}$$

It gives U_{brel}=U_{arel} according to the above formula. That is, the low-frequency signal can be generated by dividing the frequency of the high-frequency signal, and the frequency accuracy of the high-frequency signal can be conveyed to the low-frequency signal. According to this idea, the frequency resolution of the low-frequency signal can be regulated with high precision. The high-frequency signal, for example, is a 10MHz high stable frequency signal produced from the rubidium atomic clock, with a frequency accuracy which is $U_{arel} = 5 \times 10^{-11}$. If a 1Hz signal with high stability is desired, it can be obtained by formula (3), which gives $1Hz = \frac{10 \times 10^6 (1 \pm 5 \times 10^{-11})}{10^7} Hz = 1 \times (1 \pm 5 \times 10^{-11}) Hz$. As a result, the frequency precision of the low-frequency signal can theoretically approach the atomic clock's frequency accuracy. This approach can solve the problem that the frequency resolution of the present function signal generator is not high at low frequencies. The frequency resolution of the present function signal generator at 1Hz can be raised from 1 μHz to 1nHz. It is important to note that the frequency accuracy of the low-frequency signal is also related to the relevant circuit, which will influence the frequency accuracy of the output signal to some degree. The uncertainty of the designed high-precision frequency source will be investigated and addressed further in this study.

3. Principles of the system

A high-precision frequency signal generator is developed in this article. A schematic representation of the proposed high-precision frequency signal generator is shown in Fig. 1.

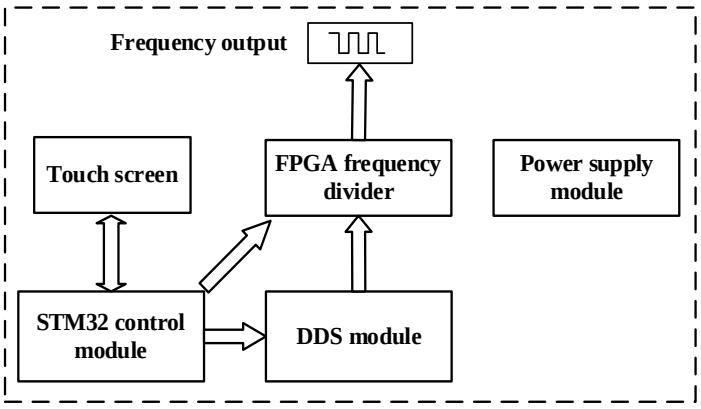

Fig. 1 Schematic diagram of the proposed high-precision frequency signal generator.

The device is equipped with an external touch screen as the human-computer interaction interface. The STM32 (STMicroelectronics) control module is linked to the external touch screen via an RS232 serial connector to enable data transmission and receiving. The external touch screen allows users to configure the frequency settings of the STM32 control module. After receiving the frequency setting instructions, the STM32 control module initiates communication with the DDS module to set the DDS module's output frequency. Simultaneously, when the FPGA module receives the frequency signal produced by the DDS module, it performs the frequency division function for the DDS module's output frequency signal in accordance with the STM32 module's control instructions. Finally, the high-precision square wave frequency signal is output by a pin of the FPGA module. The function of the power supply module is to convert the 220V Alternating Current (AC) into the Direct Current (DC) voltage required by each system module.

Fig. 2 shows the working flow chart of the device. This flowchart illustrates the operation process of the device. It encompasses the initialization process of the STM32, FPGA, serial port function, and AD9854 modules. After initialization, the device needs to wait for the user to set the frequency parameter and decide whether or not to perform multiplication and division operations based on whether the frequency parameter is greater than or equal to 100kHz. First, after the high-precision frequency signal generator is powered on, the system simultaneously initializes the STM32 main control module and the FPGA frequency division circuit. The communication function of the RS232 serial port and the DDS module, which is constructed using the AD9854 chip circuit mentioned in its datasheet, is then initialized [17]. Following the startup described

above, the device waits for the user to specify the frequency settings on the touch screen.

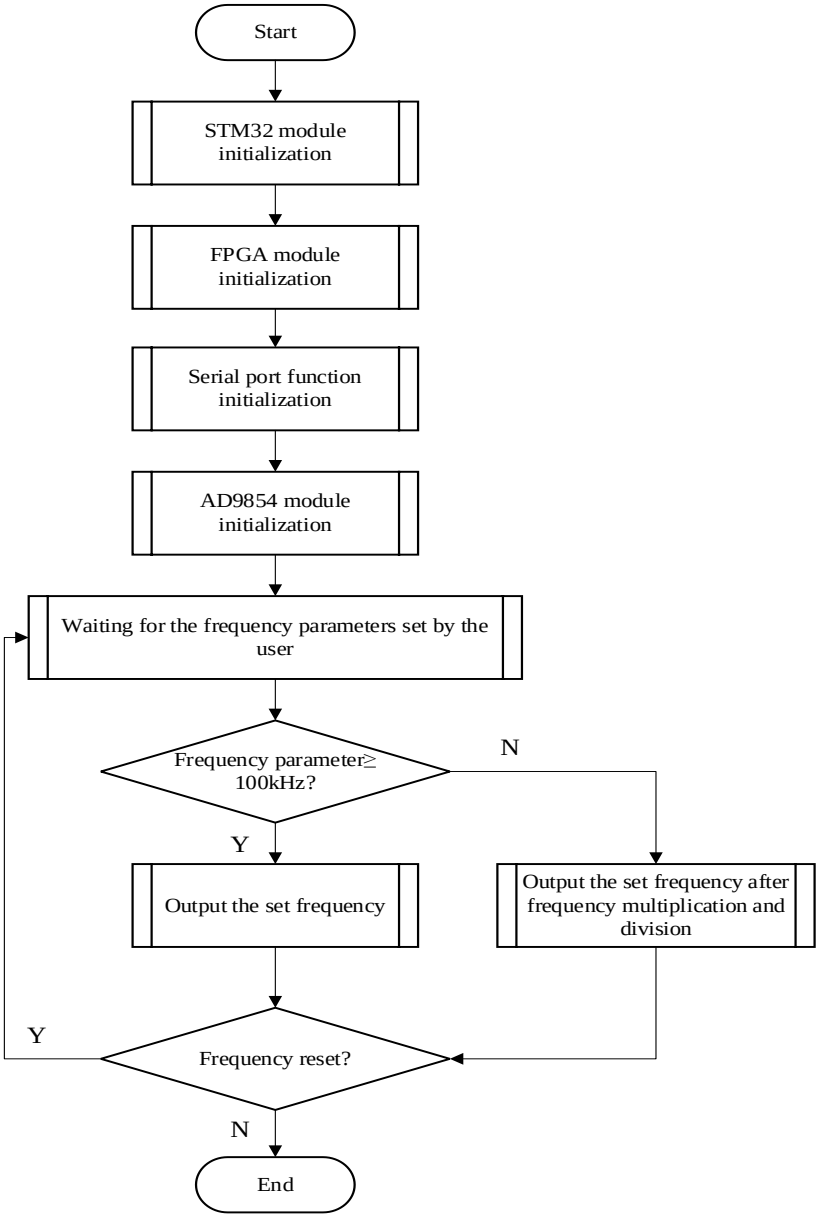

Fig. 2 Operational flow chart of the device.

If the selected frequency is equal to or greater than 100kHz, the user-specified frequency signal is sent straight via the DDS and FPGA modules, bypassing frequency multiplication and frequency division. Otherwise, the STM32 module

instructs the DDS module to execute frequency multiplication and then instructs the FPGA module to split the DDS module's frequency signal and output the user-specified frequency signal. If the user wants to reset the signal frequency, the system will go through the same steps as before.

4. High-frequency signal generation circuit

A high-frequency signal generation circuit is designed to generate the required high-precision high-frequency signal using the proposed signal frequency multiplication and frequency division theory. The high-frequency signal generated by the circuit has a frequency range of 100kHz to 10MHz. The Advanced RISC Machines (ARM) processor is used in the design of the high-frequency signal generation circuit to control the DDS chip, which generates the high-frequency signal. A rubidium atomic clock is used as an external reference frequency for the DDS chip to ensure the accuracy of the output frequency of the signal generation circuit. After being processed by the FPGA frequency division module, the high-frequency signal generated by the signal generation circuit can output a high-precision square wave signal with a frequency range of 1Hz to 10MHz, and the frequency resolution for low-frequency signals below 100Hz can reach the 9th significant digit. The system uses an STM32f407 processor as the primary control unit to drive and operate the DDS chip [18]. The cortex M4 core processor features 192kb SRAM, 1024KB flash, 6 serial ports, and 112 general Input/Output (I/O) ports. The STM32f407 processor has an operating frequency of 168MHz, which can fulfill the control needs of controlling the DDS device. Simultaneously, one of the processor's serial ports is used for communication with the touch screen in order to accomplish the function of accepting user commands and facilitating human-computer interaction. Because of its excellent bandwidth, phase consistency, and high precision in frequency synthesis, the DDS chip may be employed as a steady analog signal source. The system employs a high-performance DDS chip AD9854 built by the ADI (Analog Devices, Inc.) company to create a square wave signal with a frequency range of 100kHz to 10MHz. With dual integrated 12-bit DACs, an ultra-high speed comparator, and a 4× to 20× programmable reference clock multiplier, dual 48-bit programmable frequency registers, dual 14-bit programmable phase offset registers, 12-bit programmable amplitude modulation, and output shaped keying function, the chip's internal clock rate can reach 300MHz. When an external atomic clock is used as the standard clock source, the AD9854 can create a frequency-programmable square wave signal with excellent stability using a 48-bit frequency accumulator and an internal phase accumulator. The schematic diagram of the high-frequency signal generation circuit constructed in this project is shown in Fig. 3. The STM32 control unit's common I/O interface is linked to the DDS

module's control interface, address interface, and data interface through a current limiting resistance network, and the DDS module's S/P select interface is set to the high level to enable parallel programming. The REFCLK interface of the DDS module is used for reference clock input. The external rubidium atomic clock is used as the standard clock signal to operate the DDS module in this case. The 10MHz standard frequency signal produced by the external atomic clock is delivered to the DDS module through the SMA (SubMiniature Version A) interface to prevent interference and assure frequency stability of the external reference clock.

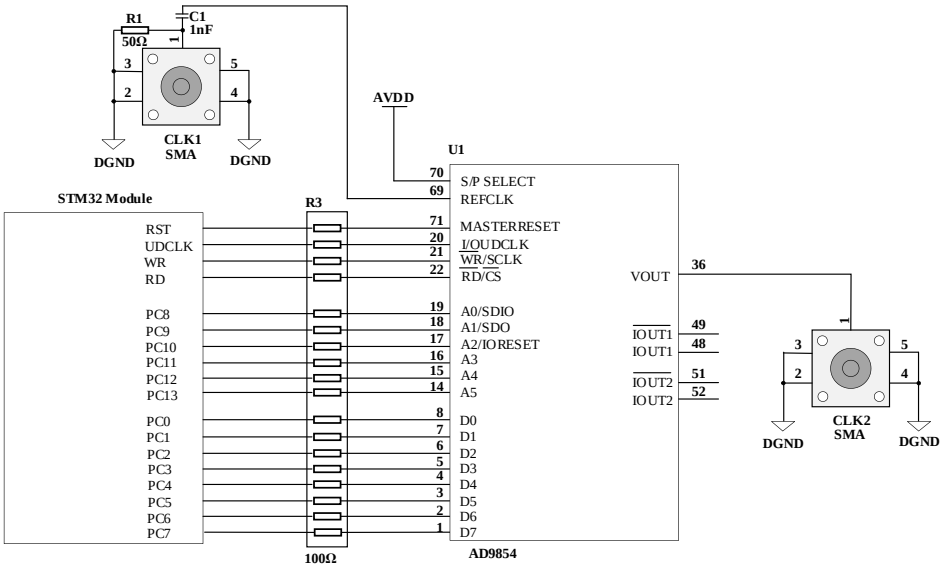

Fig. 3 Schematic diagram of high-frequency signal generation circuit.

Similar to the other DDS devices, the value of the frequency tuning word (FTW) of the AD9854 module can be calculated by the following formula [17]:

$$FTW = \frac{(f_{set} \times 2^N)}{f_{SYSCLK}} \tag{4}$$

where N is the resolution of the 48-bit phase accumulator, f_{set} represents the expected output frequency in Hz, and f_{SYSCLK} represents the system clock frequency in Hz. The frequency tuning word, abbreviated FTW, is often a decimal that must be rounded to an integer before being translated to binary format, which is represented by a 48-bit binary number. The output of the AD9854 module of the high-precision frequency generator is controlled by the instructions supplied by the STM32 module and recorded into the relevant registers of the AD9854 module. The device uses the interface mode of parallel programming between the

STM32 module and the DDS module to simplify the frequency control function of the DDS module. When using the parallel programming interface mode, the S/P select pin of the AD9854 chip must be set to high to enable the parallel I/O mode. The AD9854 chip's I/O interface is compatible with industrial microcontrollers. Its I/O ports have 6 address bits, 8 bidirectional data bits, and write/read control input pins. Fig. 4 depicts the working sequence diagram of the AD9854 module's parallel input. When the STM32 module sends a low level to the pin $\overline{WR}$, the control instructions can be written into the AD9854 chip for programming control, as shown in the picture.

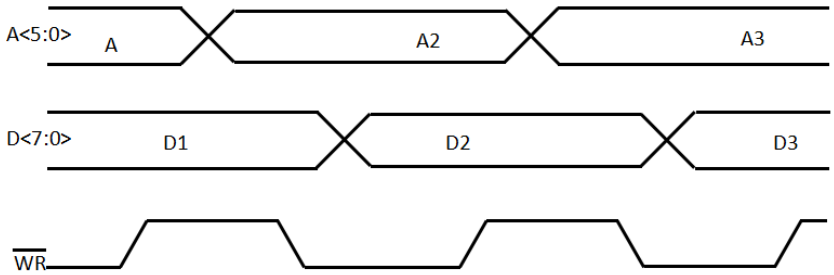

Fig. 4 Working sequence diagram of parallel input.

5. Control circuit for frequency division

The Cyclone FPGA chip realizes the frequency division control circuit, one of the key modules of the high-precision frequency generator. The FPGA device can fulfill low-cost design requirements, has a user-programmable I/O interface, and has significant benefits in parallel computing. In this paper, the EP4CE10 chip is used to design the DDS module's frequency division control circuit, which realizes the frequency division function of the DDS module's output signal and converts the high-frequency signal with high stability into a low-frequency signal [19]. The frequency of the produced low-frequency square wave signal may be regulated down to the ninth significant digit, improving the frequency resolution and accuracy of the signal. The frequency division control circuit is depicted schematically in Fig. 5. The FPGA module receives frequency division instructions from the STM32 module through the standard I/O ports and is coupled to the output frequency port of the DDS module via the SMA interface. The driving clock of the frequency division control circuit is set at 50MHz. The FPGA module implements the frequency division function for signals ranging from 100kHz to 1MHz but does not perform frequency division processing on signals above 1MHz.

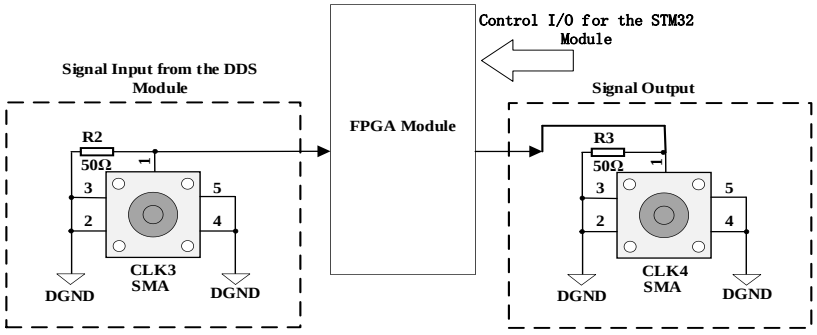

Fig. 5 Schematic diagram of frequency division control circuit.

6. Measurement results and uncertainty analysis

The uncertainty of the output frequency of the designed signal generator is experimentally measured and studied in this work. The frequency measurement standard in the experiment is a pendulum frequency counter CNT-91, and the accuracy of its external rubidium atomic clock is 5×10^{-11}. The measured object is the output frequency of the high-precision signal generator designed in this study. During the measurement, the frequency output terminal of the measured signal generator should be connected to the frequency counter CNT-91's input terminal A via a coaxial cable. The signal generator's output frequency should be set to 1Hz and the frequency counter should be set to the frequency measuring function. The measurement interval is set to 5 seconds. The frequency value produced by the tested device should be noted. The output frequency error of the signal generator under test is computed using the following formula

$$e = f_x - f_p \tag{5}$$

where e is the output frequency error of the tested signal generator, f_x is the output frequency value of the tested signal generator, and f_p is the frequency value measured by the frequency counter. According to the above formula, f_x and f_p are the primary causes of the measurement uncertainty for the frequency error of the measured signal generator. The frequency accuracy analysis of the developed signal generator in this paper is based on the above two factors.

6.1 Standard uncertainty introduced by the tested signal generator

The source of the standard uncertainty of the output frequency of the signal generator is mainly caused by the repeatability of its output frequency. By using the uncertainty evaluation method, the output frequency of the tested device

is measured 21 times under the repeated conditions. The measurement results are shown in Fig. 6.

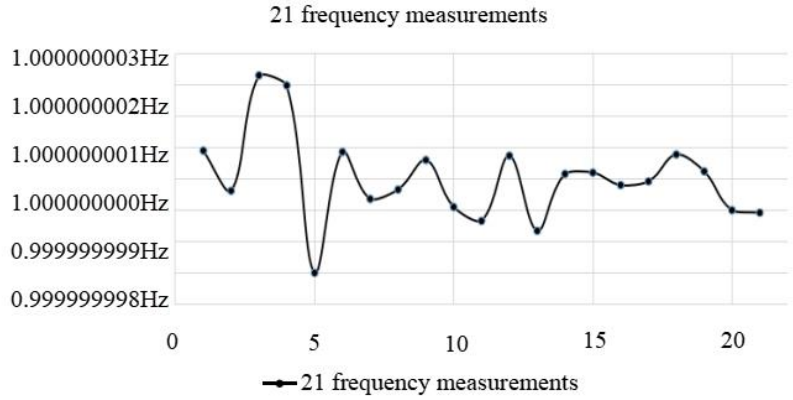

Fig. 6 21 frequency measurements at 1Hz.

The average value of the measurement results is $\overline{f_x}$=1.0000000005133Hz. The standard deviation of a single experiment according to the Bessel formula can be written as $s=\sqrt{\frac{\sum_{t=1}^{n}(f_{xt}-\overline{f_x})^2}{n-1}}$=7.089×10^{-10}$Hz$. The standard uncertainty of u_1 is $u_1=\frac{s}{\sqrt{21}}=1.547\times10^{-10}Hz$ with degrees of freedom $v=n-1=20$, where n is the number of measurements (in this case, n=21).

6.2 Standard uncertainty introduced by the frequency counter

According to the equation (5), the uncertainty source of the measured frequency f_x also includes the time base error and the uncertainty component introduced by the resolution of the frequency counter. As a result, the external rubidium atomic clock is employed as the frequency counter's reference clock in the project. Therefore, the measurement error of the external rubidium atomic clock is 5×10^{-11}. When the measured frequency is 1Hz, the error is 5×10^{-11}Hz. According to the calculation of uniform distribution, if the half-width is $a=\pm2.5\times10^{-11}$Hz and the coverage factor is $k=\sqrt{3}$, the uncertainty introduced by the external time base of the frequency counter is $u_2=a/k=1.443\times10^{-11}$Hz.

Furthermore, the uncertainty component introduced by the resolution of the frequency counter is considered. According to the instrument manual, the frequency resolution of the equipment reaches the 12th significant digit. When the measured frequency is 1Hz, the resolution is 1×10^{-11}Hz, and the half-width of the

interval is $a=\pm 5\times 10^{-12}$ Hz. If the coverage factor is $k=\sqrt{3}$ according to the uniform distribution, the uncertainty component introduced by the resolution of the frequency counter is $u_3=a/k=2.887\times 10^{-12}$ Hz.

6.3 Combined standard uncertainty

The sensitivity coefficient can be obtained from equation (5) as $c_1=\frac{\partial e}{\partial f_x}=1$ and $c_2=\frac{\partial e}{\partial f_p}=-1$. Since the estimation values of covariance for u_1, u_2 and u_3 are all zeros, the combined standard uncertainty is given by $u_c=\sqrt{c_1^2u_1^2+c_2^2u_2^2+c_2^2u_3^2}=1.554\times 10^{-10}$ Hz.

6.4 Extended uncertainty

Taking the confidence factor $k=2$, the expanded uncertainty can be obtained as $U_{95}=k_{95}u_c\approx 3\times 10^{-10}$ Hz, and its relative uncertainty is $U_{rel}=\frac{U_{95}}{f_x}\approx 3\times 10^{-10}$.

As shown in Fig. 6, the set frequency value is 1Hz, and the average frequency value of the square wave signal output by the high-precision standard frequency source is $\overline{f_x}$=1.0000000005133*Hz* . As a result, the number of programmable frequency digits approaches the ninth significant digit. When the specified frequency value is 1.000102038 Hz, Fig. 7 shows the 21 measured values of the device's output frequency, with the average value being 1.0001020379448Hz. It can be seen that the effective frequency bits of the high-precision frequency source designed in this paper can reach 9 digits.

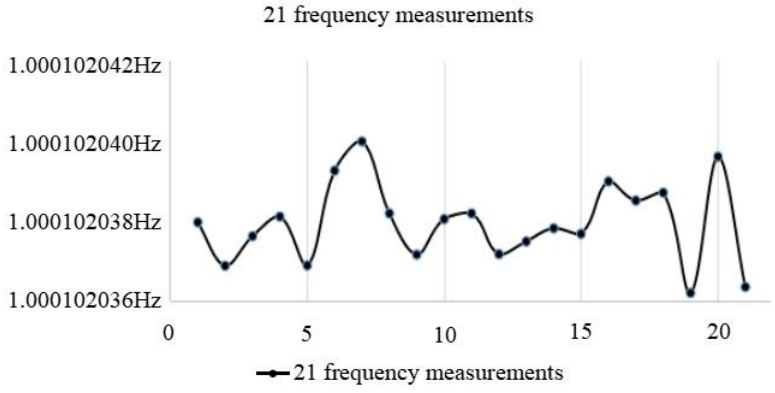

Fig. 7 21 frequency measurements at 1.000102038 Hz.

7. Conclusions

In this paper, we conduct the research work based on an atomic clock, the high-precision DDS chip, and the FPGA frequency division circuit and develop a high-precision frequency source based on the frequency division technology to achieve higher frequency resolution for frequency source design. We theoretically deduce the feasibility of this technology. The high-frequency signal generation circuit and FPGA frequency division control circuit are designed based on an STM32 chip and an AD9854 chip, and the working principle of these circuits is described in detail. Finally, the designed high-precision frequency source is tested by the high-precision frequency counter based on an atomic clock. Through the uncertainty analysis of the experimental results, it is found that the high-precision frequency source designed in this paper is able to output a stable square wave signal, and its programmable effective frequency bits can reach nine digits, particularly at low frequencies such as 1Hz, where the frequency resolution can reach 1nHz. As a result, the output frequency range of the device is 1Hz to 10MHz with nine programmable digits. The theoretical analysis and the device designed in this paper are of great significance to the time-frequency measurement technology. The DDS chip design might benefit from using the proposed theory in the study to increase its frequency accuracy. It can also be applied to the design of the function signal generator to improve its programmable resolution of frequency, which is typically 1 μHz. It must be noted that future efforts to create a high-precision frequency source may concentrate on generating programmable sine waves with high accuracy at various specified frequencies, which is still a challenge.

Acknowledgments

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