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SUSTRATE LEAKAGE COMPENSTAION TECHNIQUE FOR LOW QUIESCENT CURRENT BANDGAP VOLTAGE REFERENCES

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Improving the accuracy of the output voltage of a regulator implies the usage of superior order compensated internal voltage reference and techniques for trimming its output voltage after fabrication. Some of these trimming techniques may affect the temperature behaviour of the reference because of the substrate leakage currents. This paper presents a new method for compensating the substrate leakage current for a voltage references trimmed with Zener zap diodes.

Keywords: bandgap, voltage reference, substrate leakage current

1. Introduction

A high performance application requires high precision supply voltages. This can be obtained by using an accurate voltage regulator. Since the accuracy of the output voltage of a regulator is given mainly by the accuracy of the internal reference, design techniques that minimises the variation with temperature should be used as well as trimming networks that allow the modification of the output voltage after fabrication, at wafer level or at package level.

Several trimming techniques have been developed over the time [1][2]. Depending on the structures available in a specific technology, one of the following techniques can be used to adjust the output voltage of a regulator: fusible links, Zener zap and laser trimmed resistors. In a standard BiCMOS process the post fabrication adjustments are done with zapping diodes as the method is inexpensive and reliable. Despite of these advantages, this technique may impose severe limitations in special applications like the ones from the automotive market. In these cases, the maximum operating temperatures are specified usually up to $150^{\circ}C$ or even higher. The substrate leakage currents have in this range of temperatures an important contribution to the precision of the output voltage and special techniques have been developed to minimize or compensate the effect of these currents [3]. Zap diodes used for adjusting at wafer

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level the output voltage of the regulator also introduce leakage currents into the internal reference which cannot be compensated using the method described in [3]. The effect of the trimming network is visible especially for low current voltage references.

This paper presents a new method for compensating the substrate leakage current effect of the zapping structures on the bandgap voltage reference of a regulator. Chapter 2 presents the Brokaw bandgap reference used. The trimming technique is shown in chapter 3. Chapter 4 describes the effect of the leakage current of the zap diodes and then a new method for eliminating this influence is proposed. Chapter 5 presents the simulations results. Last chapter contains the conclusions of this paper.

2. Brokaw bandgap reference

Fig. 1 shows the architecture of the well-known Brokaw bandgap voltage reference. The schematic comprises a start-up circuitry formed by Q_4, Q_5, Q_6 transistors and R_3 resistor, a proportional to absolute temperature (PTAT) current generator formed by Q_1, Q_2 and R_2, the biasing mirror formed by M_1 and M_2 transistors, a leakage compensation transistor by Q_3 for the PTAT generating current formed and the output stage formed by M_3 transistor.

The reference voltage is given by

$$V_{REF} = V_{BE1} + I_1 \cdot R_1 \quad (1)$$

where I_1 is the current through R_1 resistor, and V_{BE1} is the base emitter voltage of Q_1 transistor for which the temperature behaviour is described by [4]

$$V_{BE1} = V_{g0} - \frac{V_{g0} - V_{BE1}(T_0)}{T_0} T - (\eta - 1) V_T \ln\left(\frac{T}{T_0}\right) \quad (2)$$

where V_{g0} represents the extrapolated bandgap voltage at 0K, T_0 is the reference temperature, usually considered 300K, η is a process dependent parameter and V_T represents the thermal voltage

$$V_T = \frac{kT}{q} \quad (3)$$

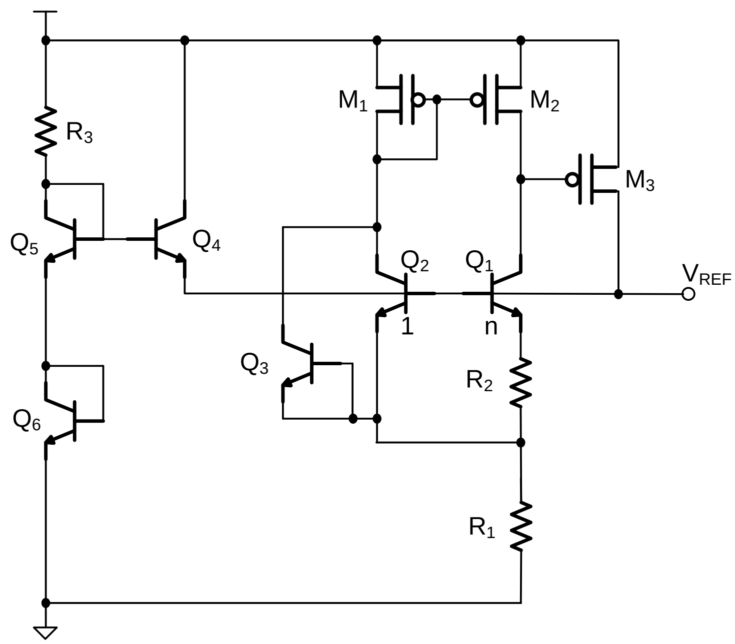

Fig. 1. Brokaw bandgap voltage reference

The PTAT current through R_2 resistor, generated by the difference of the base emitter voltages of Q_1, Q_2 transistors, is given by

$$I_{PTAT} = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_T \ln n}{R_2} \tag{4}$$

where n is the ratio of the emitter areas of the two transistors. It has been taken into account that the M_1, M_2 current mirror forces equal currents in the collector of Q_1, Q_2 transistors.

As a consequence, the expression (1) of the reference voltage becomes

$$V_{REF} = V_{BE1} + 2\frac{R_1}{R_2} V_T \ln n \tag{5}$$

From (3) and (5) the variation of the reference voltage in temperature is shown

$$V_{REF}(T) = V_{g0} - \frac{V_{g0} - V_{BE1}(T_0)}{T_0} T - (\eta - 1)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) + 2\frac{R_1}{R_2}\frac{kT}{q}\ln n \tag{6}$$

First order compensation of the thermal characteristic of the reference voltage can be achieved by mutual cancelation of the second and forth terms in (6)

$$2\frac{R_1}{R_2}\frac{k}{q}\ln n-\frac{V_{g0}-V_{BE1}(T_0)}{T_0}=0 \tag{7}$$

Hence, the temperature variation of the reference voltage is given by

$$V_{REF}(T)=V_{g0}-(\eta-1)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \tag{8}$$

The substrate leakage current of Q_1, Q_2 transistors introduces a new increasing voltage with temperature in (8) [3]

$$V_L=2\frac{R_1}{R_2}V_T\ln\left[1+(n-1)\frac{I_L}{I_{PTAT}-nI_L}\right] \tag{9}$$

For high bias currents ($I_{PTAT}>>nI_L$), $V_L\cong 0$. At low currents level and at elevated temperatures the influence of the substrate leakage current on the reference voltage increases. Thus, $V_{REF}(T)$ will increase significantly for temperatures above 110˚C [3].

In order to compensate the effect of the substrate leakage current of the bipolar transistors, Q_3 has been added in the circuit (Fig. 1). The additional voltage from (9) is now eliminated from the expression of the reference voltage as the collector currents of Q_1, Q_2 remain equal for the whole temperature range [3].

3. Trimming network

Besides the variation with temperature, the output voltage of a reference will exhibit small deviations from the nominal value because of the technological process imperfections like device mismatches, resistor tolerances and package shifts effects. For precision voltage references, usually a trimming network is used in order to minimize these variations [1].

Hence, in Fig. 2 shows a typical trimming network for a Brokaw bandgap voltage reference in a BiCMOS process using zapping diodes. R_1 and R_2 resistance are divided in two asymmetrical parts. The smaller ones are in places in parallel with Dz_1 and Dz_2 diodes. These zapping diodes provide the possibility to shunt each one of the R_{12} and R_{22} resistors so as to adjust the reference voltage [1].

Note that the voltage across R_{12} and R_{22} is in the range of 1 to 10mV. Hence, the two diodes are blocked.

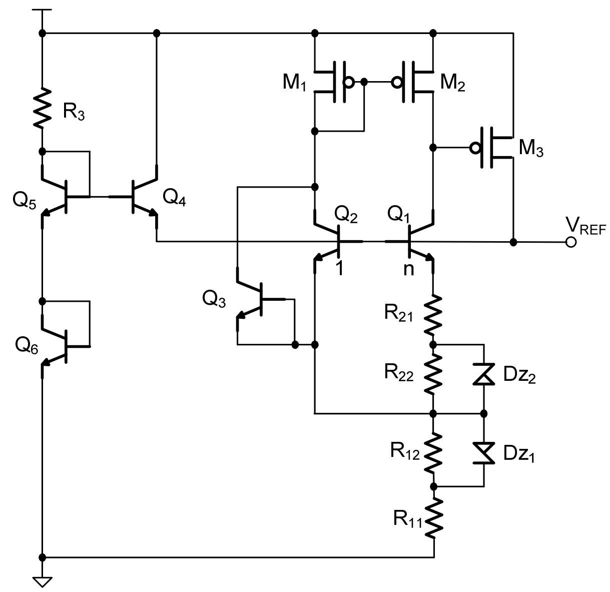

Fig. 2. Brokaw bandgap voltage reference with trimming network

By shunting resistor R_{22}, the reference voltage becomes :

$$V_{REF}^{'} = V_{BE1} + 2\frac{R_1}{R_{21}} V_T \ln n \tag{10}$$

Thus, the variation from the nominal value is given by

$$\Delta V_{REF}^{'} = V_{REF}^{'} - V_{REF} = 2\left(\frac{R_1}{R_{21}} - \frac{R_1}{R_2}\right) V_T \ln n = 2\frac{R_1}{R_2}\frac{R_{22}}{R_{21}} V_T \ln n \tag{11}$$

It is obvious that by shunting of R_{22} will lead to an increase of the reference voltage.

A decrease of the reference voltage is obtained when R_{12} is shunted. Therefore, from (5) results

$$V_{REF}^{"} = V_{BE1} + 2\frac{R_{11}}{R_2} V_T \ln n \tag{12}$$

and, the variation from nominal value is

$$\Delta V_{REF}^{"} = V_{REF}^{"} - V_{REF} = 2\left(\frac{R_{11}}{R_2} - \frac{R_1}{R_2}\right)V_T \ln n = -2\frac{R_{12}}{R_2}V_T \ln n \qquad (13)$$

The variation in (13) is negative. Thus, by shunting of R_{12} the output voltage of the reference can be decreased.

As a conclusion, by using the trimming network proposed in circuit from Fig. 2 both positive and negative variation of the output voltage due to process variations can be compensated. For high precision references, more than two trimming steps can be used by increasing the number of zapping diodes.

4. Influence of the zap diodes on the bandgap

The zap diodes Dz_1 and Dz_2, as the bipolar transistors, have parasitic p-n diodes to substrate. Fig. 3 shows these parasitic diodes and the proposed circuit for compensating the substrate leakage current. This circuit is formed by M_3, M_4 transistors and D_3 diode.

The reverse current density of the substrate diodes is given by [5]

$$I_L = AT^{3-\frac{\gamma}{2}} e^{-\frac{Vg_0}{kT}} \qquad (14)$$

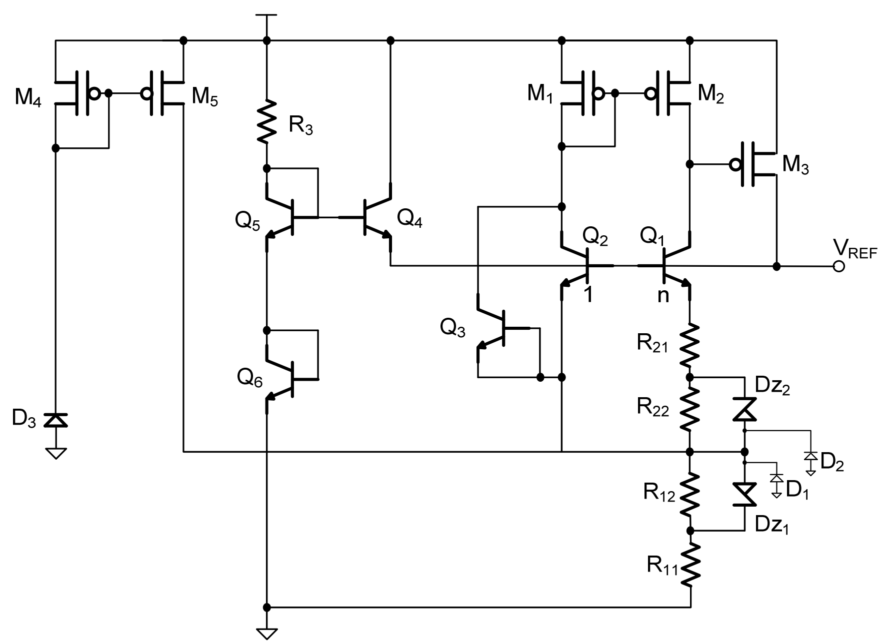

Fig. 3. Brokaw bandgap voltage reference with trimming network

The current through R_1 resistor becomes

$$I_1 = 2I_{PTAT} - I_L \tag{15}$$

The reference voltage is now given by

$$V_{REF} = V_{BE1} + 2\frac{R_1}{R_2}V_T \ln n - I_L R_1 \tag{16}$$

Using (8) and (14), the variation with temperature of the voltage reference is

$$V_{REF}(T) = V_{g0} - (\eta - 1)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) - AT^{3-\frac{\gamma}{2}} e^{-\frac{Vg_0}{kT}} R_1 \tag{17}$$

At high temperatures, the exponential term in (17) becomes significant.

To cancel this variation the area of the D_3 (a substrate diode, too) has to be equal to the sum of the areas for both zap structures. D_3 is reversed biased and M_4 and M_5 transistors create a current mirror that injects into R_1 resistor a current equal to the sum of zapping diodes leakage currents. As a result the expression (8) becomes again valid as the substrate leakage current cancelation has been achieved for the zapping structures.

Note that this technique can be used to compensate the leakage currents of Q_1 and Q_2. In this case the area of the new substrate diode should be equal the area difference of transistors Q_1 and Q_2.

6. Results

The Brokaw bandgap reference discussed above with and without all the compensation circuits (see Figs. 1-3) have been simulated using a single-metal, single-poly BiCMOS technology. The nominal supply voltage is *5V* and the operating temperature range is *-40˚C* up to *175 ˚C*. A nominal reference voltage of *1.213V* has been obtained at *25˚C*. A current consumption of *0.65mA* has been achieved at *25 ˚C* and the maximum value of the quiescent current over the whole temperature range is *0.9mA*.

Fig. 4 presents the temperature dependence of the output reference voltage with and without trimming circuits.

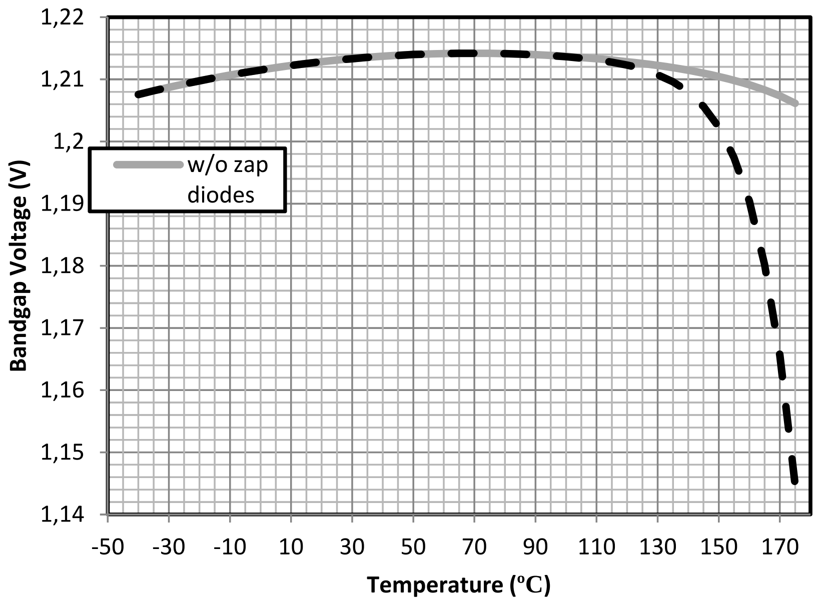

Fig. 4 Reference voltage function of temperature for the bandgap with and without zapping structures

The variation for the reference without trimming (Fig. 1) over the whole temperature range is *8mV*. By adding the zap structures for trimming (Fig. 2) the output voltage the temperature variation increases significantly. For temperatures above *120˚C* the influence of the substrate leakage current of zap diodes is visible as the output voltage decreases with *65mV*. Thus, a total deviation of *69mV* is obtained for circuit from Fig 2.

Fig. 5 shows the simulation results for the bandgap reference with zapping diodes and total substrate leakage current compensation (Fig. 3). The variation of the output voltage obtained is only *8.4mV*.

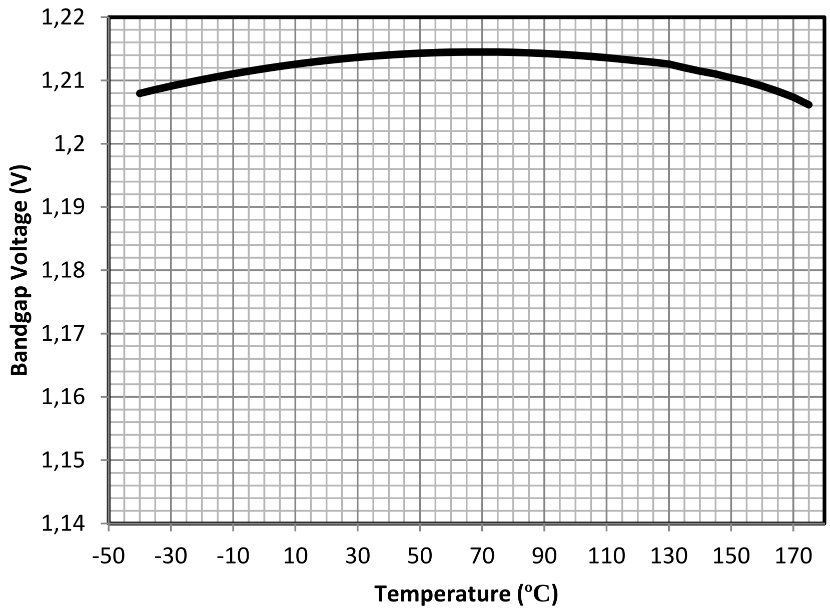

Fig. 5 Reference voltage function of temperature for the bandgap with zapping structures and total leakage current compensation

7. Conclusions

A new method for compensating the leakage current of the bipolar devices for bandgap voltage reference in a BiCMOS technology has been presented. Two methods to cancel the leakage current has been discussed.

To compensate the leakage current of the zap diode used for trimming the voltage reference, a new circuit is proposed. With this circuit, the change in the voltage reference decrease for the whole temperature range (*-40˚C* up to *175 ˚C*) from *69mV* to *8.4mV*. This variation is close to the variation of a similar bandgap architecture without any trimming option. Moreover, the proposed circuit can be also used to compensate the leakage current that affects the PTAT generating current.

The proposed method can be used for reference voltages from voltage regulators in automotive applications.

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