NEW MODULAR MULTILEVEL CURRENT SOURCE INVERTER WITH MINIMUM NUMBER OF COMPONENTS

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In this paper a novel multilevel current source inverter structure is proposed. This inverter is likely to be used in low/medium power applications. The proposed topology is analyzed and then compared with conventional inverters in order to validate the superiority of the proposed inverter. In this topology, all the desired current levels can be obtained using lower number of circuit devices. The number of required circuit devices is an essential factor, affecting technical and economic aspects of the system. The overall costs, circuit size, reliability and the control complexity are dependent directly to the number of required elements, including DC current sources, power semi-conductor switches and related gate driver circuits of switches. The proposed inverter is simulated to validate its practicability. Also, the experimental results are provided to demonstrate the good performance of the suggested converter. The simulation and experimental results are in good agreements which show the effectiveness of the proposed inverter.

Keywords: Multilevel Current Source Inverters, Symmetric Inverter, Reduction of Circuit Components

1. Introduction

Since the first concept of multilevel inverter was introduced in early 1980s by Nabae et al., there have been intense investigations devoted to the multilevel inverters. Multilevel output waveform offers several essential merits. In this regards, the magnitude of fundamental harmonic, the quality of output power and the efficiency of overall system are increased. Also, the THD value, power losses and voltage/current variations versus time are lowered. Staircase output voltage/current of multilevel inverters is provided using several DC links connected to the input side [1-3]. As the number of steps in the output waveform increases, it reaches nearly sinusoidal waveform, and, hence, the mentioned advantages will be improved as well. Generating sinusoidal waveform by

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synthesizing DC inputs is the main aim of multilevel inverters [4]. Multilevel inverters are employed in many applications such as Flexible AC Transmission Systems and renewable energy resources [5, 6]. To qualify the output current/voltage waveform of multilevel inverters, different modulation strategies have been proposed, which improve the performance of these inverters [9-11]. Some of popular switching strategies are, different pulse width modulation (PWM) techniques and space-vector PWM schemes are proposed to improve the output current/voltage harmonic spectrum [7-8]. Different international standards, like IEEE-929, IEEE-1547, and EN-61000-3-2 confirm inverter output power quality i.e. harmonic spectra and so, THD of output voltage/current. Multilevel inverters are divided into two categories, multilevel voltage source inverters (MVSIs) and multilevel current source inverters (MCSIs). The MCSI delivers AC current waveforms from DC current sources to the load, while MVSI has DC voltage links and generates AC voltage waveform. Mostly in distributed generation units, grid connected inverters transform DC power to AC power which is fed into the power grid. In order to link AC and DC sides in power grid, grid connected MCSI can be a suitable choice. Simpler control of MCSI is the superiority of this structure than its counterpart, MVSI. The grid connected MCSI can buffer the output current from the grid voltage fluctuation, generates a predetermined current to the power grid without AC current feedback loops, and can achieve a high-power factor operation. Because of MCSIs inherent short circuit protection abilities, grid voltage can't affect the output current [12]. Unfortunately, few MCSI topologies can be addressed in literatures. Paralleling several three-level H-bridge CSIs is a common way to generate multilevel current waveform, called CHB. Similar to its counterpart, cascade CHB, the major problem related to them, are their circuit complexity, high number of power switches and a great number of auxiliary DC sources [13]. Another approach is a multi-cell topology based multilevel CSI, which the main drawback of this topology is the existence of bulky intermediate inductors causes a complex balancing control of the intermediate current level [14]. Although some methods that have been proposed can solve these problems but still using cumbersome inductors will be costly and limit the application of this kind of CSI [14]. Another different multilevel CSI, which employs a single rating inductor cell topology is presented in [15]. The disadvantages of this structure are extra losses and lower efficiency of power conversion due to the existence of cumbersome inductors to achieve the stable intermediate level currents. Higher costs and lower reliability are the results of the high number of components about MCSIs which cause circuit complexity and necessitates complex control scheme of the inverter. So, the main aim of advanced topologies of MCSIs is to reduce the necessity of circuit devices. Therefore, researcher's efforts are mainly focused on reduction of circuit elements [16]. So, a multilevel inverter topology with higher performance and

lower number of required components can be a useful achievement. In this paper, a new modular configuration for the symmetric multilevel current source inverter is investigated. This inverter needs less number of circuit components to provide a large number of steps in comparison with CHB and the presented inverter in [16]. The lower number of devices reduces the costs and circuit size, enhances the reliability and ease the control method. The advantages of the proposed multilevel inverter is validated by provided comparisons. The simulation and experimental results are obtained to confirm the practicability of the proposed inverter.

2. Proposed Topology

The overall view of the proposed inverter is shown in Fig. 1. The proposed inverter consists of *n*-isolated DC current sources. The values of the DC sources are equal, so, the proposed inverter is symmetric. Side effects on the output current quality and producing undesired harmonics due to the inequality in the current steps are the results of inequality in DC current sources. So, producing balanced DC current sources is the most considerable point among all symmetric inverters. As the aim of this study is to propose a new topology for multilevel inverters, the ways to provide the DC current sources, is not taken into consideration.

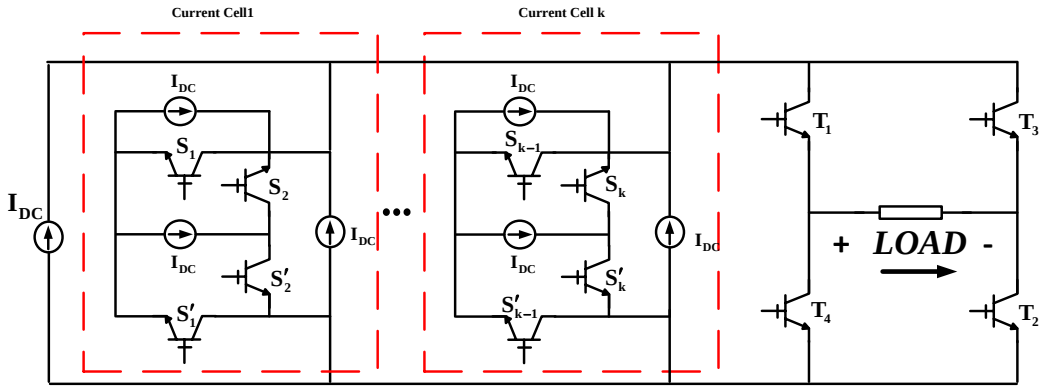


Fig. 1. Proposed multilevel inverter

k-basic cells vocalize the elements of proposed inverter. The basic cell of the suggested multilevel inverter is shown in Fig. 2. As shown, it consists of three equal DC current sources and four semiconductor unidirectional switches which each unidirectional switch is an IGBT. The output current of each basic cell which includes four levels consisting of positive and zero values generated by the complementary of switches $(S_{i1}\ with\ \bar{S}_{i1})$, $(S_{i2}\ with\ \bar{S}_{i2})$. Various switching states of the basic cell of suggested topology, for each output voltage step are represented in Table 1. In Table, 1 shows that the relevant switch is turn-on and 0 points out the

off state. As seen, the proposed inverter contains of H-bridge inverter connected to its output and can provide all positive and negative steps in output waveform.

A provided output phase current is synthesized by individual currents of DC sources. Due to considering the same value (I_{dc}) for all the DC current sources, the proposed topology is called symmetric topology:

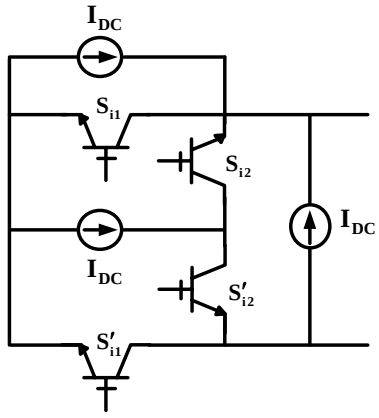


Fig. 2. Basic cell of proposed topology

Table 1

Switching states of basic unit of symmetric proposed topology

State	S_{i1}	S_{i2}	I_o
1	0	1	$+3I_{dc}$
2	0	0	$+2I_{dc}$
3	1	1	$+I_{dc}$
4	1	0	0

The greatest amount of output current ($I_{o,\max}$) of the introduced topology can be calculated by the following equation

$$I_{o,\max} = \sum_{i=1}^{n} I_i = nI_{dc} \tag{1}$$

Here, the number of DC sources is n. A cycle of a typical waveform of the output phase current synthesized is represented in Fig. 3. The output current levels from $-nI_{dc}$ to $+nI_{dc}$ can be produced using different switching combinations of the proposed multilevel inverter cells.

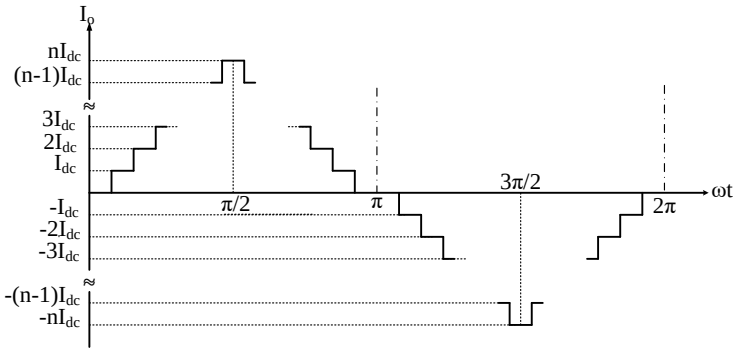


Fig. 3. Typical output current waveform of the proposed multilevel inverter

The number of current levels (m) is given by the following equation:

$$m = 2\frac{I_{o,\max}}{I_{dc}} + 1 \tag{2}$$

It is obvious that to generate m-levels in the output current, n-DC sources are needed. That is:

$$n = \frac{m-1}{2} \tag{3}$$

One efficient way to increase the number of output current levels is to increase the number of cells. However, having k basic cells, it needs n DC links. Each cell consists of three DC current sources. It is clear that, in this configuration n must be in a proper relationship with k . So:

$$n = 3k + 1\,; \quad k = 1, 2... \tag{4}$$

In other words, the values of n and k must gratify the given relationship:

$$k = \frac{n-1}{3} \tag{5}$$

In the proposed inverter, the number of cells (k) is integer. Thus, if an integer number did not result, the nearest integer number is certainly the appropriate solution. Then, the value of n must be updated according to k . The number of switches in the proposed inverter is given by (6):

$$N_{switch} = \frac{4n+8}{3} \tag{6}$$

Since the used switches in the proposed inverter are unidirectional, for each switch one driver is needed. The required switching pulses for each switch are

produced by the related driver circuit. So:

$$N_{Driver} = N_{switch} \tag{7}$$

The other factor of multilevel inverters is the semiconductor device power (*SDP*). The total *SDP* of switches is calculated by the following equation:

$$SDP_{Total} = \sum_{j=1} SDP_{Switch_j} = \sum_{j=1} V_{Switch_j} \times I_{Switch_j} \tag{8}$$

SDP defines the power ratings of semiconductors. Therefore, it is one of the main criterions to evaluate the overall costs of the implemented inverter. So, the total *SDP* of the proposed inverter can be formulated as follows:

$$SDP_{(pu)} = 6n - 2 \tag{9}$$

3. Comparison of the Proposed Inverter with other Multilevel Inverters

The great number of power devices is the main issue among all multilevel inverters which causes intricate circuit, control scheme and also increases the total costs of the inverter with significant reduction in the inverter reliability. In order to distinguish the efficiency of the suggested configuration, a comparison with the cascaded MCSI and the other symmetric MCSI reported in [16] is provided. To compare fairly, maximum output current is assumed equal for all mentioned inverters. A large fraction of the inverter cost is the price of required DC current sources. Therefore, the essential parameter in overall costs is the number of DC current sources. Fig 4 shows the number of DC current sources versus output levels.

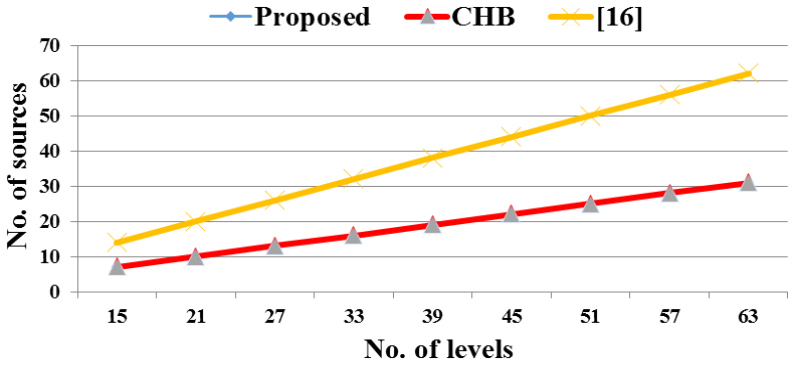


Fig. 4. Number of DC current sources versus number of levels for the proposed topology and the other mentioned solutions

It is obvious from Fig. 4 that the number of DC current sources is lower for the proposed inverter compared to [16]. This number for the proposed inverter is the same as CHB. Due to the efficient effect of the number of DC current sources in overall costs of inverters, the reduced number of sources, can be mentioned as a significant advantage of the suggested inverter. Fig. 5 shows the number of unidirectional switches versus the number of current levels for different inverters.

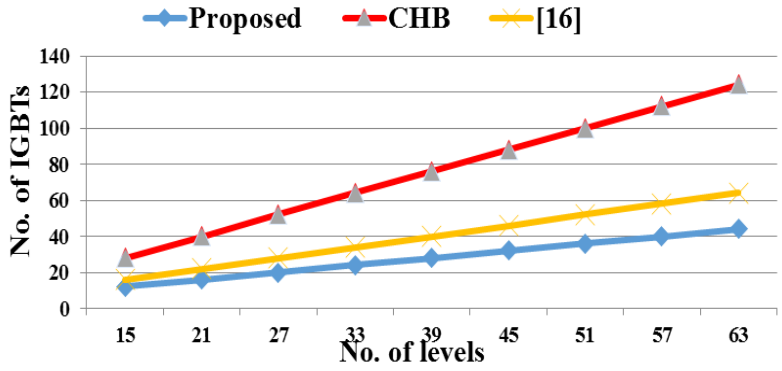


Fig. 5. Number of IGBTs (unidirectional switches) versus number of levels for proposed topology and other mentioned solutions

The comparison progress shows the superiority of the proposed topology over the mentioned configurations from requirements for IGBTs and gate drivers' circuits' point of view. As a result, reductions in the required installation area and costs are obtained for this configuration. Also, the control scheme gets simpler. In addition, the proposed of [16] uses several diodes which increase the costs, but it is not considered in comparisons. Assuming the cost of a diode is a fraction of IGBTs cost, the total expense of [16] would be much more than the proposed MCSI. Another essential parameter which plays a consequential role in overall inverter expense is the power rating of the power switches. Fig. 6 compares the total SDP of the mentioned topologies. Also, it must be noted that the *SDP* of each diode is half of the IGBT. This fact is considered in *SDP* comparison. It is apparent that the ratings of switches applied in low/medium power applications, are almost the same. So, the number of required power switches is more important than the rating of power semiconductor switches in low/medium power applications. So, for the advantages detailed for the proposed inverter and because of the nature of applications where the proposed inverter will be utilized, a bit increase in total *SDP* of the overall system compared to CHB can be neglected, while a considerable reduction in number of switches is achieved.

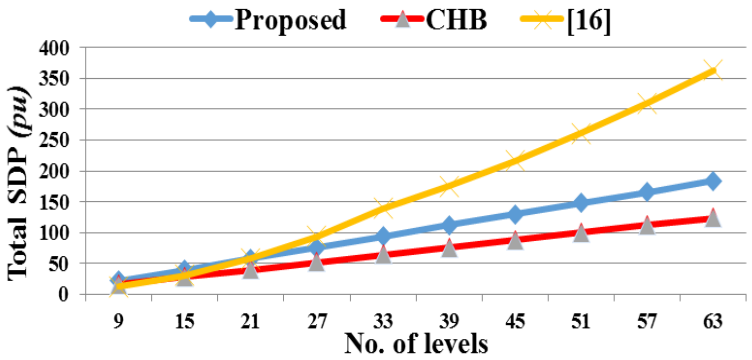


Fig. 6. Total *SDP* value versus output voltage levels for the proposed and the other multilevel inverters

4. Simulation and Experimental Results

Simulation results illustrate the feasibility of the proposed multilevel inverter. MATLAB/Simulink software is used to simulate the proposed inverter. Finally, the experimental results validate the practicability and the good performance of the suggested symmetric MCSI. Table 2 represents the main parameters of implemented circuit.

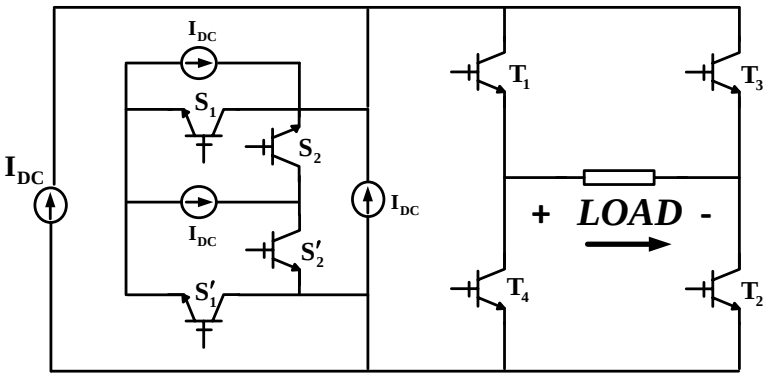
Table 2

Parameters of implemented inverter

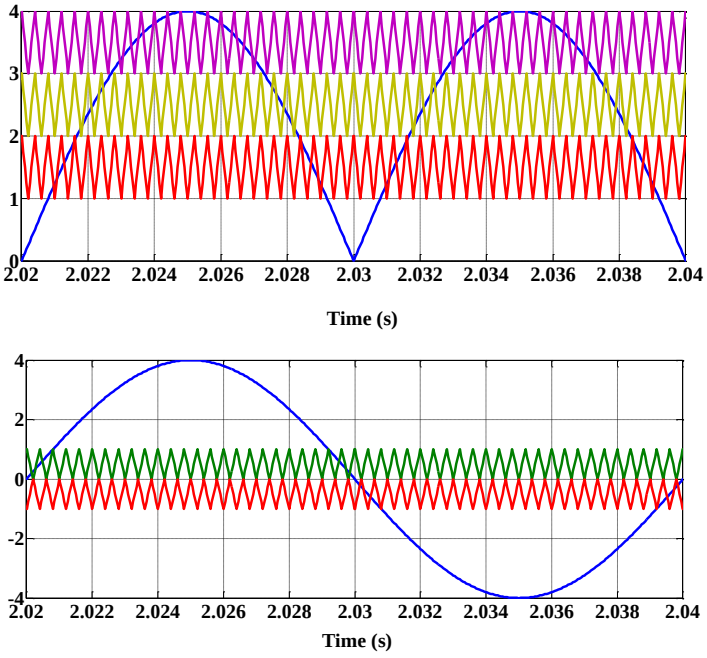
Type of switch	IRF260
Type of MOSFET driver	TLP250
Pulse Generator	DsPIC30F4011
DC Current Sources Magnitudes	0.4A
Load Parameters	22 Ohm & 8mH
Fundamental Frequency	50Hz

Fig. 7(a) shows the circuit diagram of a single phase proposed multilevel inverter. It consists of four DC sources and eight switches which produce a staircase waveform with the maximum current of 2A. A series *R–L* (12 Ω and 5mH respectively) load is considered. In order to produce a high quality of the output current harmonic spectrum, several modulation techniques such as fundamental frequency-switching, sinusoidal PWM, selective harmonic elimination (SHE-PWM), space vector PWM (SV-PWM) are proposed. Among these methods, the most common used is the multicarrier sub-harmonic pulse width modulation (MCSHPWM). The principle of the MCSHPWM method is based on a comparison of a sinusoidal reference waveform, with shifted carrier triangular waveforms. For generating m levels, *m-1* carriers are needed. In the 9-level inverter, to obtain any level of current, four switches should be turned on. Fig. 7(b) shows the modulation waveforms. As shown in Fig. 7(b), the carriers are

triangular waveforms and the reference waveform is sin wave that coordinates the 9-level inverter. The triangular waveforms have the same amplitude, *Ac* and the same frequency, *fc*. The sin reference wave has a frequency *fr* and an amplitude *Ar*. Also the output waveform has a fundamental frequency *fr*. At each instant, the result of the comparison is used in order to generate the proper switching function to give a suitable output current level.



a) circuit diagram of 9-Level multilevel inverter



b) Modulation waveforms for switching

Fig. 7. Circuit diagram and Operation principle of the 9-level proposed inverter

Table 3 defines the switching principle of the symmetric 9-level proposed inverter. In this Table, 1 means that the corresponding switch is turned on and 0

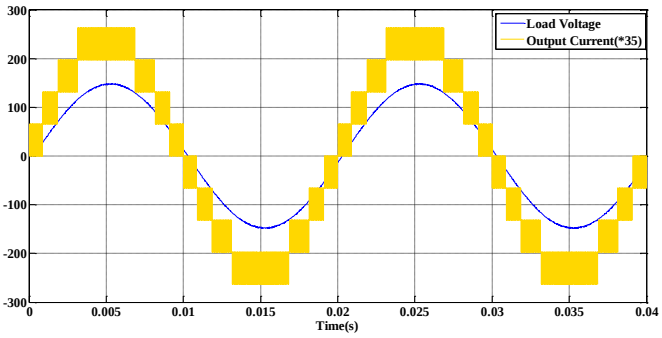
indicates the off state.

Table 3

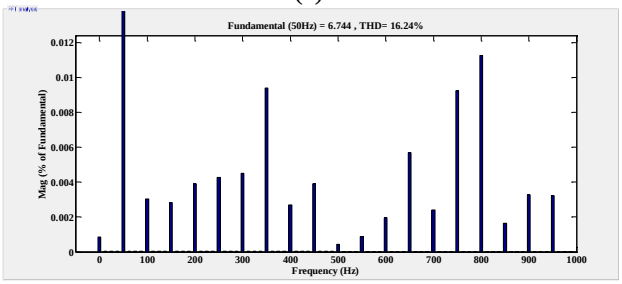
Switching states of proposed symmetric 9-level inverter

Output Voltage	S_1 S_2 T_1 T_2 T_3 T_4
$4I_{dc}$	011100
$3\ I_{dc}$	001100
$2\ I_{dc}$	111100
I_{dc}	101100
0	--0110/--1001
$-\ I_{dc}$	100011
$-2\ I_{dc}$	110011
$-\ 3\ I_{dc}$	000011
$-\ 4\ I_{dc}$	010011

Fig. 8 illustrates the current and voltage waveforms of the 9-level symmetric inverter.



(a)



(b)

Fig. 8. a) Current and Voltage waveforms, b) harmonics content of the proposed symmetric 9-level inverter output current

Fig. 8 shows that the proposed multilevel inverter can generate all current steps for a test case of 9-level symmetric inverter. To validate the practicability of the proposed multilevel inverter, the measured output voltage and current waveforms of the implemented single phase prototype of the symmetric 9-level proposed inverter are shown in Fig. 9. As it can be seen, the results confirm the

ability of the proposed inverter in generating the desired output current waveform. As seen in these figures, the simulation and experimental results are in good agreement. The negligible difference between the magnitudes of the simulation and experimental results is due to voltage drops on switches in the prototype.

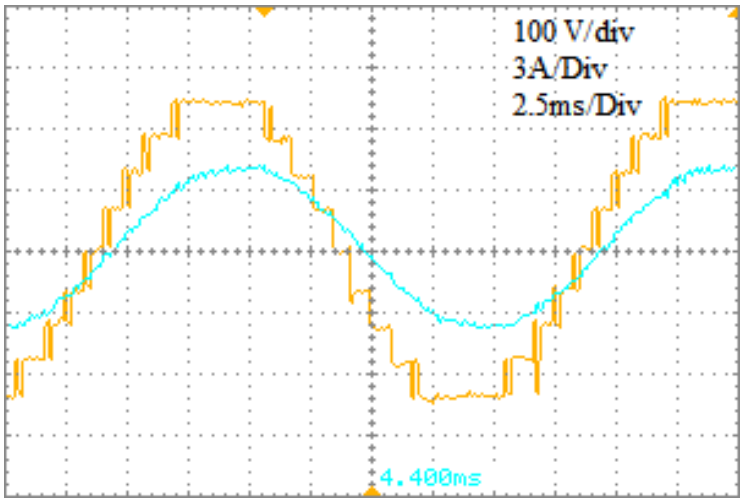


Fig. 9. Experimental results of implemented 9-level inverter, output current (1 Ohm resistance voltage) and voltage

5. Conclusion

In this paper, an advanced topology for symmetric multilevel current source inverters has been proposed. Reduced number of devices, including its DC current sources, switches and gate driver circuits is the advantage of this modular structure. As mentioned before, the provided comparison study between suggested inverter, CHB and recently proposed converters expresses the superiority of the proposed inverter over the mentioned topologies. Reduction in total costs, circuit size and simpler control scheme are the results of lower number of required devices. A prototype of the proposed symmetric topology has been implemented that validate the practicability of the proposed inverter. Finally, simulation and experimental results are compared with each other and the provided comparison shows that the obtained results are in good agreements.

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