A DEVELOPED SYMMETRIC/ASYMMETRIC MULTILEVEL CONVERTER TOPOLOGY WITH REDUCED NUMBER OF POWER ELECTRONIC COMPONENTS

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In this paper a developed symmetric and asymmetric cascaded multilevel inverter is proposed. In asymmetric mode, the values of DC voltage sources are defined in a way that the number of output levels gets more than the condition when the symmetrical DC sources are used. In this regards, to calculate the required magnitudes of DC links several solutions are proposed. It's obvious that the proposed topology can increase the number of output voltage levels using lower number of circuit devices. Comparison study validates the superiority of the proposed inverter. Provided simulation and experimental results confirm the practicality of proposed structure.

Keywords: Multilevel Voltage Source Inverter, Asymmetric Inverter, Symmetric Inverter, Reduction of Circuit Components

1. Introduction

A multilevel inverter is a power electronic equipment which has an important portion in power processing [1]. The most important advantages of the multilevel inverters are higher power quality, lower harmonic components, better electromagnetic interface and higher amplitude of fundamental component, higher efficiency, lower harmonic distortion, lower switching losses and lower *dv/dt*. The multilevel inverter components mainly are power semiconductor switches, diodes, gate driver circuits and DC power supplies. The multilevel voltage source inverters with synthesizing DC input voltages are used in order to generate stepwise output voltage waveform. In order to have more levels and so sinusoidal like waveform at the output, the number of DC links in input side should be more and more. As a matter of fact, voltage source inverters provide AC voltage waveform to the load by using several DC voltage power supplies connected to input side. Multilevel inverters are mostly installed in high power systems and used in mining applications as regenerative conveyors, and medical intentions like MRI gradient coil driver, hydro pump storage, FACTS and renewable energy

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conversion (wind and photovoltaic) [1, 2]. Multilevel converters are classified into 3 topologies: the neutral point clamped (NPC) or diode clamped [3], the flying capacitor (FC) or capacitor clamped [4] and the cascaded H-bridge (CHB) inverters [5]. The NPC inverter was based on a modification of the classic 2-level inverter topology adding two new power semiconductor switches per phase. Using this topology, each power device has to stand, at the most, half voltage in comparison with the two-level case with the same DC-link voltage. So, the voltage can be doubled. However, the NPC inverters need clamping diodes and are prone to voltage imbalances in their DC capacitors [6] which have kept the industrial acceptance of the NPC topology up to three levels only [7]. Moreover, another drawback is their unequal voltage sharing among series connected capacitors that results in DC-link capacitor unbalancing and requiring a great number of clamping diodes for higher levels. The FC inverter seems that the spread of the inverter to higher than three levels is possibly easier than the NPC alternative in commercial applications. This inverter requires a large number of storage capacitors for higher output voltage levels which increases the overall costs. In addition, another disadvantage of this structure is that the capacitors voltage balancing is difficult. As said before, CHB inverters are the other kind of multilevel converters. Because of the modularity and simplicity of the control, they are widely used in many applications. Cascaded H-bridge converters are made of power conversion cells, which are supplied by an isolated DC source on the DC side and have four switches. These cells are series-connected on the AC side in order to feed the load. So, if the number of H-bridge converters increases, more voltage levels will be obtained at the output. There are two groups of cascade multilevel converters, the symmetric and the asymmetric multilevel converters. In the symmetric cascade, multilevel converters, the values of DC voltage sources are equal but in the asymmetric one the values of these sources are different from each other. The high modularity is the advantage of the symmetric CHB multilevel inverter. In this topology, more number of switches are used. It is clear that, by increasing the number of switches, the total cost is increased and control gets complex. By using this inverter in asymmetric mode, the topology loses modularity, but more number of output voltage levels will be obtained. Various modulation methods can be applied to multilevel inverters. From the switching frequency aspect, switching strategies of multilevel inverters are categorized into high switching frequencies such as sinusoidal pulse-width modulation strategy [8] and low switching frequencies, often equal to fundamental switching frequency of the components, which create stepwise output voltage waveform [9]. The second category comprises three major switching strategies so-called “optimized harmonic stepped waveform” [10], “selective harmonic mitigation PWM” [11] and optimal minimization of the total harmonic distortion (THD) [12, 13]. The most important disadvantage of

multilevel inverters is the great number of circuit devices needed including its power semiconductor switches, gate drivers and DC power supplies. This may cause the overall system to be more expensive and complex. So, in practical implementation, reducing the requirements is very important. In this regards, several multilevel structures are reported in literatures. In [14], two different algorithms are proposed to define the magnitudes of DC voltage sources in CHB. Using asymmetrical DC sources can increase the number of output voltage levels. A novel MVSI, has been reported in [15]. This inverter uses bidirectional switches. Each bidirectional switch consists of two IGBTs and two diodes. If these IGBTs are connected as common emitter, then for each bidirectional switch, only one gate driver circuit is needed. The main novelty of this converter is the reduced number of switches compared to CHB. This improvement causes a reduction on gate drive circuits. But, this topology encountered higher Peak Inverse Value (*PIV*) compared to CHB. The topology presented in [16], uses unidirectional switches. For unidirectional switches the number of gate drivers is equal to the number of switches. The number of switches and gate driver circuits are less than in conventional CHB, but the total *PIV* is more. The inverter of [17] reduces the requirements for circuit devices. It is known that reducing the number of switches of the conventional inverters imposes an undesired increase in total *PIV* value. With proper connection of power switches to DC voltage sources, this increase can be limited. Comparatively, the *PIV* of [17] is increased to that of [16]. But, it must be mentioned that, since the number of IGBTs, switches and gate driver circuits are reduced significantly, an increase in total *PIV* is acceptable and can be neglected while this increase cannot detract from its values of obtained benefits from reductions. A novel MVSI has been suggested in [18] that reduces the power components compared to CHB resulting higher *PIV*. But its PIV is less than those one of [15, 17]. The topology presented in [19] is the reconfiguration of [15]. This inverter is well known because of its lower number of semiconductor switches. The *PIV* of this inverter is reduced, compared to that of [15] while this number is more than CHB. Recently, novel MVSIs have been suggested. The required power devices for these inverters are less compared to CHB and these inverters have kept the *PIV* equal to CHB. Designing a suitable configuration for the multilevel voltage source inverter is the main goal of this paper. The recommended topology is originated from the conventional CHB's model. In this topology the numbers of circuit devices are low so, the total costs and the installation area are remarkably reduced and it is easily controlled. Based on these studies, the proposed inverter requires less power switches, IGBTs, power diodes, driver circuits and DC voltage sources.

2. Proposed Configuration

The proposed basic unit is illustrated in Fig. 1. This formation is made of three DC-voltage sources and four semiconductor unidirectional switches. These switches $(S_{1i} \text{ and } \overline{S}_{1i})$ and $(S_{2i} \text{ and } \overline{S}_{2i})$ must be controlled in a complementary manner. On the other hand, in order to prevent the short circuit of DC voltage sources S_{1i} and S_{2i} switches cannot be turned on simultaneously with $\overline{S}_{1i}$ and $\overline{S}_{2i}$, respectively. In Table 1, the turn on and off states of the power switches are shown. In this Table, 1 shows that the relevant switch is turn-on and 0 points out the off state. According to Table 1 the proposed basic unit is able to generate four different levels at the output: 0, V_i, $2V_i$ and $3V_i$.

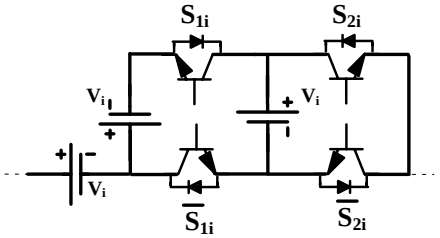


Fig. 1. Circuit diagram of the basic cell of proposed MVSI

Table 1

Various switching states of suggested basic cell

STATE NO.	S_{1i}	S_{2i}	STATE VOLTAGE
1	0	1	0
2	1	0	$3V_i$
3	1	1	$2V_i$
4	0	0	V_i

The overall view of the proposed converter is shown in Fig. 2. This inverter is mainly made of three parts:

- Two single DC sources, pointed by V_{dc} and V_s
- Series connection of several basic units
- Appropriate connection between switches

The magnitude of V_s can be either zero or any values of V_{dc} or $2V_{dc}$; so, choosing the proper value for V_s depends on the number of required DC voltage sources, and the number of DC sources depends to the number of output voltage levels. According to Table 1, it is obvious that the basic unit is only able to generate positive levels at the output. To generate both negative and positive voltages at the output of the proposed inverter $H_U, \overline{H}_U, M, \overline{M}, H_L \text{ and } \overline{H}_L$ switches are properly connected in border sides. In other words, these switches are used to convert the polarity of the output voltage to opposite polarity. The proposed unit is symmetric, so the magnitude of required DC voltage links must be equal.

Different DC voltage sources can be produced by connecting rectifiers to isolated transformers which are fed from AC voltage [20-22]. Also, these DC links can be prepared by renewable sources like fuel cell, photovoltaic or storage systems like batteries, *etc*.

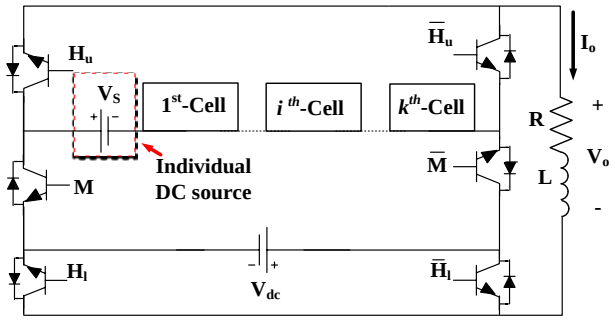


Fig. 2. Proposed MVSI

The greatest amount of output voltage ($V_{o,\max}$) of the suggested topology can be calculated:

$$V_{o,max} = \sum_{i=1}^{n} V_i \tag{1}$$

Here, the number of DC sources is indicated by n. The number of voltage levels is shown by (m) and given by the following equation:

$$m = 2\frac{V_{o,\max}}{V_{dc}} + 1 \tag{2}$$

A. SYMMETRIC METHOD

In this method, all the DC voltage sources have the same value. So, this structure is called symmetric multilevel inverter. For generating an *m*-levels output voltage, *n*-DC sources are needed.

$$n = \begin{cases} \frac{m-1}{2}; & if\ m = 6L+3 \\ \frac{m-1}{2}; & if\ m = 6L+5 \\ \frac{m-1}{2} - 1; & if\ m = 6L+7 \end{cases} \tag{3}$$

By increasing the number of cells it is possible to reach a definite value in the numbers of output voltage levels. It is clear that each cell consists of three DC voltage sources, so with n DC links, it is possible to have k basic cells. The relation between k and n are defined as below:

$$k = \begin{cases} \frac{n-1}{3}; & if\ m = 6L+3 \\ \frac{n-2}{3}; & \text{otherwise} \end{cases} \tag{4}$$

As said before, the value of V_s is set according to the number of the output voltage levels.

$$V_S = \begin{cases} 0 & if\ m = 6L+3 \\ V_{dc} & if\ m = 6L+5 \\ 2V_{dc} & if\ m = 6L+7 \end{cases} \quad (5)$$

For a better understanding, for generating an m-levels output voltage, the number of required DC sources (n) must be calculated using (3) and the value of V_s must be chosen according to the given formula in (5). For example to generate 9-levels in the output voltage, the number of DC links is four and V_s is set to be zero. Also, for $m = 11 and\ 13$, the number of DC voltage sources is calculated to be five. And then V_s is obtained to be $V_s = V_{dc}\ and\ 2V_{dc}$, respectively. In the suggested inverter, the number of switches (N_{switch}) is obtained from (6):

$$N_{Switch} = \begin{cases} \frac{4n+14}{3}; & if\ m = 6L+3 \\ \frac{4n+10}{3}; & if\ m = 6L+5 \\ \frac{4n+10}{3}; & if\ m = 6L+7 \end{cases} \quad (6)$$

Moreover, the relationship between the number of output levels (m) and the number of *IGBTs* (N_{switch}) is as follows:

$$N_{Switch} = \begin{cases} \frac{2m+12}{2}; & if\ m = 6L+3 \\ \frac{2m+8}{2}; & if\ m = 6L+5 \\ \frac{2m+6}{2}; & if\ m = 6L+7 \end{cases} \quad (7)$$

In the suggested inverter, the required switching pulses for each switch are produced by the related driver circuit. So:

$$N_{Driver} = N_{switch} \quad (8)$$

One important problem in multilevel inverters is the voltage rating of switches. The PIV of all switches is calculated by the following equation:

$$PIV = \sum_{j=1}^{N_{Switch}} PIV_{Switch_j} \quad (9)$$

So, for calculating the total *PIV* the below formulation is used:

$$PIV^{p.u.} = \begin{cases} 6n-2; & if\ m = 6L+3 \\ 6n-4; & if\ m = 6L+5 \\ 6n; & if\ m = 6L+7 \end{cases} \quad (10)$$

In symmetric mode, the relationships between *PIV* and m is formulated as follows:

$$PIV^{p.u.} = \begin{cases} 3m-5; & if\ m = 6L+3 \\ 3m-7; & if\ m = 6L+5 \\ 3m-9; & if\ m = 6L+7 \end{cases} \quad (11)$$

B. ASYMMETRIC METHODS

In multilevel inverters, the number and the maximum amplitude of generated output levels are based on the number and the value of used DC voltage sources. The proposed topology can be used as symmetric and asymmetric inverters. The symmetric method is explained in the previous section. In asymmetric mode, to calculate the required magnitudes of DC voltage sources six different solutions with different value of used DC voltage sources are defined and their parameters are calculated and shown in Table. 2. If the DC sources magnitudes are chosen correctly, a considerable increase in the number of output levels can be obtained without doing any manipulation on inverters hardware. According to these facts, the proposed inverter based on these solutions is considered as asymmetric inverter. In addition, based on the equations of the number of output voltage levels and its maximum amplitude, it is clear that these values in the asymmetric inverter are more than symmetric one with the same number of used DC voltage sources and power switches. It is important to mention that, in all of the proposed solutions, the magnitudes of DC voltage sources are different from one unit to another while they are equal in each unit. These DC links are selected according to a geometric progression. In some solutions defined for asymmetric mode, the proposed inverter can increase the number of output voltage levels adding two power switches to V_s. Fig. 3 defines the arrangement of these switches surrounding V_s. This reform is essential in 5th and 6th solutions. Otherwise, there is no need of this reform. Increases in maximum output voltage levels and amplitude are the most considerable merits of the proposed solutions when the non-equal DC voltage sources are applied. In order to investigate the advantages and the disadvantages of the proposed solutions of the asymmetric inverter, a full comparison is provided from several points of view such as the number of IGBTs and DC voltage sources. It is pointed out that the proposed solutions are indicated by $P_1 - P_6$, respectively. Fig. 4 compares the number of IGBTs. As it is obvious, the required numbers of IGBTs in the 6th proposed solution are lower than the other mentioned solutions. As mentioned before in unidirectional switches, the number of IGBTs is the same as the number of switches, power diodes and driver circuits. Therefore, in the 6th proposed solution, the number of switches, power diodes and driver circuits is less than in the other mentioned solutions. Fig. 6 compares the number of required DC voltage sources. As shown in Fig. 5, the 6th proposed solution needs a lower number of DC voltage source in generating particular levels.

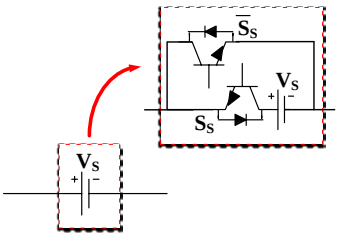


Fig. 3. Required reform to increase the number of output voltage steps

It is clear from the comparisons that the sixth proposed solution has better performance than all mentioned solutions.

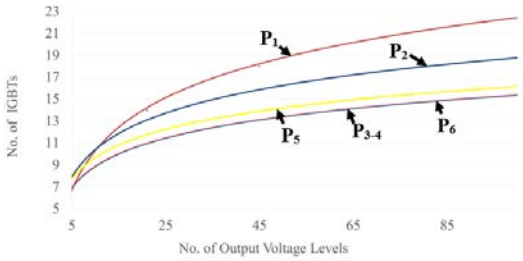


Fig. 4. Number of IGBTs versus number of levels for proposed solutions

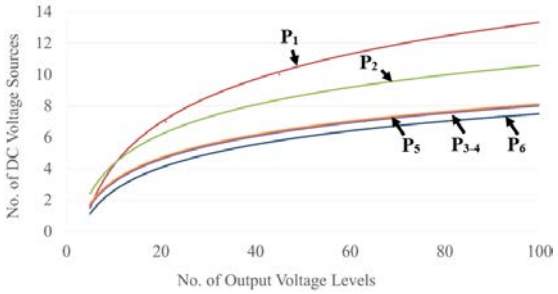


Fig. 5. The number of DC voltage sources versus number of levels for proposed solutions

3. Comparison of Proposed Inverter with other Multilevel Inverters

It's obvious from the afore mentioned discussions that implementing an asymmetric inverter in comparison to the proposed symmetric inverter is more commodious and more efficient from the technical point of view. As discussed, in multilevel voltage source structures the number of the required circuit devices including DC voltage sources, power semi-conductor switches and related gate driver circuits of switches versus the output voltage levels is significant, because the overall costs, circuit size, reliability and control complexity are directly dependent on it. Assuming the thirty-one-level in the output voltage for a test case, it's found that in symmetric mode, the number of DC voltage sources is fifteen, the number of switches and so gate driver circuits both are twenty-two. But considering asymmetric configuration with its 6^{th} proposed solution, these numbers are five and twelve, respectively. This comparison can be expanded to

the whole range of output voltage levels and the results will always keep similar. In order to compare the suggested configuration with CHB and the recently proposed inverters, it's fair assuming that the maximum output voltage is equal for all mentioned inverters.

Table 2. The proposed algorithms for asymmetrical converter and their related parameters

Proposed algorithms	V_s	*Magnitude of DC voltage sources*	k	N_{Switch}	m	PIV^{pu}
1st proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{4n+14}{3}$	$3\times2^{\frac{n-2}{3}}-3$	$9\times2^{\frac{n+2}{3}}-14$
2nd proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=3^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{4n+14}{3}$	$3^{\frac{n+2}{3}}$	$3^{\frac{n+5}{3}}-5$
3rd proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{4n+14}{3}$	$4^{\frac{n+2}{3}}-1$	$3\times4^{\frac{n-2}{3}}-8$
4th proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=2V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{4n+14}{3}$	$4\times2^{\frac{n-2}{3}}-1$	$3\times2^{\frac{n-2}{3}}-8$
5th proposed algorithm	1	$V_{1,1}=V_{2,1}=V_{3,1}=3V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-2}{3}$	$\frac{4n+16}{3}$	$6\times4^{\frac{n-2}{3}}-1$	$18\times4^{\frac{n-2}{3}}-8$
6th proposed algorithm	2	$V_{1,1}=V_{2,1}=V_{3,1}=4V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-2}{3}$	$\frac{4n+16}{3}$	$2\times4^{\frac{n-1}{3}}-1$	$6\times2^{\frac{n-1}{3}}-8$

So, the comparison of MVSIs versus output voltage levels is discussed. In this regards the proposed asymmetric configuration with its 6th proposed solution is applied in comparisons. In this part, in order to have an impartial comparison, the number of IGBTs, the amount of gate driver circuits, the number of DC voltage sources and the total *PIV* versus output voltage levels is compared considering the proposed converter and the recently reported inverters in literature. It is pointed out that all other inverters participated in the comparison study and their different solutions are shown by $R_1 - R_{10}$ in these comparisons. The conventional symmetric cascaded H-bridge inverter is pointed by R_1. Moreover, two other solutions for this inverter have been presented in [14]. These solutions are indicated by R_2 and R_3, respectively. In these solutions the values of DC links are as $V_1 = V_{dc}, V_{2-\infty} = 2V_{dc}$ and $V_1 = V_{dc}, V_{2-\infty} = 3V_{dc}$, respectively. The other reported symmetric multilevel inverters are indicated by R_4 - R_{10}. The solution R_4 which is

compared is presented in [16]. R_5, R_6 and R_7 are the other inverters used for comparison and analyzed in [19, 21-22] respectively. To emphasize the practicability of the represented structure, the R_8, R_9 and R_{10} solution pointed out in [15], [18], [17] are also compared with this structure. The number of IGBTs versus the number of voltage levels for various MVSI configurations are shown in Fig. 6. In the proposed inverter unidirectional switches are used, so the number of gate drivers is equal to the number of switches. By analyzing the R_8 inverter, it is obvious that this inverter has several bidirectional switches in its topology and each bidirectional switch consists of two IGBTs. For each bidirectional switch, only one gate driver circuit is needed, because these IGBTs are connected as common emitter. So, the number of gate driver circuits versus output voltage levels is represented in Fig. 7. According to Fig. 6 and 7, in the whole range of possible voltage levels, the requirements for IGBTs and gate driver circuits used in the proposed topology are less than in the other mentioned solutions. As a result, in the proposed inverter the required installation area and costs are reduced and the control schema gets simpler. Another parameter which has important impact on the overall cost of the inverter is the number of required DC voltage sources. So, by using a lower number of it, the overall cost will be reduced.

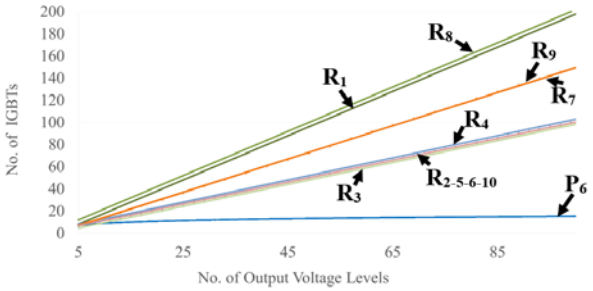


Fig. 6. Number of IGBTs versus number of levels for proposed topology and other mentioned solutions

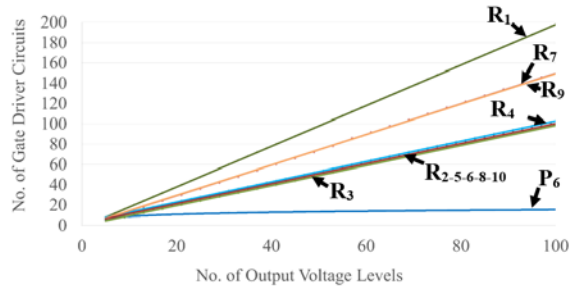


Fig. 7. Number of gate driver circuits versus number of levels for proposed topology and other mentioned solutions

The number of DC voltage sources versus output levels in all mentioned inverters is represented in Fig. 8. From the comparison studies, it is obvious that in order to

have the same level in the output, the number of required DC voltage sources in the proposed asymmetric inverter is always lower. Another essential parameter which plays a significant role on the overall inverter cost is voltage rating of power switches. It is known that reducing the number of switches of the conventional inverters imposes an undesired increase in total *PIV* value. With the proper connection of power switches to DC voltage sources, this increase can be limited. The PIV values of the mentioned inverters are represented in Fig. 9. Because of the big reduction in circuit equipment in the proposed inverter, a bit increase in its total *PIV* compared to some conventional inverters is acceptable and can be neglected, while a reduction in number of switches, gate driver circuits and DC power supplies is achieved.

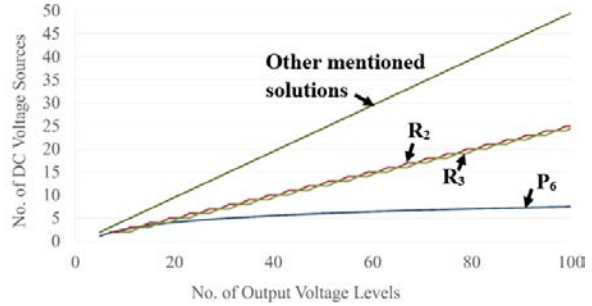


Fig. 8. The number of DC voltage sources versus number of levels for proposed topology and other mentioned solutions

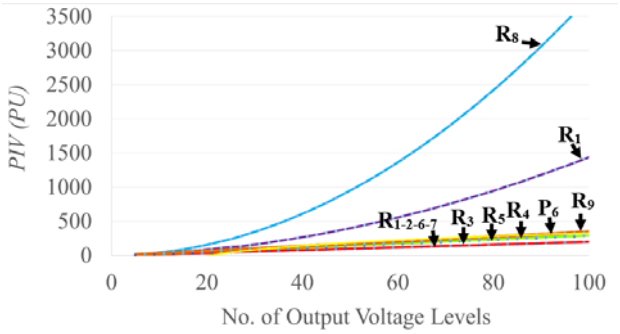


Fig. 9. Total *PIV* value versus number of levels for proposed topology and other mentioned solutions

4. Simulation and Experimental Results

At first the simulation studies should be presented, to show the feasibility of the proposed multilevel inverter. In this regards, MATLAB/Simulink software is used for simulation purposes. In the next step, the experimental results are studied to certify the practicability and the good performance of the suggested MVSI. The adjustable DC sources which are available in the laboratory, have been used to provide the DC voltage links. The main parameters of implemented circuit are represented in Table 3.

Table 3

Parameters of implemented inverter

Type of switch	IRF260
Type of MOSFET driver	Hcpl316j
Pulse Generator	DsPIC30F4011
DC Voltage Sources Magnitudes	5V
Load Parameters	35 Ohm & 36 mH
Fundamental Frequency	50Hz

The circuit diagram of the 23-Level multilevel inverter is shown in Fig. 10. Fig. 11 represents the voltage and current waveforms of the 23-level asymmetric inverter. For the given simulation results in Fig. 11, it is concluded that generating all the voltage levels in the suggested inverter validates the practicability of the proposed inverter. The measured output voltage and current waveforms of the implemented single phase prototype of the 23-level proposed inverter shown in Fig. 12 (a) and (b) validate the feasibility of the suggested multilevel inverter.

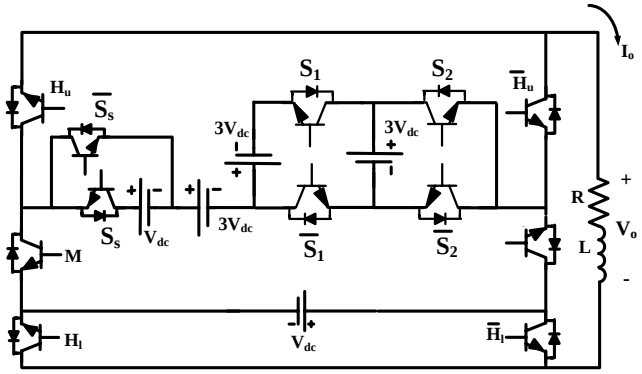


Fig. 10. Circuit diagram of 23-Level multilevel inverter

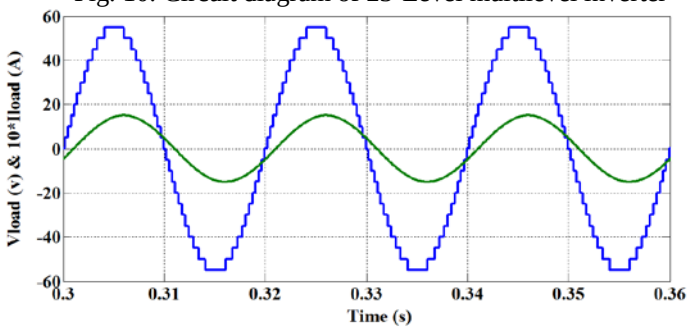
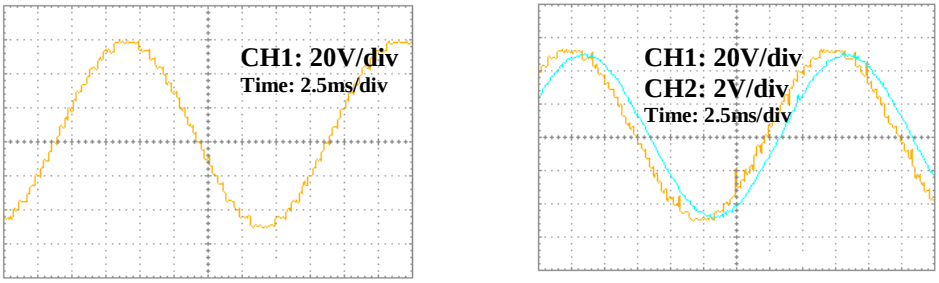


Fig. 11. Voltage and current waveforms of voltage waveform of proposed asymmetric 23-level inverter



(a) (b)

Fig. 12. Experimental results of implemented 23-level proposed inverter
a) Output voltage (no load) and b) Output voltage and current (10/3 Ohm resistant voltage)

By considering Fig. 11 and 12, it is obvious that there is a good compromise between the experimental and simulation results and the negligible difference between the magnitudes of these waveforms is due to the voltage drops on switches in the experimental prototype.

5. Conclusion

The main purpose of this paper is to propose a developed structure for symmetric and asymmetric multilevel voltage inverters. Also, several different solutions have been presented for the proposed asymmetric inverter structure in order to calculate the required magnitudes of DC voltage sources. This novel modular configuration reduced number of circuit devices. As a result the total costs and the installation area are reduced, the reliability is increased and the control system gets simpler. In order to demonstrate the practicability of the proposed inverter over the mentioned structures, a comparison study among the proposed inverter, CHB and recently proposed inverters is performed. Also, a prototype of the proposed topology has been accomplished to emphasize the practicability of the represented structure. At the end of the paper, the provided simulation and experimental results are compared with each other to demonstrate the good compromise of the achieved results.

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