CURRENT-MODE REFERENCES BASED ON MOS SUBTHRESHOLD OPERATION

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Utilizarea tranzistoarelor MOS în conducţie sub prag, sau inversie slabă, este folosită frecvent în aplicaţiile de consum redus ale electronicii moderne. Referinţele de tensiune şi curent sunt circuite care pot beneficia substanţial de operarea tranzistoarelor MOS în inversie slabă. Utilizarea referinţelor bazate pe arhitecturi cu mod de lucru în curent a devenit foarte răspândită în ultimul deceniu, datorită abilităţii acestora de a-şi menţine performanţele funcţionale la valori scăzute ale tensiunii de alimentare. Această lucrare prezintă arhitecturi originale de implementare a unor referinţe de tensiune MOS cu modul de lucru în curent şi compensare termică de ordin superior, a căror funcţionare se bazează pe operarea tranzistoarelor MOS în inversie slabă. O metodă originală de implementare a unui generator de current IPTAT^2 utilizat în cadrul mecanismului de compensare termică de ordin superior este prezentată, de asemenea, în lucrare.

Subthreshold MOS operation, or weak inversion, is most often required by the low-power applications in modern electronics. Voltage and current references are among the circuits that can greatly benefit from operating the MOS devices in weak inversion. At the same time, the current-mode architectures for voltage and current references became very popular during the last decade, due to their ability to perform at lower supply voltages. This paper presents original architectures for the implementation of current-mode voltage references with higher-order thermal compensation, based on subthreshold MOS operation. An original method for implementing an IPTAT^2 current generator employed by the higher-order compensation mechanism is also described.

Keywords: MOS subthreshold operation, weak inversion, current-mode voltage reference, thermal compensation

1. Introduction

One of the major trends of nowadays electronics is low-power operation, a combination of low supply voltage and low quiescent current. Under such constraints, the classical principle of bandgap voltage-mode references of about 1.25V cannot be applied anymore. In a classical bandgap reference, first order thermal compensation is achieved by summing up a voltage **p**roportional **t**o

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absolute **t**emperature (PTAT) and a voltage that is **c**omplementary **t**o **a**bsolute **t**emperature (CTAT), generated in such a way to achieve mutual cancellation of the variation with temperature. Typically, the CTAT voltage is the voltage drop across a silicon diode, while the PTAT voltage is generated by a PTAT current across a resistor. The PTAT current is the result of the voltage difference between two silicon diodes of different junction areas, across a second resistor. Such a thermally compensated bandgap voltage reference has an output range of 1.2..1.3V, depending on technology. The head-room for these references usually requires an additional V_{DSsat} above the output voltage, limiting the minimum supply voltage to values around 1.5V. Significant research was dedicated to designing voltage references that can operate at supply voltages below 1V. Thus, low voltage techniques were developed based on current-mode architectures, which achieve specific functions based on the summation of currents, rather than voltages. A current-mode reference architecture was first described in [1], based on processing the currents related to a pair of p-n diodes with different junction areas, as shown in Fig.1.

The resulting thermally compensated reference current I_{REF} is sourced on a resistor R_6, thus generating a reference voltage V_{REF} of the desired value.

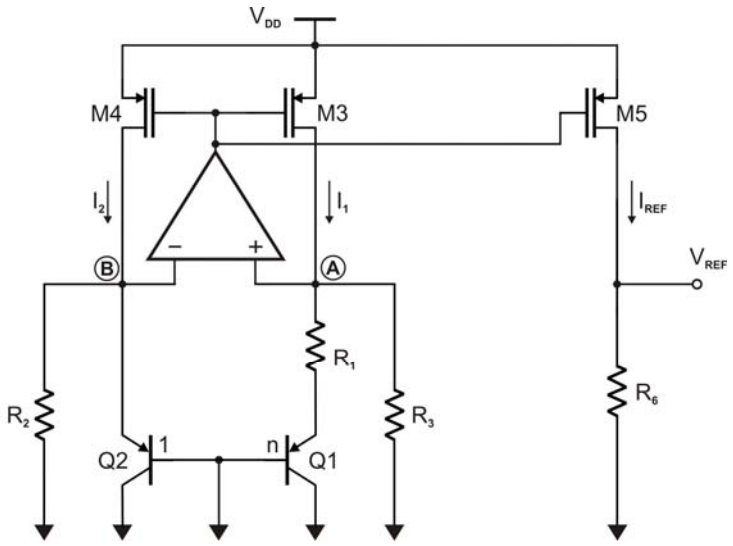

Fig.1. Current-mode bandgap reference

Advances on the implementation of current-mode references are further described in various papers, such as [2] - [6], revealing a constant interest for these design techniques, within the general trend to reduce the power supply voltage. At the same time, deep submicron technologies offer lower MOS

threshold voltages, suitable for low voltage applications. As a result, further reduction of the supply voltage can be achieved, if the classical p-n junctions employed in the reference architecture are replaced with low-threshold MOS transistors operated in weak inversion. Moreover, this approach allows a CMOS only implementation, eliminating the need for bipolar devices. Such fully CMOS solutions based on transistors operated in subthreshold are further described in this paper.

2. Subthreshold operation of the MOS transistor

Subthreshold operation, or weak inversion, is defined as the operating region of the MOS transistor at very low drain currents, with V_{GS} values around the threshold voltage V_{Th},

$$V_{GS\,subth} \le V_{Th} + 2nV_T \tag{1}$$

where the subthreshold slope factor n is technology dependent and has typical values between 1 and 2 [7],

$$n = \frac{\partial V_G}{\partial \Phi_s} = 1 + \frac{C_D}{C_{ox}} = 1 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_{Si} q N_B}{2\Phi_s}} \tag{2}$$

with the surface potential at the source, Φ_s, taking values between Φ_F+V_S and $2\Phi_F+V_S$, where

$$\Phi_F = V_T \ln\left(\frac{N_B}{n_i}\right) \tag{3}$$

is the Fermi potential, and

$$V_T = \frac{kT}{q} \tag{4}$$

is the thermal voltage.

In subthreshold, the conduction is mainly due to diffusion phenomena in the channel therefore, the drain current varies exponentially with the substrate voltage V_{BS}, and with the drain voltage V_{DS}. Similarly, a small variation of the voltage drop V_{GS} causes large variations in the drain current, also described by an exponential function. Thus, the drain current of the MOS transistor in subthreshold can be expressed as

$$I_D = \frac{W}{L} I_{D0} \exp\left[-V_{BS}\left(\frac{1}{nV_T} - \frac{1}{V_T}\right)\right]\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right]\exp\left(\frac{V_{GS} - V_{Th}}{nV_T}\right) \tag{5}$$

The saturation occurs for $V_{DS} > 3V_T$ and, as a result, the saturation drain current has the simplified expression

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS} - V_{Th}}{nV_T}\right) \tag{6}$$

where I_{D0} is a process dependent parameter

$$I_{D0} = \mu(T) V_T^2 \sqrt{\frac{\varepsilon_{Si} qN}{2\Phi_s}} \tag{7}$$

Considering the drain currents $I_D(T_0)$ and $I_D(T)$ at the reference temperature T_0 and at the nominal temperature T, the following formula can be derived

$$\ln \frac{I_D(T)}{I_D(T_0)} = \ln\left(\frac{T}{T_0}\right)^{2-\beta_\mu} + \frac{q}{nk}\left[\frac{V_{GS}(T) - V_{Th}(T)}{T} - \frac{V_{GS}(T_0) - V_{Th}(T_0)}{T_0}\right] \tag{8}$$

where β_μ is the temperature coefficient of the electric charge carriers mobility

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-\beta_\mu} \tag{9}$$

β_μ is a parameter that has values between 1.2 and 2.0 [8].

For a PTAT$^\alpha$ drain current $I_D(T) = cT^\alpha$,

$$\frac{I_D(T)}{I_D(T_0)} = \left(\frac{T}{T_0}\right)^\alpha \tag{10}$$

we get

$$\ln\left(\frac{T}{T_0}\right)^{\alpha+\beta_\mu-2} = \frac{q}{nkT}\left[\left(V_{GS}(T) - V_{Th}(T)\right) - \left(V_{GS}(T_0) - V_{Th}(T_0)\right)\frac{T}{T_0}\right] \tag{11}$$

yielding

$$V_{GS}(T) = V_{Th}(T) + \left[V_{GS}(T_0) - V_{Th}(T_0)\right]\frac{T}{T_0} + \frac{nkT}{q}\left(\alpha + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{12}$$

The temperature variation of the MOS threshold voltage can be expressed in a simplified and generally accepted form, by

$$V_{Th}(T) = V_{Th}(T_0) - AT,\ A > 0 \tag{13}$$

The formula (12) for V_{GS} reveals linear and non-linear temperature dependent terms that need to be compensated in order to achieve a minimal variation with temperature, as required in voltage and current references.

3. Current-mode reference based on subthreshold MOS operation

MOS transistors operated in subthreshold represent an attractive solution for implementing thermally compensated voltage references, without employing bipolar devices. Current-mode techniques can be applied for mutual compensation of the linear PTAT and CTAT terms. Moreover, the exponential variation of the drain current with the gate-to-source voltage can be used to compensate non-linear variation with temperature of the reference currents and voltages. Thus, higher order temperature effects can be significantly reduced.

Following these considerations, we propose a current-mode reference architecture (Fig.2) with the NMOS devices M1 and M2 operated in subthreshold, which achieves the compensation of linear temperature dependent terms, known as first order thermal compensation.

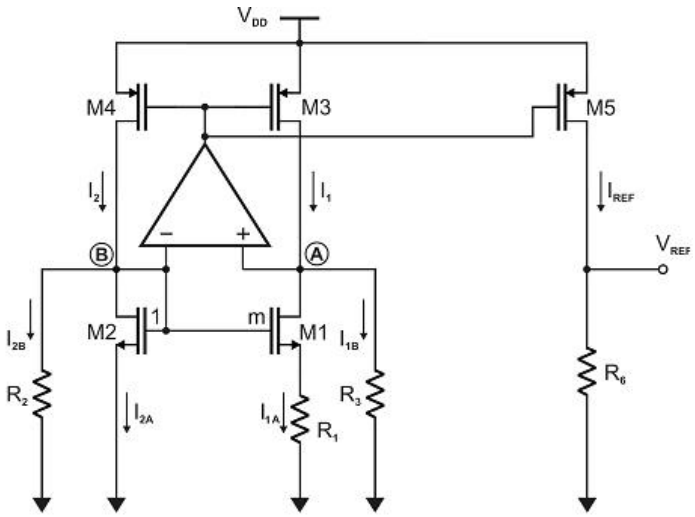

Fig. 2. Subthreshold current-mode reference with first order temperature compensation

Since the currents I_1 and I_2 are equal, and due to the OPAMP's ability to maintain equal voltage levels on the nodes A and B, for R_2=R_3 we obtain

$$I_{1A} = I_{2A} \tag{14}$$

yielding

$$V_{GS2} - V_{GS1} = nV_T \ln m \tag{15}$$

Then, the current through R1

$$I_{1A} = \frac{1}{R_1} nV_T \ln m \tag{16}$$

is a PTAT current.

The resistor R_2 subtracts a CTAT current from node A,

$$I_{2B} \cong \frac{V_{Th}}{R_2} \tag{17}$$

and resistor R_3 subtracts a similar CTAT current from node B since $R_3 = R_2$

$$I_{1B} = I_{2B} \tag{18}$$

Transistors M1 and M2 are in saturation, since M2 is diode connected and, similar to (12), the formulas for the corresponding gate-to-source voltages as a function of temperature are

$$V_{GS1}(T) = V_{Th}(T) + \left[V_{GS1}(T_0) - V_{Th}(T_0)\right]\frac{T}{T_0} + \frac{nkT}{q}\left(\alpha + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{19}$$

$$V_{GS2}(T) = V_{Th}(T) + \left[V_{GS2}(T_0) - V_{Th}(T_0)\right]\frac{T}{T_0} + \frac{nkT}{q}\left(\alpha + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{20}$$

where $\alpha = 1$ since $I_{1A} = I_{2A}$ are PTAT currents.

From equations (15) and (18) we get,

$$I_{2B}(T) = \frac{V_{Th}(T)}{R_2} + \frac{1}{R_2}\frac{T}{T_0}\left[V_{GS2}(T_0) - V_{Th}(T_0)\right] + \frac{nV_T}{R_2}\left(\alpha + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{21}$$

Using equations (14), (16) and (21), we can write the current I_2 as

$$I_{2A} + I_{2B} = I_{2CTAT} + I_{2PTAT} + I_{2NL} \tag{22}$$

where

$$I_{2CTAT} = \frac{V_{Th}(T)}{R_2} \tag{23}$$

$$I_{2PTAT} = T\left(\frac{1}{R_2}\frac{V_{GS2}(T_0) - V_{Th}(T_0)}{T_0} + \frac{1}{R_1}\frac{nk}{q}\ln m\right) \tag{24}$$

$$I_{2NL} = \frac{1}{R_2}\frac{nkT}{q}\left(\alpha + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{25}$$

As I_{REF} and I_2 are equal, it results that first order thermal compensation can be achieved by mutual cancellation of the linear I_{2CTAT} and I_{2PTAT} variation with temperature at the reference temperature T_0,

$$\left.\frac{dI_{2CTAT}}{dT}\right|_{T=T_0} + \left.\frac{dI_{2PTAT}}{dT}\right|_{T=T_0} = 0 \tag{26}$$

The current I_{2NL} has a smaller contribution than I_{2CTAT} and I_{2PTAT} to the global variation with temperature of the current I_2 due to its logarithmic function therefore, the thermal compensation of I_{2NL} is regarded as a second order correction, while the main thermal compensation mechanism stands in the mutual cancellation of the I_{2CTAT} and I_{2PTAT} thermal variation.

Equations (23), (24) and (26) yield

$$-\frac{A}{R_2} + \frac{1}{R_2 T_0}\left[V_{GS2}(T_0) - V_{Th}(T_0)\right] + \frac{1}{R_1}\frac{nk}{q}\ln m = 0 \tag{27}$$

hence

$$R_2 = R_1\frac{q}{nk\ln m}\left(A - \frac{V_{GS2}(T_0) - V_{Th}(T_0)}{T_0}\right) \tag{28}$$

where

$$V_{GS2}(T_0) - V_{Th}(T_0) \le 2n\frac{kT_0}{q} \tag{29}$$

according to (1).

Second order thermal compensation pursues total invariance with temperature, including both the linear and the non-linear temperature dependent terms. From (22),

$$\left.\frac{dI_{2CTAT}}{dT}\right|_{T=T_0} + \left.\frac{dI_{2PTAT}}{dT}\right|_{T=T_0} + \left.\frac{dI_{2NL}}{dT}\right|_{T=T_0} = 0 \tag{30}$$

In order to cancel I_{2NL}, and similarly I_{1NL}, convenient nonlinear currents I_{2C} and I_{1C} must be added in the nodes B and A, as proposed in Fig.3.

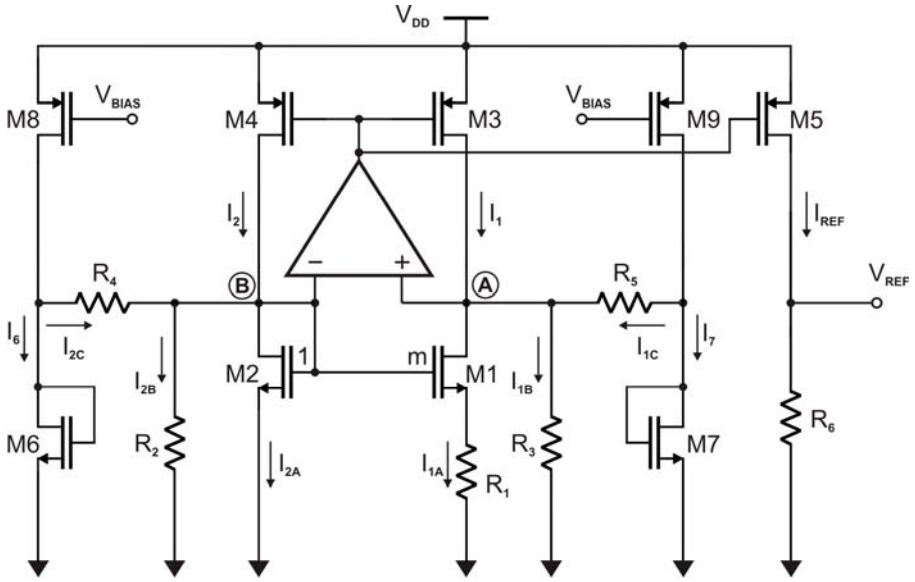

Fig. 3. Subthreshold current-mode reference with second order thermal compensation

We will demonstrate that, for achieving the desired second order thermal compensation, temperature dependent currents

$$I_6 = I_7 = CT^{\alpha_6} \tag{31}$$

must bias transistor M6, respectively transistor M7 . Indeed, using for V_{GS6} a similar expression as for V_{GS2}, we get

$$V_{GS6}(T) = V_{Th}(T) + \left[V_{GS6}(T_0) - V_{Th}(T_0)\right]\frac{T}{T_0} + nV_T\left(\alpha_6 + \beta_\mu - 2\right)\ln\frac{T}{T_0} \tag{32}$$

and the current injected in node B through R_4 is

$$I_{2C} = \frac{V_{GS6}(T) - V_{GS2}(T)}{R_4} = \frac{1}{R_4}\left[V_{GS6}(T_0) - V_{GS2}(T_0)\right]\frac{T}{T_0} + \frac{nV_T}{R_4}\left(\alpha_6 - \alpha_2\right)\ln\frac{T}{T_0} \tag{33}$$

Assuming that I_6 is chosen such that $V_{GS6}(T_0) = V_{GS2}(T_0)$, then

$$I_{2C} = \frac{nV_T}{R_4}\left(\alpha_6 - \alpha_2\right)\ln\frac{T}{T_0} \tag{34}$$

and the condition for I_{2C} to cancel I_{2NL} requires

$$\frac{nV_T}{R_4}\left(\alpha_6 - \alpha_2\right)\ln\frac{T}{T_0} = \frac{nV_T}{R_2}\ln\frac{T}{T_0} \tag{35}$$

which yields

$$R_4 = (\alpha_6 - \alpha_2) R_2 \tag{36}$$

When M6 is biased with a PTAT^2 current

$$I_6 = CT^2 \tag{37}$$

the coefficients α_6 and α_2 follow the relationship

$$\alpha_6 = \alpha_2 + 1 \tag{38}$$

and the second order thermal compensation is achieved for

$$R_2 = R_4 \tag{39}$$

In a similar manner, $$R_5 = R_3 \tag{40}$$

Then,

$$I_2 = I_{2A} + I_{2B} - I_{2C} \tag{41}$$

$$I_1 = I_{1A} + I_{1B} - I_{1C} \tag{42}$$

and $$I_{REF} = I_1 = I_2 \tag{43}$$

achieves thermal compensation

$$\left.\frac{dI_{REF}}{dT}\right|_{T=T_0} = 0 \tag{44}$$

while $$V_{REF} = I_{REF} R_6 \tag{45}$$

benefits of the same thermal behavior as I_{REF}.

Although variation with temperature of the resistors was not included in the previous considerations, such variations cancel out as long as the resistors are of the same type.

The PTAT^2 current can be achieved using a typical architecture as the one described in [9] and represented in Fig. 4.

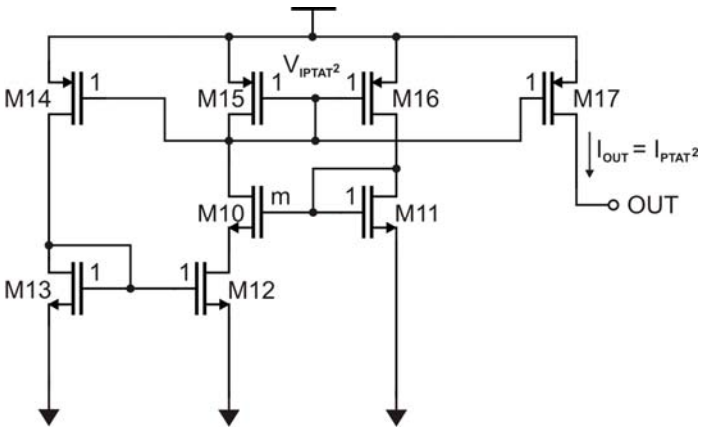

Fig. 4. PTAT^2 current generator

Transistors M10 and M11 are operated in subthreshold, while M12 and M13 function in strong inversion. The KLV equation on loop M10, M11, M12 yields

$$I_{OUT} = \frac{V_{GS11} - V_{GS10}}{R_{ds12}} \tag{46}$$

where

$$V_{GS11} - V_{GS10} = nV_T \ln m \tag{47}$$

and

$$R_{ds12} = \left[\mu_n C_{ox} \frac{W_{12}}{L_{12}} \left(V_{GS12} - V_{Th} \right) \right]^{-1} \tag{48}$$

as transistor M12 is operated in the linear region.

Since transistor M13 is in saturation and $V_{GS13} = V_{GS12}$

$$V_{GS12} - V_{Th} = V_{GS13} - V_{Th} = \sqrt{\frac{2I_{OUT}}{\mu_n C_{ox} \frac{W_{13}}{L_{13}}}} \tag{49}$$

yielding

$$R_{ds12} = \left[\frac{W_{12}}{L_{12}} \sqrt{\frac{2I_{OUT}\mu_n C_{ox}}{\frac{W_{13}}{L_{13}}}} \right]^{-1} \tag{50}$$

Finally, from (46), (47) and (50)

$$I_{OUT} = 2n^2 V_T^2 \mu_n C_{ox} \left(\frac{W_{12}}{L_{12}} \right)^2 \frac{L_{13}}{W_{13}} \ln^2 m \tag{51}$$

hence I_{OUT} is a PTAT^2 current.

A more accurate implementation can be achieved when the PTAT^2 current is obtained from an I_{PTAT} current generated in a similar manner as in the current mode reference previously presented. Such a PTAT^2 current source is proposed in Fig.5 where transistors M24 and M25 provide the I_{PTAT} current and transistors M18, M19, M20, M21 are all operated in subthreshold with

$$V_{GS} = nV_T \ln\left(\frac{I_D}{I_{D0}} \frac{L}{W} \right) - V_{Th} \tag{52}$$

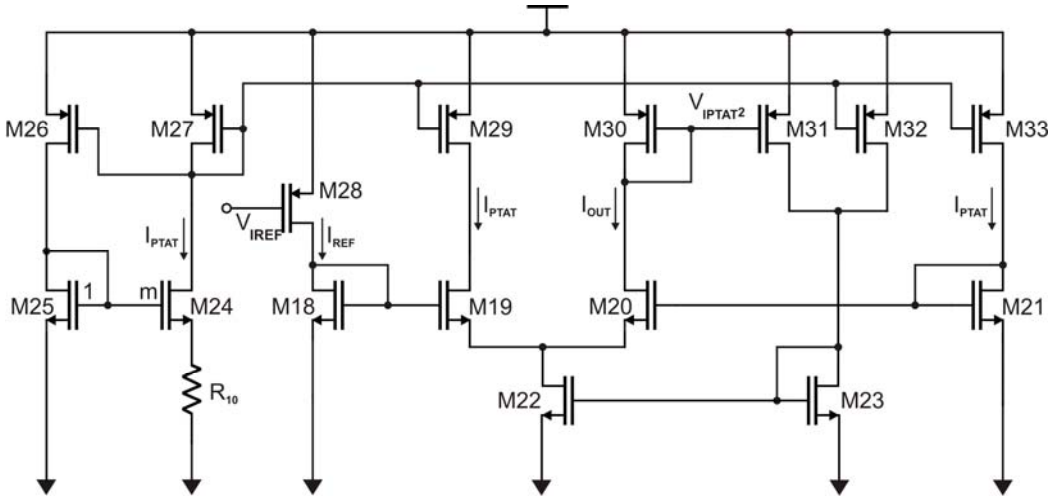

Fig. 5. PTAT^2 current generator with enhanced performance

As a result of the V_{GS} summation across transistors M18, M19, M20 and M21

$$-V_{GS18} + V_{GS19} - V_{GS20} + V_{GS21} = 0 \tag{53}$$

we get a PTAT^2 current

$$I_{OUT} = \frac{I^2_{PTAT}}{I_{REF}} \tag{54}$$

which does not depend on the temperature variation of the electric carriers mobility.

In a practical implementation, employing such a PTAT^2 current generator for the architecture in Fig.3 requires the biasing of transistors M8 and M9 to the $V_{IPTAT}{}^2$ potential generated on the gate of M30 represented in Fig.5. At the same time, the current I_{REF} provided by transistor M28 in Fig.5 is obtained by connecting the gate input V_{IREF} to the common gate of transistors M3, M4 and M5 from the reference in Fig.3, thus mirroring the current I_{REF} of the voltage reference. Moreover, the I_{PTAT} current in Fig.5 can be a mirror copy of the current I_{2A} from the voltage reference. Higher precision can be achieved by using voltage buffers between M6 and R4, respectively between M7 and R5, as shown in Fig.6.

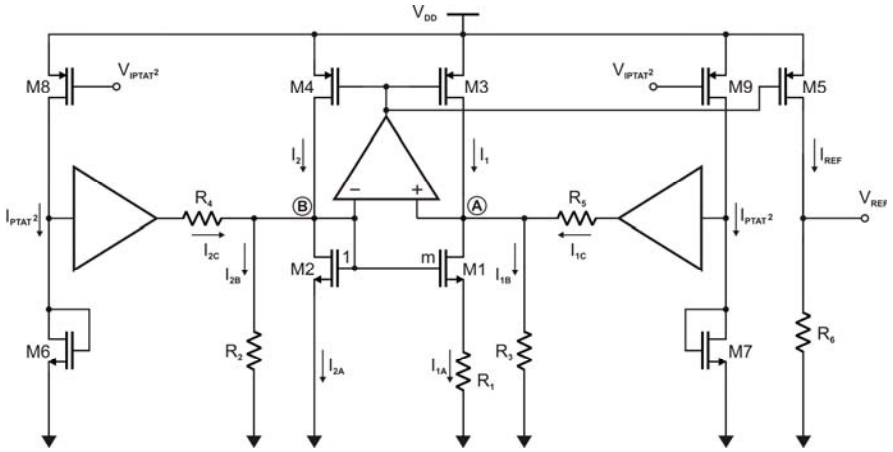

Fig. 6. Current-mode reference with second order thermal compensation biased with a $PTAT^2$ current generator

5. Experimental results

The current-mode references were implemented in a 0.35um technology in order to compare the temperature stability perşformance of the first and second order compensation mechanisms. The simulation results are presented in Fig. 7, for a nominal VREF of around 0.8V and a supply voltage VDD=1.2V. VREF1 represents the output voltage of the reference version with first-order compensation, shown in Fig. 2, while VREF2 and VREF3 are the output voltages of the reference architecture described in Fig. 3, with I_{PTAT}^2 generators shown in Fig. 4 and Fig.5 respectively. The simulations were performed for a temperature range between $-50^{\circ}C$ and $+120^{\circ}C$.

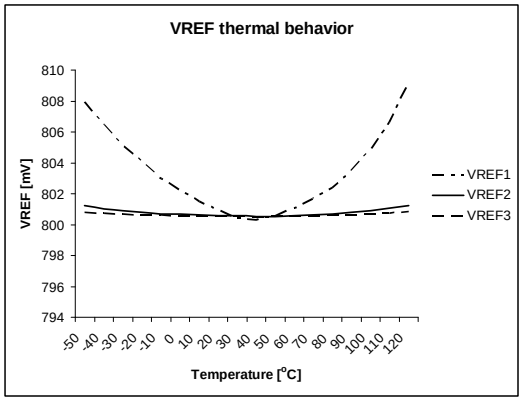

Fig. 7. Temperature variation of the reference voltage for the current-mode architectures

A detail of the reference voltage variation with temperature for the second order thermal compensation architectures is represented in Fig. 8.

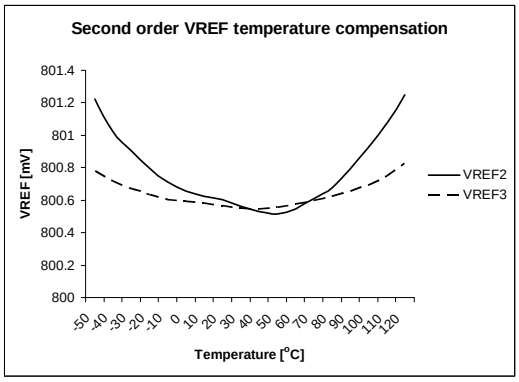

Fig. 8. Reference voltage variation with temperature for second order thermal compensation

The thermal coefficient of the references can be computed using the formula

$$TC_{VREF} = \frac{\max\left[VREF(T)\right] - \min\left[VREF(T)\right]}{\min\left[VREF(T)\right]} \frac{10^6}{T_{MAX} - T_{MIN}} [ppm/^\circ C] \qquad (55)$$

The first order thermal compensation yields a performance of $TC_{VREF1} = 66 ppm/^\circ C$, while the second order compensation methods yield $TC_{VREF2} = 5.35 ppm/^\circ C$ and $TC_{VREF3} = 2.1 ppm/^\circ C$. Increased temperature stability comes with the price of increased ground current, due to additional current branches. Thus, while the first order compensation circuit that generates V_{REF1} consumes around $2\mu A$, the second order compensated circuit which provides V_{REF2} consumes approximately $4\mu A$ and the one generating V_{REF3}, about $5\mu A$. The supply current overhead comes from additional circuit branches implemented by M6 and M7, the current consumed by the I_{PTAT}^2 generators and the supply current required by the voltage buffers between the transistor M6 and resistor R4, and between the transistor M7 and resistor R5, respectively.

6. Conclusions

This paper describes original solutions for low-power and low-voltage reference design, based on current-mode techniques and MOS transistors operated in subthreshold. The study introduces an original architecture that implements a current-mode reference featuring first order thermal compensation, based on

mutual cancellation of the variation with temperature of PTAT and CTAT currents generated with MOS transistors. A higher-order thermal compensation mechanism is further added to the initial architecture, using a $PTAT^2$ current generator that produces a bias current for correcting the non-linear temperature dependent terms. An original solution for implementing the $PTAT^2$ current generator employed by the higher-order compensation mechanism is also described. Such a thermal compensation scheme provides an improved thermal stability by eliminating the temperature effect of the carriers' mobility. Designed in a 0.35um standard CMOS technology, the simulation results confirm the theoretical considerations presented in the paper.

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