HYSTERESIS MODULATED SLIDING MODE CONTROL FOR QUADRATIC BOOST SWITCHED CAPACITOR CONVERTER

Sivaraj DESINGU[1], Arounassalame MOUTTOU[2]

A high voltage gain quadratic boost switched capacitor DC–DC converter is proposed for standard output voltage of 48 V. This paper presents a reduced order modelling of quadratic boost switched capacitor converter in order to reduce the complication of the modeling of the system and Hysteresis Modulated Sliding Mode Control (HMSMC) scheme is applied for controlling the proposed nonlinear converter. It has only two feedback state variables on the sliding surface and the inner loop sliding surface depends on the input inductor current. The proposed system with controller is tested under load disturbances and supply disturbances. The deliberate outcomes of this proposed system with controller is compared with the conventional PI controller. The simulation of the proposed converter with controller is carried out using MATLAB/SIMULINK and the results are reported.

Keywords: Reduced Order Model, Voltage Regulation, PI Controller, HMSMC Controller

1. Introduction

The advancement of modern technology needs a broad range of step-up voltage. In particular, applications as photovoltaic power system, energy unit frameworks, micro grid, renewable grid inverter and energy harvesting requires the use of wide range gain DC-DC converters. A conventional DC–DC converters couldn't satisfy the need for wide-range of DC voltage. A non- isolated High gain DC-DC converter have become very admired due to its wide applicability, particularly considering that DC- AC converters must be ordinarily provided with high DC voltages [1-3]. A numerous high gain DC-DC converter topologies are developed latter. Positive output cascade boost converter provides the increased output voltage by geometric progression using super lift technique and it provides better output than arithmetic progression of voltage lift technique used in three-series Luo-converter. It consists main series, additional series, double series, triple series and multiple series. Each series carries individual inductor and some

[1] Research Scholar, Pondicherry Engineering College, Puducherry - 605 014, India, e-mail: sivaraj2d@gmail.com.

[2] Associate Prof., Dept. of Electrical and Electronics Engineering, Pondicherry Engineering College, Puducherry - 605 014, India, e-mail: arun@pec.edu

capacitor and diode in the circuit [4]. The cascade converter produces high voltage gain with an expansion in number of switches, diodes, inductors and capacitors. Use of more inductor and capacitor in the circuit, results in ESR and electromagnetic interference issues which leads to low efficiency. Some of isolated converter provides high voltage gain with the help of transformer, coupled inductor and stacking on the secondary side with integrated boost converter discussed in [5, 6]. In these topologies, the controller execution is inconvenient due to the switching frequency issue and leakage inductance. To overcome these issues snubber topologies are introduced in the active voltage clamp fly back converter to reduce the transformer leakage inductance and reducing the dissipating power by recycling process [7]. Some of high gain converters like forward, push pull, fly back converter etc., are giving high voltage gain by changing the turn's proportion of the transformer. The power switch of these converters experiences high voltage spike which destructs the switches, and the leakage inductance of the transformer makes high dissipation of power. So, these type of converter not suitable for low to medium power applications. The non-isolated converter offers a simple structure, less weight and less assembling cost. In this, the topology of quadratic boost circuit comprises of single dynamic switch and the voltage increases in a quadratic type of the duty ratio. Traditional quadratic boost converter can achieve high step-up voltage gain when it operates at high duty cycle. In addition, the switch undergoes extreme duty cycle results a serious reverse recovery problem. To address this issues, many circuit developed along with quadratic boost converter like coupled inductor, voltage multiplier etc., [8, 9]. The coupled inductor circuit provides high gain voltage with a reduced number of switches, but it may increment the turn's ratio. Because of coupled inductance input current ripple and conduction loss are also increased. The multilevel converter is a non-isolated converter, and it provides few advantages such continuous input current, wide duty ratio, and can be operated in high switching frequency [10]. This paper proposes Quadratic Boost Switched Capacitor Converter (QBSCC) to secure high output voltage. This converter adds the properties of quadratic boost and multilevel converter like high voltage transformation ratio. Here, high voltage gain is achieved without utilizing a transformer, without enormous duty ratio and without coupled inductor. This proposed converter (QBSCC) take care of the imbalance issue which happens in the diode clamped multilevel converter and furthermore give the choice to increase the number of output voltage level by including more diode-capacitor pair [11]. To accomplish better steady state and dynamic response on varying line and load, it is necessary to operate in a closed loop and the control strategies for these types of converters are very less. This paper presents a full order and reduced order modelling for the QBSCC and implementation of the hysteresis

modulation based Sliding Mode Controller. The performance of the sliding mode controller is compared with that of PI controller and the results are reported.

The rest of the paper organized as follows. Section 2, the analysis and modeling of QBSCC is discussed and in section 3 discussed about the Hysteresis Modulated sliding mode controller. Performance analysis of the QBSCC with HMSMC controller is discussed in section 4 and finally conclusions are presented in section 5.

2. Quadratic Boost Switched Capacitor Converter

2.1 QBSCC Operation

The quadratic boost switched capacitance convertor contain 2N-1 diode and 2N-1 capacitance, Here N indicates range of voltage level, it provides self-balancing voltage and simplex current flow while not perturbing main quadratic boost convertor circuit and the range of voltage levels is taken as two (N=2). The combined circuit of quadratic boost convertor with switched capacitance circuit shown in Fig. 1. During ON state of switch sw, the diode D_1 is reverse biased and diode D_2 in forward biased. The inductors L_1 and L_2 stores energy from the input source (E) and capacitor (C_1) respectively. Capacitor C_1 discharge slowly through the inductor L_2 by switch sw. During OFF state of switch sw, the diode D_1, D_3, D_5 are forward biased and the other two diodes D_2, D_4 are in reverse biased condition. Then the Inductors L_1 and L_2 start discharging the stored energy in the continuous conduction mode. On the same time voltage across capacitor C_1 start charging through D_1. The capacitor C_2 charged through inductor L_2 by turning on of the diode D_5, similarly C_2 and C_3 are also charged by turning on the diode D_3 for the short duration of time [12].

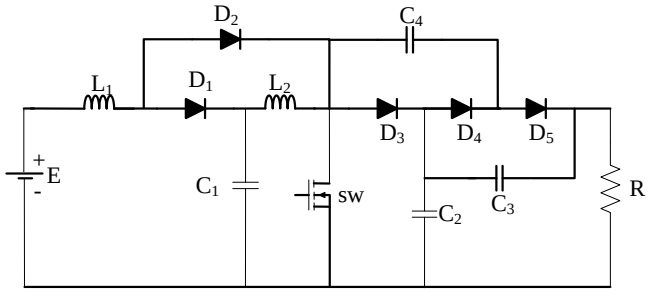
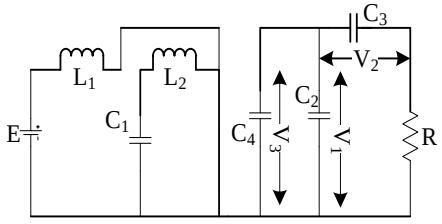


Fig. 1. Quadratic Boost Switched Capacitor Converter

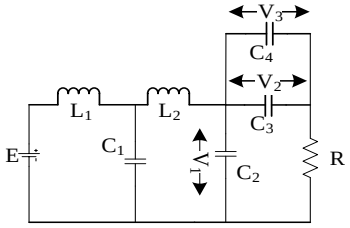
2.2 Full order Modelling of QBSCC

During ON state the capacitor C_2 and C_4 are looked as parallel, while the voltage across C_4 is V_3 and voltage across C_2 is V_1. In this condition the capacitor C_4 obtain energy from the capacitor C_2 shown in Fig. 2(a). During OFF state of the switch the capacitor C_3 and C_4 are looked as parallel similar to previous case, here from capacitor C_4 energy is transferred to the capacitor C_3 presented in Fig.

2(b). The dynamic nonlinear state equations of the switch ON state and OFF state is given in the equations (1) and (2).



(a) ON state of the switch: $0 < t < dt$



(b) OFF state of the switch: $\mathrm{dt} < t < T$

Fig. 2. Full order switching state of QBSCC

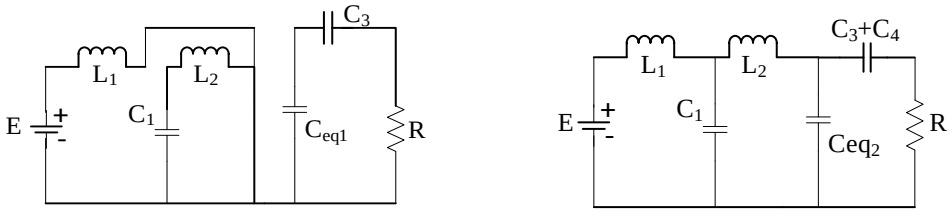
$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{E}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{C1}}{L_2} \\ \dfrac{dV_{C1}}{dt} = -\dfrac{i_{L2}}{C_1} \\ \dfrac{dV_1}{dt} = -\dfrac{1}{(C_2+C_4)R}V_1 - \dfrac{1}{(C_2+C_4)R}V_2 \\ \dfrac{dV_2}{dt} = -\dfrac{1}{C_3R}V_1 - \dfrac{1}{C_3R}V_2 \\ \dfrac{dV_3}{dt} = -\dfrac{1}{(C_2+C_4)R}V_1 - \dfrac{1}{(C_2+C_4)R}V_2 \end{cases} \tag{1}$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{E}{L_1} - \dfrac{V_{C1}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{C1}}{L_2} - \dfrac{V_{C2}}{L_2} \\ \dfrac{dV_{C1}}{dt} = \dfrac{i_{L1}}{C_1} - \dfrac{i_{L2}}{C_1} \\ \dfrac{dV_1}{dt} = \dfrac{i_{L2}}{C_2} - \dfrac{V_1}{C_2R} - \dfrac{V_2}{C_3R} \\ \dfrac{dV_2}{dt} = \dfrac{1}{(C_2+C_3)R}V_1 - \dfrac{1}{(C_2+C_3)R}V_2 \\ \dfrac{dV_3}{dt} = \dfrac{1}{(C_3+C_4)R}V_1 - \dfrac{1}{(C_3+C_4)R}V_2 \end{cases} \tag{2}$$

In order to design a controller for the proposed QBSCC, it is necessary to obtain the transfer function of the entire system. However, due to the presence of additional capacitors and diodes, the full order model may become complex and the order of transfer function increase. The reduced order model provides the flexibility to minimize the order of transfer function without considering the fast transient parameters.

2.3 Reduced order Modelling of QBSCC

The dynamic behavior of reduced order model will be approximately equal to the full order model. The output voltage of the QBSCC is in the balancing form and hence the voltages across the capacitors C_2 and C_3 are equal. When the switch is in ON condition the capacitor C_2 is in parallel to the capacitor C_4. This parallel combination of two capacitors taken as a single equivalent capacitor and denoted as C_{eq1}, which is 2C, and it shown in Fig. 3(a). Similarly, when the switch is in OFF state C_3 and C_4 are in parallel, then the equivalent capacitor is taken as C_{eq2} shown in Fig. 3(b). Here it is assumed that $C \approx C_2 \approx C_3 \approx C_4$ and $V_1 \approx V_2 \approx V_3 \approx \ldots \approx V_N \approx V/N$. In the reduced order model of QBSCC the number of parameters reduced to four [13].



(a) ON state of the switch $0 < t < dt$ (b) OFF state of the switch $dt < t < T$

Fig. 3. Reduced order QBSCC switching state

The state equations are obtained using Kirchhoff voltage law and Kirchhoff current law. The dynamic nonlinear state equations of the switch ON state and OFF state is given in equations (3) and (4). The average state space model of the reduced order quadratic boost switched capacitor converter is given in equations (5), (6) and (7).

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{E}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{C1}}{L_2} \\ \dfrac{dV_{C1}}{dt} = -\dfrac{i_{L2}}{C_1} \\ \dfrac{dV}{dt} = -\dfrac{NV}{RC_{eq1}} \end{cases} \qquad 0 < t < dt \tag{3}$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{E}{L_1} - \dfrac{V_{C1}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{C1}}{L_2} - \dfrac{V}{L_2} \\ \dfrac{dV_{C1}}{dt} = \dfrac{i_{L1}}{C_1} - \dfrac{i_{L2}}{C_1} \\ \dfrac{dV}{dt} = \dfrac{i_{L2}}{C_{eq2}} - \dfrac{NV}{RC_{eq2}} \end{cases} \qquad dt < t < T \tag{4}$$

$$\dot{x(t)} = Ax(t) + Bu(t) \tag{5}$$

$$y = Cx(t) + Du(t) \tag{6}$$

The behavior of the system can be understood by checking the location of poles and zeros. From the transfer function of the proposed system (output voltage to duty ratio) given in equation (8).

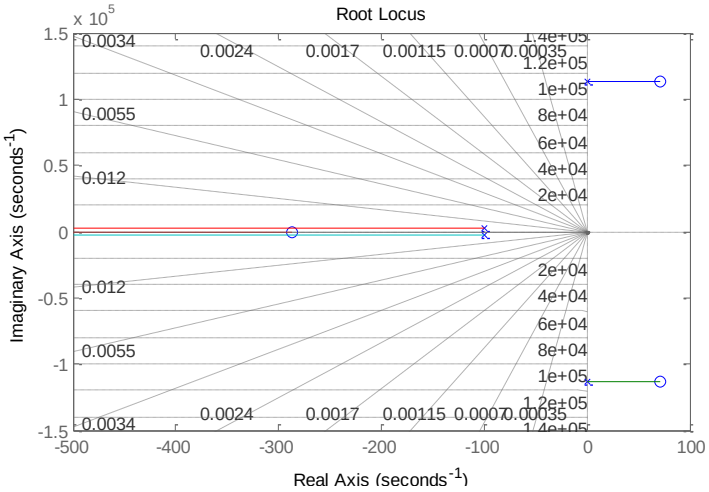


Fig. 4 Root locus of the transfer function of output voltage to duty cycle for QBSCC

It is found that all the poles are located in the left half of the s-plane (0 ± i112900, -100 ± i2540), and couple of zeros present in right half of the s-plane (70 ± i11289). Hence the proposed converter is completely stable and non-minimum phase system, refer in Fig. 4. The single loop controller is sufficient to regulate the output voltage of the proposed system, but the ripple in the output becomes high and switching frequency problem arise. To solve this issue two loop controller is needed. In literature [14, 15], current controller is mostly utilized in the high gain converter for non- minimum phase condition.

$$\begin{bmatrix} \dot{\widehat{i_{L1}}} \\ \dot{\widehat{i_{L2}}} \\ \dot{\widehat{V_{C1}}} \\ \dot{\hat{V}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{(1-D)}{L_1} & 0 \\ 0 & 0 & \dfrac{1}{L_2} & \dfrac{(1-D)}{L_2} \\ \dfrac{(1-D)}{C_1} & -\dfrac{1}{C_1} & \dfrac{1}{L_2} & 0 \\ 0 & \dfrac{(1-D)}{C} & 0 & -\dfrac{N}{2CR} - \dfrac{N(1-D)}{CR} \end{bmatrix} \begin{bmatrix} \widehat{i_{L1}} \\ \widehat{i_{L2}} \\ \widehat{V_{C1}} \\ \hat{V} \end{bmatrix} + \begin{bmatrix} \dfrac{E}{(1-D)L_1} & \dfrac{1}{L_1} \\ \dfrac{E}{(1-D)^2 L_2} & 0 \\ -\dfrac{\left(\frac{3}{2}-D\right)NE}{(1-D)^4 RC_1} & 0 \\ -\dfrac{\left(\frac{3}{2}-D\right)NE}{(1-D)^3 RC} + \dfrac{NE}{(1-D)^2 C_1} & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{e} \end{bmatrix} \tag{7}$$

$$\frac{V_O}{V_C} = \left(\frac{1}{V_P}\right)\left(\frac{V_0/d}{1 + \frac{N}{V_p}(i_{L1}/d)}\right) \tag{8}$$

$$\frac{\widehat{V_0}}{\hat{d}} = \frac{4.3 \times 10^6 s^3 + 6.3 \times 10^8 s^2 + 1.1 \times 10^{15} s + 1.5 \times 10^{17}}{s^4 + 200s^3 + 2.5 \times 10^8 s^2 + 4.9 \times 10^{10} s + 8.3 \times 10^{14}} \tag{9}$$

$$\frac{\widehat{i_{L1}}}{\hat{d}} = \frac{1.3 \times 10^5 s^3 + 5.1 \times 10^8 s^2 + 3.3 \times 10^{13} s - 7.1 \times 10^{17}}{s^4 + 200s^3 + 2.5 \times 10^8 s^2 + 4.905 \times 10^{10} s + 8.2 \times 10^{14}} \tag{10}$$

The transfer function of the proposed converter obtained from equation (8) has couple of zeros are in right half of s-plane and only one zero in left half of s-plane (70 ± i112890, -290). Due to this two loop controller (inner current loop and outer voltage loop) is not much effective, so nonlinear controller is better for this type of converter. Hence sliding mode is better option for effective regulation of the output voltage.

3. SLIDING MODE CONTROLLER FOR QBSCC

The fundamental deterrent for sliding mode control execution is a phenomenon called chattering in control. The traditional asymptotic state observer technique is used to reduce the chattering or adjustment with a time varying gain. The state space model of quadratic boost switched capacitor converter under hysteresis modulation sliding mode control works in continuous conduction mode [16-18]. The state trajectory parameter for the sliding mode control is given in equation (11).

$$S(x) = i_{L1} - i_E(t) \tag{11}$$

The state trajectory computation is formed by the error information of inductor current and the reference current parameter I_E (t) is given by the equation (12).

$$I_E(t) = -K_p\left(nV(t) - V_{ref}\right) - K_i \int_{-\infty}^{t} (nV(\tau) - V_{ref})d\tau \tag{12}$$

The operation of the switching function (u) depends on sliding motion parameter values and is given in equation (13).

$$u = \begin{cases} 1, & when\ S(x) < 0 \\ 0, & when\ S(x) > 0 \end{cases} \tag{13}$$

The output voltage error (e_1) and the inductance current error (e_2) are derived from the parameter reference voltage and derived reference current by externally and it is given in the equations (14) and (15).

$$e_1 = V_{ref} - V \tag{14}$$

$$e_2 = i_{L1ref} - i_{L1} \tag{15}$$

Evaluating the existence condition $S(x)\dot{S}(x) < 0$ using the control law leads to the local reachability condition and is given in equation (16).

$$0 < V_i - L_1 \frac{dI_E}{dt} < V_{C1} \tag{16}$$

Applying the invariance condition ($S(x) = 0$ and $\dot{S}(x) = 0$) , the control law can be obtained and it is given in equation (17).

$$u_{eq} = 1 - \frac{1}{V_{C1}}\left(V_i - L_1 \frac{dI_E}{dt}\right) \tag{17}$$

The phase trajectory moves along the straight line path when the $S(x) = 0$ which represents the sliding dynamics of the converter. In this case the converter operates in sliding mode operation with infinite switching frequency. Because of the switching time delay, time constant and imperfection of switches the infinite switching frequency not ready to accomplish. The irregularity in the feedback control will create a specific dynamic behaviour in the region of the sliding surface called as chattering. In the event that the chattering is left uncontrolled, at very high switching frequency the converter operates in self oscillating form in the chattering dynamics. This is bothersome as high switching frequency will bring about excessive switching loss and serious issue in in the electromagnetic interference noise. Hence troublesome in the choosing of the parameter. The hysteresis band is denoted by the symbol ζ, which is subjectively small one. To control the switching frequency of the system needs to fix the boundary condition of ζ. The switching frequency of the converter is controlled by choosing the sliding surface S=ζ (turn on) and S= -ζ (turn off). This type of methods in SM control is commonly utilized for reducing the chattering effect. With this change, the operation is adjusted to such an extent that if the parameter of the state variable S>ζ is the turn on and $S < -\zeta$ is the turn off condition of the converter switch. In between the region $-\zeta \leq S \leq \zeta$ no switching occurs. This eases the impact of chattering and it is possible to control the frequency of the operation by varying the magnitude of ζ. The hysteresis band (ζ) and switching frequency (f_{sw}) relation must be known to control the switching frequency. The hysteresis band values are decided by the knowledge of input voltage, voltage across capacitor, switching frequency and inductance value and is given in equation (18). The corresponding switching frequency is given in equation (19).

$$\zeta = \frac{V\left(1 - \frac{V}{E}\right)}{2f_{sw}L} \tag{18}$$

$$f_{sw} = \frac{1}{T_s} = \frac{1}{\delta t_1 + \delta t_2} = \frac{E\left(1 - \left({}^{E}/_{V}\right)^{1/2}\right)}{2L_1\zeta} \tag{19}$$

The inductor current works in sliding mode, the switching frequency of quadratic boost switched capacitor converter depends essentially on the input voltage. Hysteresis band is taken as fixed values for regulating the output voltage error as zero.

4. PERFORMANCE ANALYSIS

The parameters of the proposed circuit are designed for the requirement of converter output. The formulas are constructed by considering limits for the change in inductor current, capacitor voltage and switching frequency as $\delta i_{L1} =$

$20\%\mathrm{i}_{\mathrm{L1}}$, $\delta\mathrm{i}_{\mathrm{L2}} = 20\%\mathrm{i}_{\mathrm{L2}}, \delta\mathrm{V}_{\mathrm{C1}} = 2\%\mathrm{V}_{\mathrm{C1}}$, $\delta\mathrm{V}_{\mathrm{C2}} = 2\%\mathrm{V}_{\mathrm{C2}}$ and $f_{sw} = 50$ kHz. The rating of power semiconductor devices mainly based on the selection of L and C in the circuit. Limits of load current are chosen as 0.5 A as minimum and 2 A as maximum. The expressions for the inductor current are given in equations (20) and (21)

$$i_{L1} = \frac{i_0}{(1-D)^2} \tag{20}$$

$$i_{L2} = \frac{i_0}{(1-D)} \tag{21}$$

Inductor values L_1 and L_2 are designed from the average inductor current and allowable ripple current and the relevant equations are given in equations (22) and (23).

$$L_1 = \frac{ED}{\delta i_{L1} f_{sw}} \tag{22}$$

$$L_2 = \frac{ED}{\delta i_{L2}(1-D) f_{sw}} \tag{23}$$

Using the above expression, the value of inductor L_1 is found between 37.5 µH to 150 µH and the value of inductor L_2 is found between 150 µH to 600 µH. Inductors L_1 and L_2 are capable of carrying a current of 8.8 A and 4.4 A respectively. Capacitor values are designed from average capacitor voltage and allowable ripple voltage and the relevant equations are given in equations (24) and (25).

$$C_1 = \frac{I_0 D}{(1-D)\Delta V_{C1} f_{sw}} \tag{24}$$

$$C_2 = C_3 = C_4 = \frac{I_0 D}{\Delta V_{C2} f_{sw}} \tag{25}$$

Capacitor C_1 takes value between 8.33 µF and 33.3 µF and capacitor C_2 takes value between 2.08 µF and 8.3 µF. Based on the design formula the parameters are selected and are shown in Table 1.

Table 1

Parameters of QBSCC

Parameter	Value
Output voltage (V_0)	6 V
Duty Cycle (D)	0.5 to 0.9
Capacitor C_1	22 µF

Capacitor (C_2, C_3, C_4)	100 µF
Inductor L_1	60 µH
Inductor L_2	380 µH
Load Resistor (R)	100 Ω
Switching frequency (f_{sw})	50 kHz

Quadratic boost switched capacitor converter with hysteresis modulation based sliding mode controller is shown in Fig. 5.

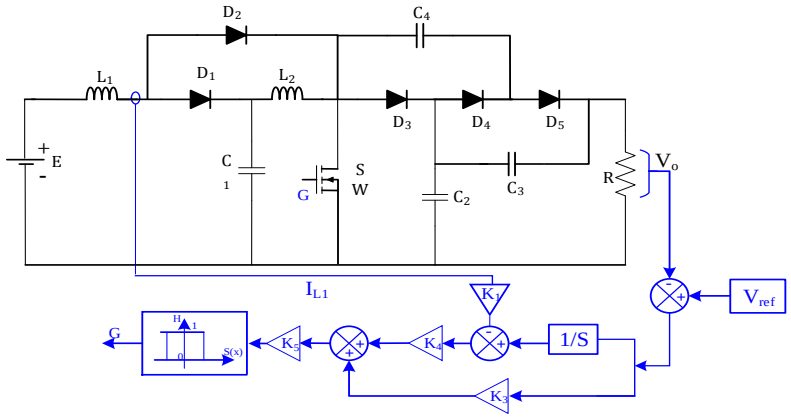


Fig. 5 Scheme of HMSMC for proposed QBSCC

Here two loop control is used. The outer loop is the voltage control and inner loop is the current control. The gain values for the sliding mode controller are chosen as K_1=0.15, K_2= 6.12, K_3=0.096, K_4=0.25 and K_5=50. The hysteresis band (ζ) value present in between ±1, in this case for better operation ζ taken as ±0.12. A PI controller also designed for the proposed QBSCC and the response is obtained. Fig. 6 shows the convergence of states under sliding mode equilibrium conditions. Fig. 7 shows the response of the HMSMC controller and PI controller for the QBSCC. It is found that when the load is changed the response for the HMSMC is better and peak overshoot is minimum. Fig. 8 presents the graph of the output ripple. From 0.0222 sec to 0.00245 sec the HMSMC controller output voltage varies from 47.96 V to 48.05 V (i.e., 0.09 V) and in the PI controller output voltage varies from 47.9 V to 48.12 V (i.e., 0.22 V) varied. Nearly 50% of ripple reduced in the HMSMC controlled by comparing with conventional PI controller.

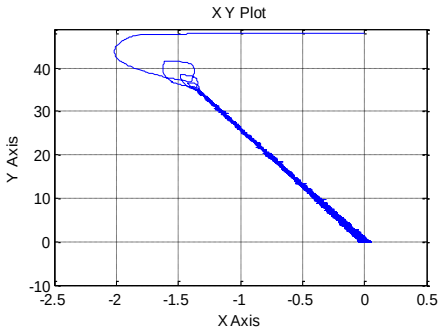


Fig.6. Phase trajectories stucture of voltage error and voltage error dynamics for the proposed system

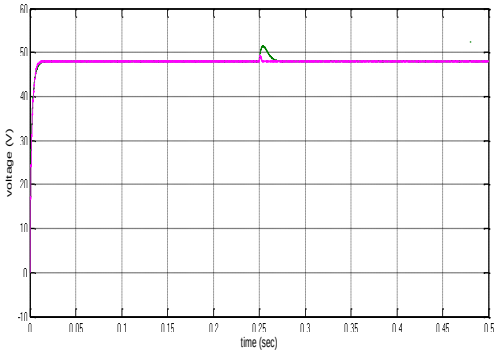


Fig.7. Output voltage response of the PI controller and HMSMC controller of QBSCC

The transient response during starting of the converter is given in Fig. 9. The rise time of the converter for both the controllers are almost same (approximately 0.08 sec) and there is no starting peak overshoot for both controllers. Further the system is tested under the line variation by varying the input voltage (E) from 6 V to 7.2 V (20%), the peak overshoot of the HMSMC controller is much reduced when compared with the conventional one. While compare the settling time HMSMC takes additionally 0.005 sec to settle and it is given in Fig. 10. Fig. 11 shows the comparison of inductor current profile for the HMSMC and PI controller. In the inductor current response, HMSMC controller produce 1 A variation in inductor 1 (i_{L1}) and 0.37 A variation in inductor 2 (i_{L2}), while PI controller for the system produces inductor 1 current variation (Δi_{L1}) of 0.4 A. i.e., 60% reduction in conventional type.

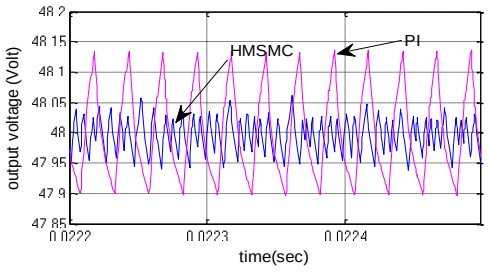


Fig. 8. Output voltage ripple comparison of PI controller and HMSMC controller of QBSCC

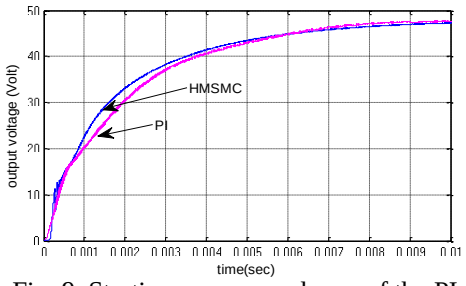


Fig. 9. Starting response scheme of the PI controller and HMSMC controller of QBSCC

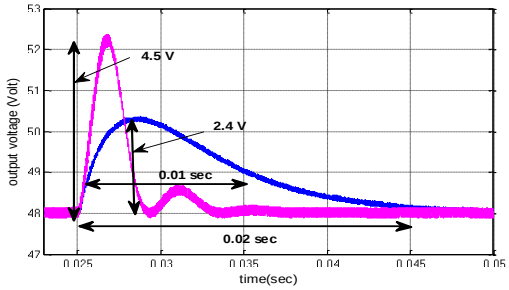
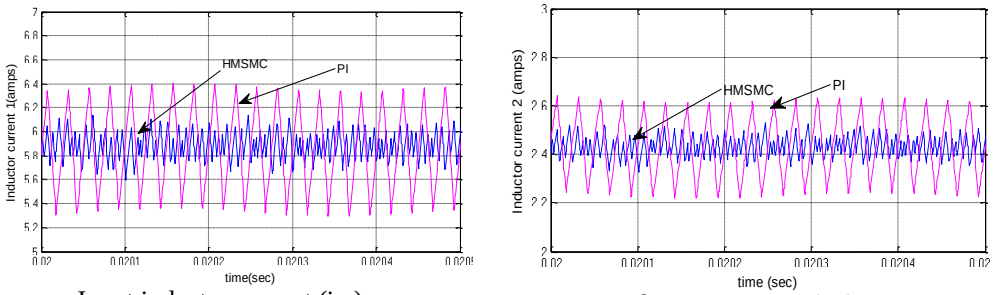


Fig. 10. Line variation transient response of the PI controller and HMSMC controller of QBSCC



Input inductor current (i_{L1}) Inductor current 2 (i_{L2})

Fig. 11. Comparison of inductor current

Similarly, inductor 2 (Δi_{L2}) current variation is also reduced as 0.2 A. i.e., 45% distortion is reduced. The steady state error of the both the controller is almost negligible and the efficiency is predicted [19-20] and is given in the Fig. 12.

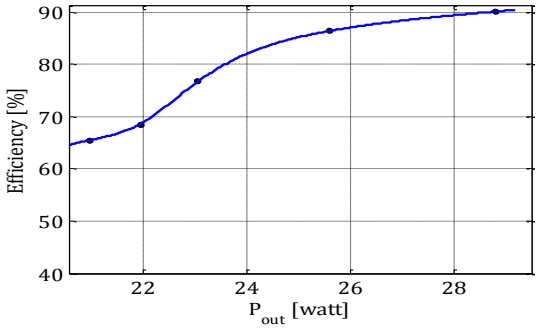


Fig. 12. Prediction on efficiency Vs output power

The efficiency for the nominal output power of 24 W is 82.5% and it is increased to 90.1% under the output power of 30 W. The overall efficiency of the system in improved by the reduction in current ripple, output voltage ripple and reduced switching loss by implementation of controller.

5. Conclusions

In this work, a hysteresis modulation based sliding mode controller is implemented and tested for the quadratic boost switched capacitor converter. The transfer function model of the QBSCC is derived using the reduced order model state equations. The simulation is carried out for the QBSCC with HMSMC controller and PI controller. The steady state and dynamic response of the converter with controllers are analyzed. It is found that the response for the QBSCC with HMSMC is much better due to reduction in peak overshoot and reduction in voltage and current ripples. Overall, the performance of the QBSCC got improved with HMSMC and efficiency got improved considerably.

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