LIMIT VALUES OF CAPACITORS IN MULTILEVEL INVERTERS

Cristian HELERA [1], Dan Alexandru STOICHESCU [2]

Because the power source of an electric vehicle is DC and its motor requires AC power, an inverter is always necessary. The most attractive are multilevel inverters whose output voltage is close to a sinusoid. The indispensable components in these inverters are the capacitors. Based on an analysis of the charging and discharging processes of the capacitors in two 5-level inverters (one of switched capacitor type and the second of diode-clamped multilevel type), the mathematical expressions of the capacity limit values are determined, which represents the scope of this paper.

Keywords: multilevel inverters; 5-level; switched capacitor inverters; diode clamped multilevel inverters

1. Introduction

In previously published articles [1],[2],[3],[4] we showed that DC electric energy can be obtained using vehicle mounted wind turbines or solar panels. This energy is inadequate to power a vehicle electric motor which needs a sinusoid voltage. Therefore, a power conditioning unit is necessary and most recommended units are, in recent years literature, the multilevel inverters as their output voltage is close to a sinusoid waveform. That is why research was carried out aimed at perfecting their electrical schemes. In [5] a method to reduce the number of the multilevel inverter components was developed; in [6] their merits are emphasized and several modulation strategies are analyzed to decide which is the optimal one.

In any multilevel inverter structure, there are one or more capacitors that must ensure short voltage fronts and keep constant the voltage at their terminals during the voltage levels. If their capacities are too large or too small, the inverter output waveform no longer approximates a sinusoid well enough; therefore, establishing calculation relationships for the minimum and maximum values of the inverter capacitors is necessary.

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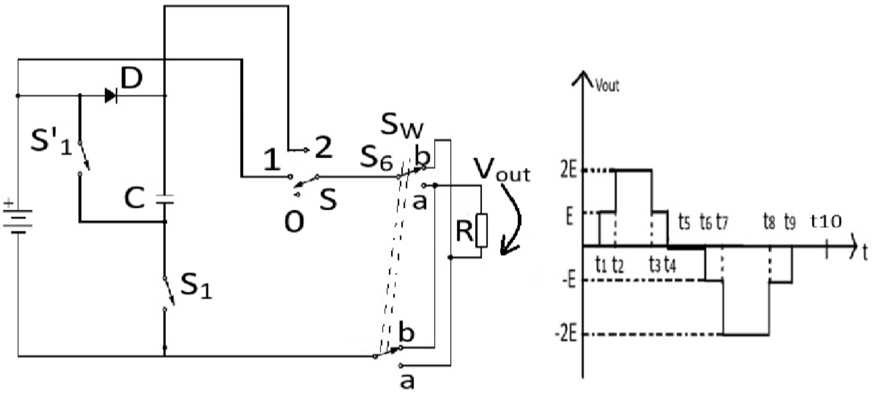
In this article, the charging and discharging processes of the capacitors in two types of inverters are analyzed. In section 2, limit values of capacitors in switch capacitor multilevel inverters are determined. In section 3 the same operation is carried out for capacitors in diode-clamped multilevel inverters. Calculation formulas useful in design are obtained.

2. Switched capacitor multilevel inverters.

The principle of operation of switched capacitor multilevel inverters is illustrated by the electric circuit of the 5-level inverter (Fig.1.a) and its waveforms (Fig..1b).



a) b)

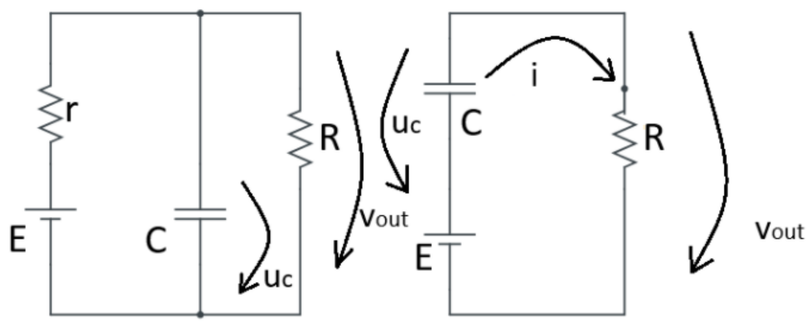
Fig. 1 Five-level switched capacitive multilevel inverter [7]

a) Electric diagram; b) Load voltage waveform v_{out}

Switches S_1 and S_1' switch mutually exclusively; that is, when $S_1$is on, S_1' is off and vice versa. To obtain the waveforms in Fig.. 1.b, the successive positions of switches are as follows [7]:

- S_w contacts are on position a during the time interval 0 – t_5 and on position b during the time interval t_5- t_{10}.Type equation here.
- during the time intervals 0 - t_1, $t_4 - t_6, t_9$ - t_{10}, the switch S is in position 0 and the other switches are on or off.
- during the time intervals $t_1 - t_2, t_3 - t_4, t_6 - t_7, t_8 - t_9$, switch S is on position 1, S_1 is on and S_1' is off; the capacitor C is charged through the diode D with voltage E and the voltage applied to the load, v_{out}, is E during $t_1 - t_2$, $t_3 - t_4$ and -E during $t_6 - t_7$, $t_8 - t_9$; the equivalent circuit of the inverter for the time intervals $t_1 - t_2$ and $t_3 - t_4$ is represented in Fig..2.a.

- during the time intervals $t_2 - t_3$ and $t_7 - t_8$, S is on position 2, S_1 is off , which leads to the blocking of diode D and the voltage on the load is 2E in the interval $t_2 - t_3$ and -2E in the interval $t_7 - t_8$. The equivalent circuit of the inverter in the interval $t_2 - t_3$ is represented in Fig..2.b.



a) *b)*

Fig.2 a) Equivalent circuit of the inverter during the time intervals $t_1 - t_2$ *and* $t_3 - t_4$
b) Equivalent circuit of the inverter during the time interval $t_2 - t_3$.

The value of the capacitor C is limited above by the condition that the durations of the voltage fronts Fig.. 1.b to be as short as possible. During a rising front – for example, the front at moment t_1– the capacitor C is charged from electromotive force (emf) E through the internal resistance of the source and the internal resistance of the open diode D. The sum of these resistances is r. The equivalent circuit is the one in Fig.. 2.a.

The expression of the capacitor voltage is:

$$u_c = E\left(1 - e^{-\frac{t}{\tau}}\right) \quad \text{where } \tau = rC. \qquad (1)$$

Considering that the front ends at time Δt, when $u_c(\Delta t)$ = 0,9E, it follows:

$$E\left(1 - e^{-\frac{\Delta t}{\tau}}\right) = 0{,}9\ E \qquad (2)$$

so that it results:

$$\frac{\Delta t}{\tau} = -\ln 0{,}1 = 2{,}3 \qquad (3)$$

$$\tau = rC = \frac{\Delta t}{2{,}3};\ C = \frac{\Delta t}{2{,}3r} \qquad (4)$$

The capacity C is limited below by the condition that in intervals t_2- t_3 and t_2- t_8, the voltage on it does not decrease significantly.

According to figure 2b, in these intervals the capacitor C tends to discharge from the value E to zero and charge to the value -E.

Equating the sum of voltages in the circuit represented in Fig. 2b to zero, results:

$$R_i - u_C = E \tag{5}$$

Since $i_C = -C\frac{du_C}{dt}$, relation (5) becomes:

$$-RC\frac{du_C}{dt} - u_C = E \;\; \rightarrow \;\tau\frac{du_C}{dt} - u_C = E \quad \text{where } \tau = RC. \tag{6}$$

The Laplace transform of equation (6) is:

$$\tau(s\,U_C(s) - u_{C0}) + \;U_C(s) = -\frac{E}{s} \text{ where } u_{C0} = E. \tag{7}$$

The solution of (7) is deduced:

$$U_C(s)(\tau s + 1) = \tau E - \frac{E}{s} \tag{8}$$

$$U_C(s) = E\frac{\tau s - 1}{\Delta(\tau s + 1)} = E\left(\frac{A}{s} + \frac{B}{s + \frac{1}{6}}\right) \tag{9}$$

The constants A and B are found to be A = -1; B = 2 and (9) becomes:

$$U_C(s) = -\frac{E}{s} + 2\frac{E}{s + \frac{1}{\tau}} \tag{10}$$

Laplace transform inversion of equation (10) is found to be:

$$u_C(t) = E(2e^{-\frac{t}{\tau}} - 1) \tag{11}$$

If it is desired that at the end of the interval $t_2 - t_3$ denoted t_{23}, the voltage u_C to decrease by only 10% of the initial value E, the expression of the capacity C is deduced from (11):

$$u_C(t_{23}) = E\left(2e^{-\frac{t_{23}}{\tau}} - 1\right) = 0{,}9\,E \tag{12}$$

$$e^{-\frac{t_{23}}{\tau}} = 0{,}95 \tag{13}$$

$$\frac{t_{23}}{\tau} = -ln0.95 = 0.051 \tag{14}$$

$$C = \frac{t_{23}}{0{,}051R} \tag{15}$$

3. Diode-Clamped Multilevel Inverters

The principle of operation of diode-clamped multilevel inverters is illustrated by the circuit diagram of the 5-level inverter in Fig.3. Its output diagram is identical to the diagram in Fig.1. b.

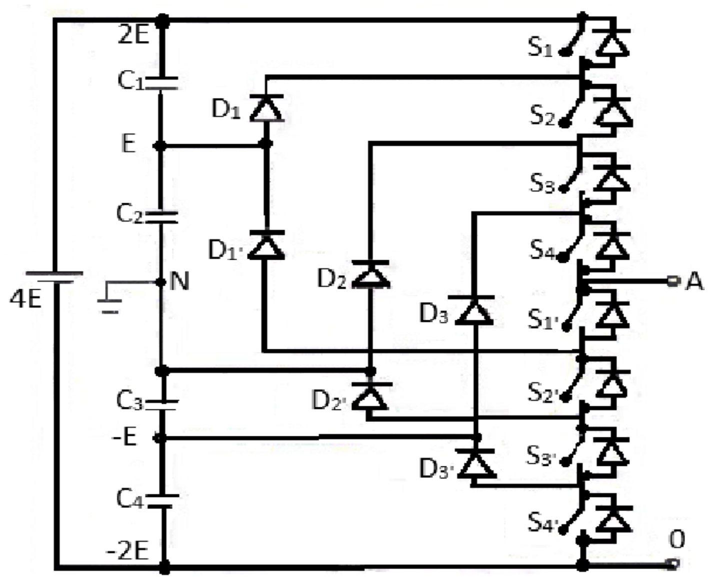


Fig.3 Five level diode-clamped multilevel inverter [7]

In order to get the desired output voltage levels, 8 switching devices are connected in series (Fig..3). The load resistance is connected between the points A and N. The 5 voltage levels of the output are synthesized by the following switch combinations (see Fig. 1b) [8]:

- during the time intervals 0-t_1, t_4-t_6, t_9-t_{10}, switches S_3, S_4, S'_1 and S'_2 are on and all others are off; $V_{AN} = 0$.
- during the intervals t_1-t_2 and t_3-t_4, switches S_2, S_3, S_4 and S'_1 are on and all others are off; $V_{AN} = E$. (the equivalent circuit diagram is represented in Fig. 4).
- during the intervals t_2-t_3, the switches S_1 - S_4 are on and switches S'_1 -S'_4 are off (the equivalent circuit diagram is represented in Fig.. 4; $V_{AN} = 2E$.
- during the intervals t_6-t_7 and t_8-t_9, the switches S_4, S'_1, S'_2, S'_3 are on and all others are off; $V_{AN} = -E$.
- during the interval t_7-t_8, the switches $S'_1 – S'_4$ are on and $S_1 – S_4$ are off; $V_{AN} = -2E$

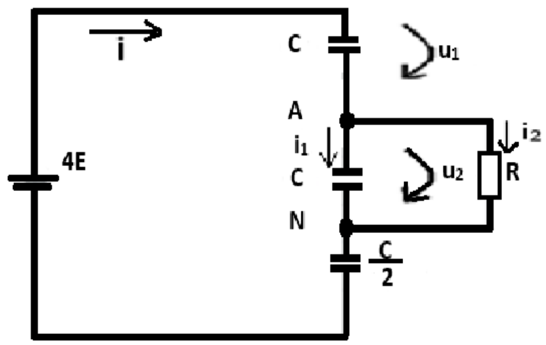


Fig.4. Equivalent circuit diagram of the inverter in Fig.3, during the time interval $t_2 - t_3$ when $V_{AN} = E$

In the diagram in Fig. 4, Kirchhoff first law is applied in node N:

$$i_1 + i_2 = i \qquad (16)$$

As $$i = C\frac{du_1}{dt} = \frac{C}{2}\frac{du_3}{dt} \qquad (17)$$

It results: $$2u_1 = u_3 \qquad (18)$$

as: $$u_1 + u_2 + u_3 = E \Rightarrow u_1 = \frac{E-u_2}{3} \qquad (19)$$

The currents in (16) are expressed in terms of the voltages u_1 and u_2:

$$C\frac{du_2}{dt} + \frac{u_2}{R} = C\frac{du_1}{dt} \qquad (20)$$

Introducing u_1 from (19) in (20) yields:

$$C\frac{du_2}{dt} + \frac{u_2}{R} = -\frac{C}{3}\frac{du_2}{dt} \qquad (21)$$

identical to $$\frac{4}{3}CR\frac{du_2}{dt} + u_2 = 0 \qquad (22)$$

Applying the Laplace transform of relationship (22), results:

$$\left(s\tau + \frac{3}{4}\right)U_2(s) = \tau E \text{ where } \tau = CR \qquad (23)$$

The solution of (23) and its inverse Laplace transform are:

$$U_2(s) = \frac{E}{s+\frac{3}{4\tau}}; \qquad u_2(t) = E\ e^{-\frac{3}{4}\frac{t}{\tau}} \qquad (24)$$

If it's desired that in the intervals t_1-t_2, t_3-t_4, t_6-t_7, t_8-t_9, having the duration t_{12}, the output voltage u_2 should decrease by only 10%, the following condition is imposed:

$$u_2(t_{12}) = E\ e^{-\frac{3}{4}\frac{t_{12}}{\tau}} = 0{,}9E \qquad (25)$$

The limit value of the capacity C results from (25):

$$\frac{3}{4}\frac{t_{12}}{\tau} = -ln0{,}9 = 0{,}1 \tag{26}$$

$$\tau = \frac{3t_{12}}{4x0{,}1} = 7{,}5\, t_{12} \tag{27}$$

$$C = \frac{7{,}5\, t_{12}}{R} \tag{28}$$

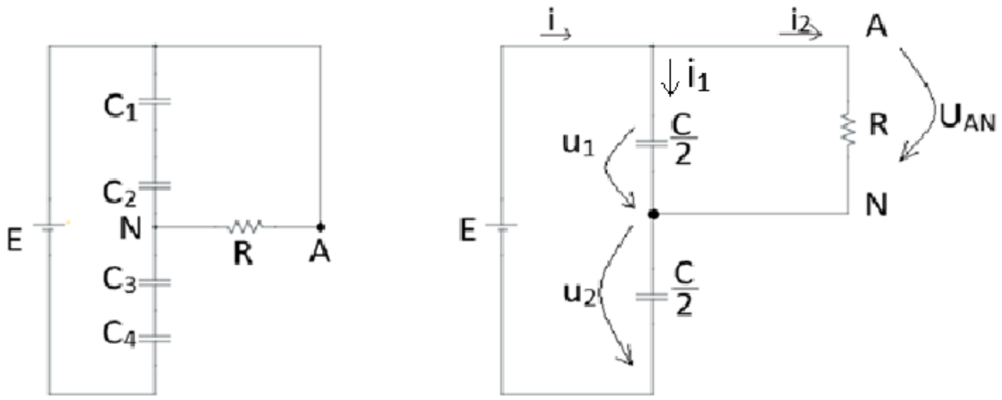


Fig.5 a) Equivalent circuit diagram of the diode-clamped multilevel inverter in Fig. 3 during time interval $t_2 - t_3$,when V_{AN}=2E. b) New version of the inverter circuit diagram in the same time interval.

Another condition imposed on the capacitors in the diode-clamped multilevel inverter in Fig..3 is deduced by observing its operation during the interval $t_2 - t_3$. In Fig..5.a is drawn an obviously equivalent diagram of the inverter and in Fig..5.b a new version of this diagram more suitable for the analysis is presented.

In the diagram in Fig.. 5b, Kirchhoff first law is applied in node N and the currents i_1, i_2, i are expressed using the voltages on the capacitors u_1 and u_2 :

$$i_1 + i_2 = i \tag{29}$$

$$\frac{C}{2}\frac{du_1}{dt} + \frac{u_1}{R} = \frac{C}{2}\frac{du_2}{dt} \tag{30}$$

as u_2=E-u_1, relation (30) becomes:

$$\frac{C}{2}\frac{du_1}{dt} + \frac{u_1}{R} = -\frac{C}{2}\frac{du_1}{dt} \tag{31}$$

Consequently:

$$RC\frac{du_1}{dt} + u_1 = 0 \tag{32}$$

Applying the Laplace transform of relationship (32), yields:

$$RC(U_1(s) - u_{10}) + U_1(s) = 0 \tag{33}$$

as u_{10} = 2E, one may write equivalently:

$$U_1(s)(\tau s + 1) = 2\tau E \text{ where } \tau = RC \tag{34}$$

The solution of (34) and its Laplace transform are:

$$U_1(s) = \frac{2E}{s+\frac{1}{\tau}} \tag{35}$$

$$u_1(t) = 2E\ e^{-\frac{t}{\tau}} \tag{36}$$

If it is desired that at the end of the interval t_{23}, the voltage u_1 decreases by only 10% of the initial value 2E, the value of the capacitor C is deduced as follows:

$$2E\ e^{-\frac{t}{\tau}} = 0{,}9\ x\ 2E \tag{37}$$

$$\frac{t_1}{\tau} = -\ln 0{,}9 = 0{,}1 \tag{38}$$

$$C = \frac{\tau}{R} = \frac{10\ t_{2/3}}{R} \tag{39}$$

4. Conclusions

In this article, an element less treated in specialized literature is taken into consideration, namely the conditions imposed on the values of the of the capacitors in the multilevel inverters so that the rectangular pulses that make up the waveform of their output are as little distorted as possible. The capacities must be large enough so that the level of the pulses is as close as possible to the horizontal and do not exceed certain limit values in order not to increase the duration of the front pulse fronts.

R E F E R E N C E S

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