LEAKAGE INDUCTANCE OPTIMIZATION FOR PHASE-SHIFTED FULL-BRIDGE DC-DC CONVERTER

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When designing a high power Phase-Shifted Full-Bridge DC-DC (FSFB) converter for an Electrical Vehicle (EV), one of the main objectives is high efficiency across wide output load. Achieving high efficiency at half to full load is usually not difficult but at light load is always a challenge. For PSFB DC-DCconverters the main parameter for tuning the efficiency at light load is the leakage inductance. In this paper a more precise method for calculating the minimum leakage inductance for PSFB DC-DC converter will be investigated. The proposed method takes in the account all converter parameters like input and output voltage range, transformer and switching devices equivalent resistance and transformer magnetizing inductance. The optimum leakage inductance should ensure reaching the desired efficiency at specified load with minimum duty-cycle loss. The derived equations are validated in a numerical example and simulations.

Keywords: automotive DC-DC converter design, leakage inductance, Phase-Shifted Full-Bridge, zero voltage switching

1. Introduction

The power density and efficiency targets have increased rapidly over the last years leading to higher switching frequencies and smaller magnetics. Increasing the switching frequency comes naturally with higher switching losses for power switches and magnetic devices having a tendency to be dominant [1]. As for magnetic components, there are multiple options in selecting the core material, shape and flux density to minimize the core and windings losses, for switching devices it is necessary to find new ways to reduce the switching losses.

Majority of the switching losses are generated when the semiconductor devices change their state from ON to OFF and vice-versa due to hard switching. Therefore, the most efficient way to reduce the switching losses of power semiconductors is to ensure soft switching in form of zero voltage switching (ZVS) across drain-to-source for the MOSFET devices and zero current switching (ZCS) between collector and emitter for IGBT devices. Soft switching can reduce or even eliminate the turn on/off losses increasing the efficiency of the converter

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[2], [3], [4]. Thus, the PSFB DC-DC converter analyzed in this paper is based on MOSFET switching devices and the study is focused on achieving ZVS only.

The typical power electrical diagram of an EV is provided in Fig. 1. The role of the DC-DC converter is to supply the low voltage car network and to charge the 12V battery. The car LV network supplies all sensitive consumers like the engine computer, airbags, braking and lights systems. For this reason, the DC-DC converter must be efficient and extremely reliable.

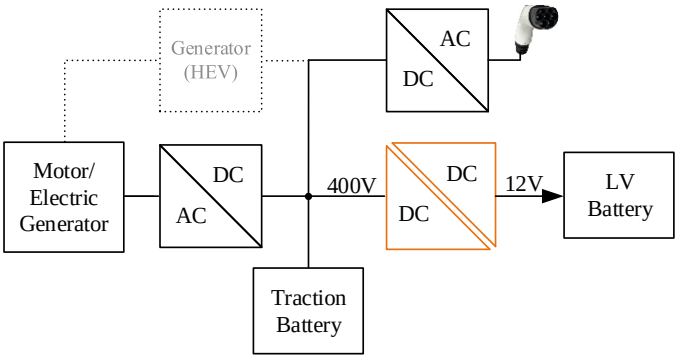

Fig. 1. Typical power electrical diagram of an EV

The paper is organized as follows. The DC-DC converter and its main waveforms are explained in Section 2. The leakage inductance provides energy during dead-times for charging and discharging of parasitic capacitances, ensuring soft switching for primary stage switches. Thus, in Section 3, the equation for determining the leakage inductance is obtained by considering the design constraints and circuit elements. In Section 4, a numerical example is presented. In Section 5, the leakage inductance is evaluated by simulations. Finally, the conclusions are given.

2. Phase-Shifted Full-Bridge DC-DC converter

As mentioned in the previous chapter, the scope of this study is to find the optimum value of leakage inductance for a PSFB DC-DC converter. In Fig. 2, the electrical diagram of the converter is presented [5].

This topology is commonly used for energy conversion from high voltage battery to the 12 V battery and for supplying the low voltage network in hybrid and electric vehicles. The main benefits of the topology are:

- High power density
- High efficiency due to soft switching
- Galvanic isolation

In Fig. 3, the main waveforms of the converter are provided [6]. Neglecting the dead time, the operation is the following:

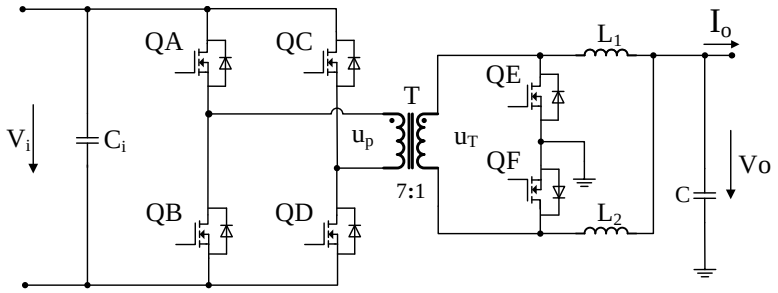

Fig. 2. Phase-Shifted Full-Bridge DC-DC converter

- $[t_0, t_1]$: the voltage u_T is positive due to conduction of QA and QD. QE is turned off and QF is turned on. The transformer secondary current is equal with i_{L1}. During this interval, entire load current is passing through QF.
- $[t_1, t_2]$: u_T is zero during this interval due to simultaneous conduction of QA and QC. The QE and QF switches are also in conduction. The L_2 current ramp i_{L2} is constant while the current ramp through L_1 becomes negative due to negative voltage across L_1.
- $[t_2, t_3]$: u_T is negative due to conduction of QC and QB. QE is also turned on, while QF is turned off. The transformer secondary current is equal with i_{L2} current and QE sustains the entire load current.
- $[t_3, t_4]$: u_T is again zero, QB, QD, QE and QF are in conduction. The current ramp i_{L1} remain constant while the current ramp through L_2 becomes negative due to negative voltage across L_1.

3. Leakage inductance calculation

When calculating the value of leakage inductance, the following parameters must be taken in the account:

- Parasitic capacitances of the primary switching devices
- Parasitic capacitance of the transformer
- Minimum output current value from where the soft switching (ZVS) is required.

The schematic of PSFB converter together with primary switches parasitic capacitances (CA, CB, CC, CD) is presented in Fig. 4. The leakage inductance (L_k) has an important role in the operating of the converter since the energy stored helps to achieve soft switching (ZVS) for primary switches (QA, QB, QC, QD). The soft switching reduce the commutation losses and increases the overall efficiency of the converter.

The condition to reach ZVS on primary switches is that the energy stored in leakage inductance (E_{Lk}) to be minimum equal to the one stored in parasitic capacitances (E_{cap}) from primary side of the converter.

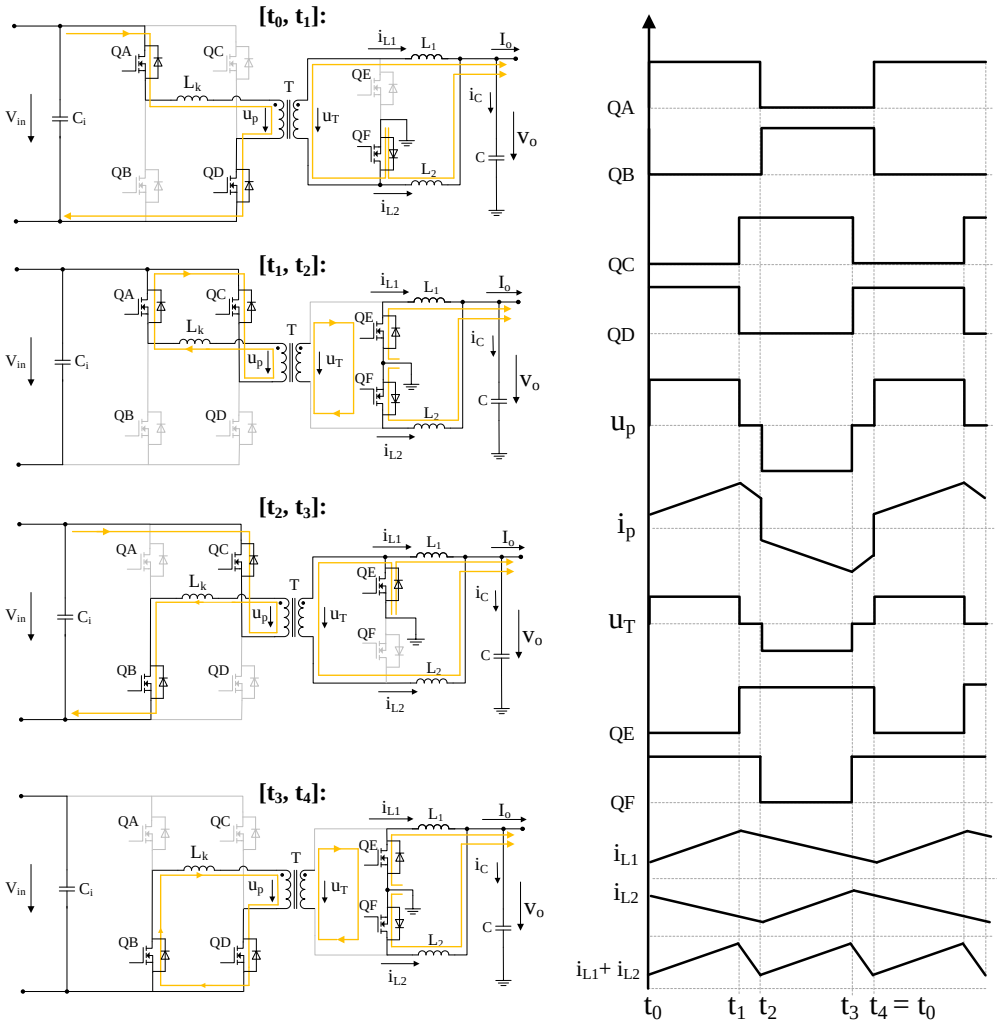

Fig. 3. Main waveforms of the Phase-Shifted Full-Bridge DC-DC converter

$$E_{Lk} \geq E_{cap} \tag{1}$$

The energy stored in the parasitic capacitances is given by:

$$E_{cap} = \frac{1}{2}\left(2C_{oss} + C_{tr}\right) \cdot V_{in}^2 \tag{2}$$

where, V_{in} is the input voltage, the C_{oss} is the primary switch parasitic capacitance and C_{tr} is the parasitic capacitance of the transformer. The C_{oss} value can usually be found in the device datasheet.

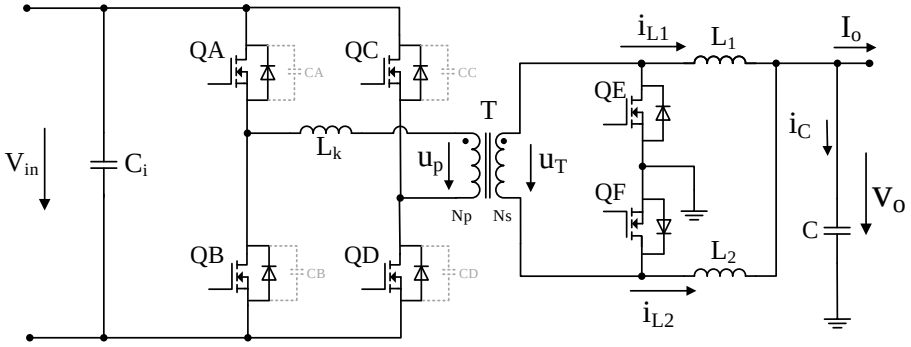

Fig. 4. Schematic of PSFB DC-DC converter with parasitic capacitances shown

The energy stored in the leakage inductance is:

$$E_{Lk} = \frac{1}{2} L_k I_d^2 \tag{3}$$

where, I_d is the instantaneous current value through leakage inductance just before switch transition.

In the worst-case situation, the value of I_d is equal with value of I_{dMIN2} which is the primary current value just before transformer voltage change the polarity, as shown in Fig. 5.

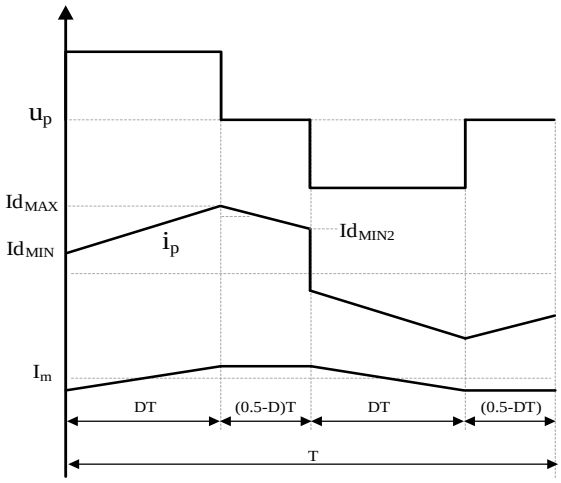

Fig. 5. Primary side waveforms of the PSFB DC-DC converter

In Fig. 5, the following notation was used:

- u_p, voltage across primary winding of the power transformer
- i_p, transformer primary current
- I_m, magnetization current reflected to the primary winding

- T, switching period
- D, duty cycle.

$$T = \frac{1}{F_{sw}} \tag{4}$$

$$D = \frac{V_o}{V_{in}} \cdot \frac{N_p}{N_s} \tag{5}$$

where, V_o is the output voltage, F_{sw} is the switching frequency, N_p and N_s are the number of turns of primary and secondary windings of transformer.

In order to calculate the value of I_{dMIN2}, some simplification of schematic from Fig.4 must be made. Therefore, during [DT, (0.5-D)T] interval the secondary side rectifiers (QE and QF) are both activated in the same time with primary switches QA and QC. During this interval, the schematic from Fig.4 can be reduced to one from Fig. 6. $Rdson_{PR}$ and $Rdson_{SR}$ are the equivalent drain-to-source resistance of primary respectively secondary rectifiers switches. R_{prim} and R_{sec} are primary and secondary windings resistance.

The circuit from Fig. 6 is a typical "RL" (resistor-inductor) circuit. This means that if the initial current I_{dMAX}, magnetization current I_m and all circuit components are known, the value of I_{dMIN2} can be determined. Therefore, the value of Id_{MIN2} can be calculated with the relation below:

$$I_{dMIN2} = I_{dMAX} \cdot e^{-\frac{R_e}{L_k}\cdot(0.5-D)\cdot T} + \frac{I_m}{2} \tag{6}$$

where, L_k is the leakage inductance, R_e is the sum of equivalent resistances reported to primary side according to Fig. 6:

$$R_e = 2Rdson_{PR} + R_{prim} + \left(R_{\text{sec}} + 2Rdson_{SR}\right)\cdot\left(\frac{N_p}{N_s}\right)^2 \tag{7}$$

The I_m is the magnetization current and can be calculated with relation below:

$$I_m = \frac{V_{in}\cdot D}{L_p \cdot F_{sw}} \tag{8}$$

where, L_p is the magnetization inductance reported to primary side.

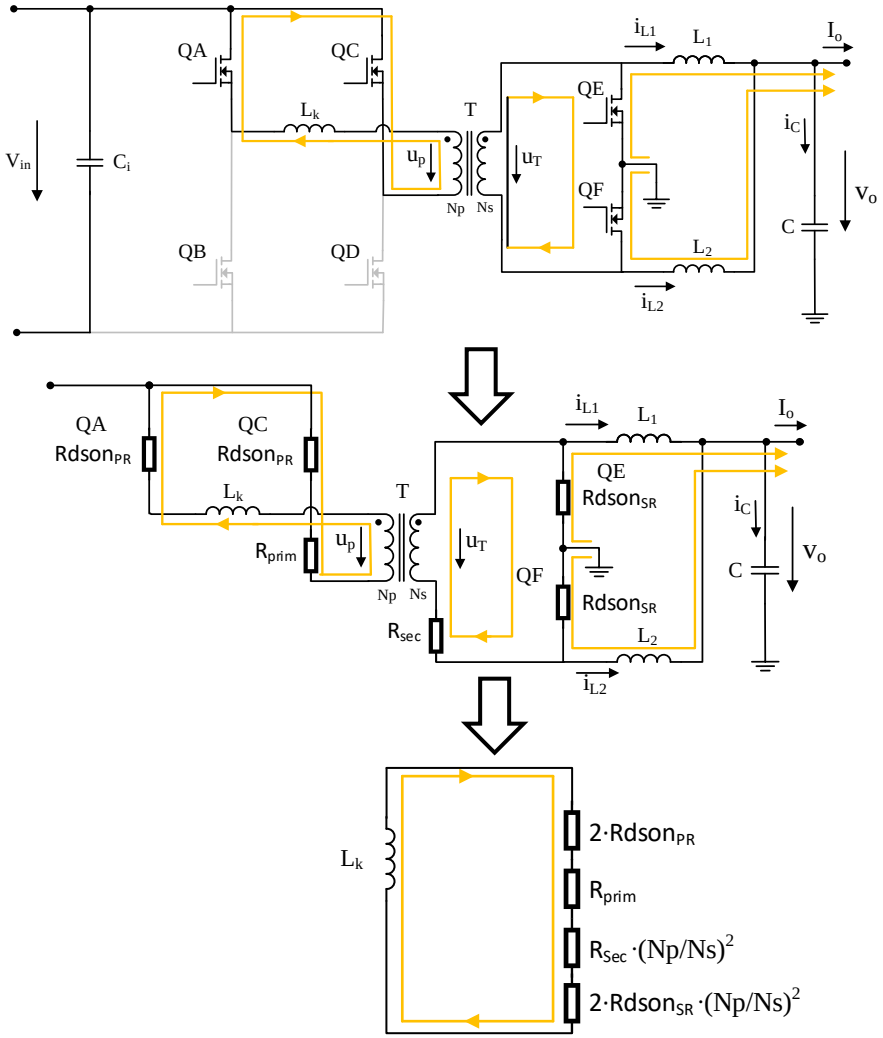

Fig. 6. Schematic simplification for time interval [DT, (0.5-D)T]

As it can be observed from equation (6), the I_{dMIN2} is a function of peak current I_{dMAX}, converter duty cycle, magnetization current, equivalent resistance, circuit components but also of leakage inductance. This means that value of leakage inductance cannot be directly determined from equation (6) as the I_{dMIN2} is also a function of L_k. Therefore, the value of the minimum leakage inductance can be found iteratively by giving values to L_k and solve (6) for I_{dMIN2} and calculating equation (3) by replacing I_d with I_{dMIN2} until equation (1) is satisfied.

In order to solve equation (6), the peak value of the secondary winding current reported to primary winding I_{dMAX} must be known. The primary current is

the sum of the magnetization current and output inductor current I_{Lo_max} reported to primary side.

$$I_{dMAX} = I_{Lo\_\max} \cdot \frac{N_s}{N_p} \tag{9}$$

The output inductor current is a function of the converter output current I_o, input voltage V_{in}, output voltage V_o, transformer turns ratio and inductance value L_o [5] as shown in equations (10) and (11).

$$I_{Lo\_\max} = \frac{I_o}{2} + \frac{\Delta i_{Lo}}{2} \tag{10}$$

The Δi_{Lo} is output inductor ripple current that can be calculated with equation below:

$$\Delta i_{Lo} = \frac{\left(V_{in} \cdot \frac{N_s}{N_p} - V_o \right) \cdot D}{L_o \cdot F_{sw}} \tag{11}$$

By combining equation (10) and (11), we obtain:

$$I_{Lo\_\max} = \frac{1}{2} \cdot \left(I_o + \frac{\left(V_{in} \cdot \frac{N_s}{N_p} - V_o \right) \cdot D}{L_o \cdot F_{sw}} \right) \tag{12}$$

Finally, by replacing (12) in (9), the equation for I_{dMAX} is obtained:

$$I_{d\max} = \frac{1}{2} \cdot \frac{N_s}{N_p} \cdot \left(I_o + \frac{\left(V_{in} \cdot \frac{N_s}{N_p} - V_o \right) \cdot D}{L_o \cdot F_{sw}} \right) \tag{13}$$

The value of I_{dMIN2} can be calculated if (8) and (13) are introduced in equation (6).

$$I_{dMIN2} = \frac{1}{2} \cdot \left(\frac{N_s}{N_p} \cdot \left(I_o + \frac{\left(V_{in} \cdot \frac{N_s}{N_p} - V_o \right) \cdot D}{L_o \cdot F_{sw}} \right) \cdot e^{-\frac{R_e}{L_k}(0.5-D) \cdot T} + \right. \\ \left. + \frac{V_{in} \cdot D}{L_p \cdot F_{sw}} \right) \tag{14}$$

The total leakage inductance energy can now be calculated by using the equation (3) and replacing I_d with I_{dMIN2}:

$$E_{Lk} = \frac{1}{2} L_k \cdot (I_{dMIN2})^2 \tag{15}$$

As can be observed from equations (14) and (15) the amount of energy stored in the leakage inductance depends on multiple parameters like:

- Equivalent series resistance of semiconductors and magnetic components reflected to primary side of the converter
- Transformer magnetizing inductance
- Output inductor
- Input voltage
- Output voltage
- Output current
- Switching frequency

In order to find the optimum leakage inductance value, the worst case must be identified. This can be done by selecting a minimum value of output current from which full ZVS is required. Considering a value close to zero is usually not a good idea because the required leakage inductance would be too large leading to significant voltage drop across it. The voltage drop across leakage inductance can be expressed also as duty-cycle loss and can be calculated with the equation (16) as shown below [5].

$$\delta D = \frac{L_k \cdot I_o}{V_{in}} \cdot \frac{N_s}{N_p} \cdot F_{sw} \tag{16}$$

In general, a value of the minimum current between 10% and 30% of nominal current is a good choice. This ensures high efficiency for wide output load range with minimum duty-cycle loss.

4. Numerical example

The derived equations from previous chapter will be used to find the optimum leakage inductance value for a PSFB DC-DC converter. The specifications of the converter are presented in Table 1.

Table 1

PSFB DC-DC converter design parameters

Parameter	Value	Parameter	Value
V_{in} range	260 V - 420 V	L_p	147 µH
V_o range	12 V - 16 V	R_{prim}	25 mΩ
I_o range	20 A - 115 A	R_{sec}	1 mΩ
P_o	1600 W	$Rdson_{PR}$	110 mΩ
F_{sw}	200 kHz	$Rdson_{SR}$	2.5 mΩ
N_p / N_s	7 / 1	C_{oss}	120 pF
L_o	1.25 µH	C_{tr}	110 pF

By considering the design parameters from Table 1 and equations (14), (15), the worst-case conditions for the converter to reach ZVS, are the following:

- Minimum output current
- Minimum output voltage
- Maximum input voltage

The minimum leakage inductance required to reach ZVS is 2.84µH and can be found at the intersection of the parasitic capacitance energy with the energy stored in leakage inductance as shown in graph from Fig. 7. At the same point, the duty-cycle loss δD can be also evaluated at a value of 0.0225.

In Fig. 8, the available leakage inductance energy as function of output current at different output voltages is presented. The intersection of the energy curves reveal the minimum output current from where the available energy is sufficient for the converter to reach ZVS. As can be observed the worst case situation is at minimum output voltage (12V) and output current (20A).

The results show that at higher output voltage levels the available leakage inductance energy is also higher. This means that the converter can reach ZVS even from zero load if the output voltage is set to a value ≥ 16 V.

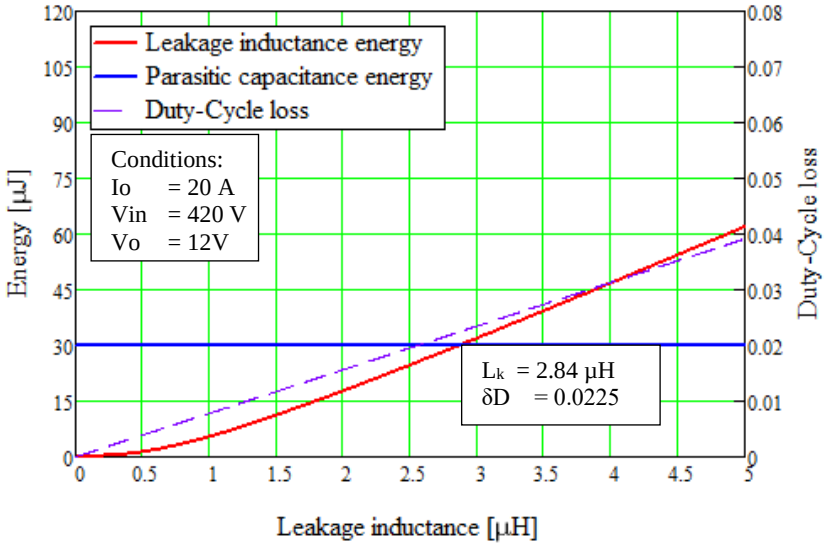

Fig. 7. Leakage inductance energy vs. leakage inductance

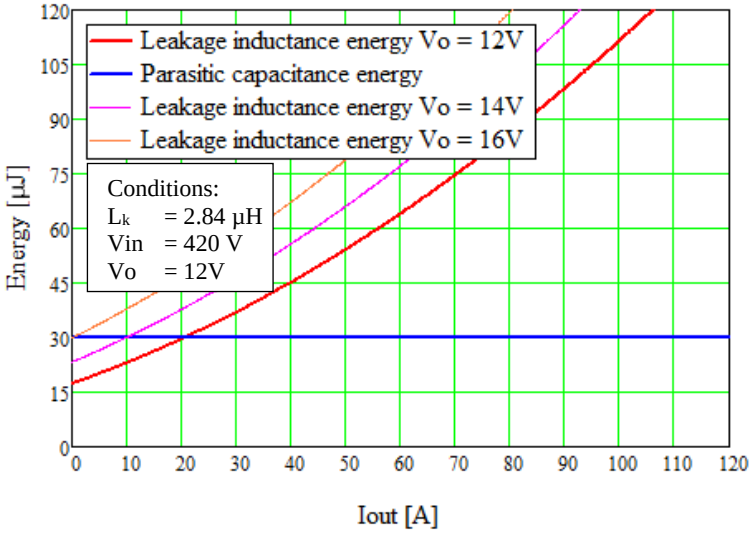

Fig. 8. Leakage inductance energy vs. converter output current

The leakage inductance energy can be also plotted against converter input voltage (Fig. 9a) and versus transformer magnetizing inductance (Fig. 9b). As expected, the available leakage energy drops slightly with rise of input voltage but the parasitic capacitance energy increases at higher rate due to V_{in} squared from equation (2).

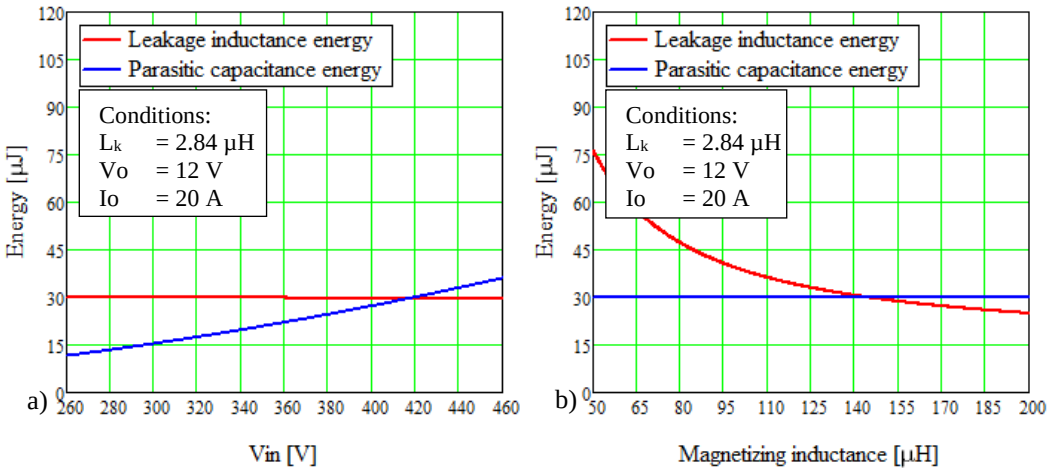

Fig. 9. a) Leakage inductance energy vs. input voltage; b) Leakage inductance energy vs. output current at different output voltages

According to the results from Fig. 9b, the available leakage inductance energy can be increased also by reducing the magnetizing inductance. The drawback of this measure is that it increases the conduction losses due to higher circulating current in the primary side of the converter. Depending on the situation, increasing the magnetizing current can be beneficial, allowing the converter to reach ZVS at lower output load with minimum duty-cycle loss.

5. Converter simulation

In order to confirm the previous derived equations, the converter with design parameters from Table 1 is simulated using PSIM software. In the Fig. 10, the converter is simulated with a leakage inductance of 1µH. It can be seen in the voltage waveforms UQA and UQB that the capacitances of the primary switches QA and QB are not fully charged/discharged during dead-time. This means that only a partial ZVS condition is reached because the leakage inductance is insufficient.

In the Fig. 11, the simulation from Fig. 10 was done one more time but with a leakage inductance of 2.84µH as calculated in the previous chapter. As can be observed, in this case, the energy stored in the leakage inductance is sufficient to ensure soft transition (full ZVS) for all primary switches.

6. Conclusions

In this paper, a more precise method for calculating the leakage for PSFB converter was presented. The proposed method takes in the account all converter

parameters like input and output voltage range, transformer and switching devices equivalent resistance and transformer magnetizing inductance.

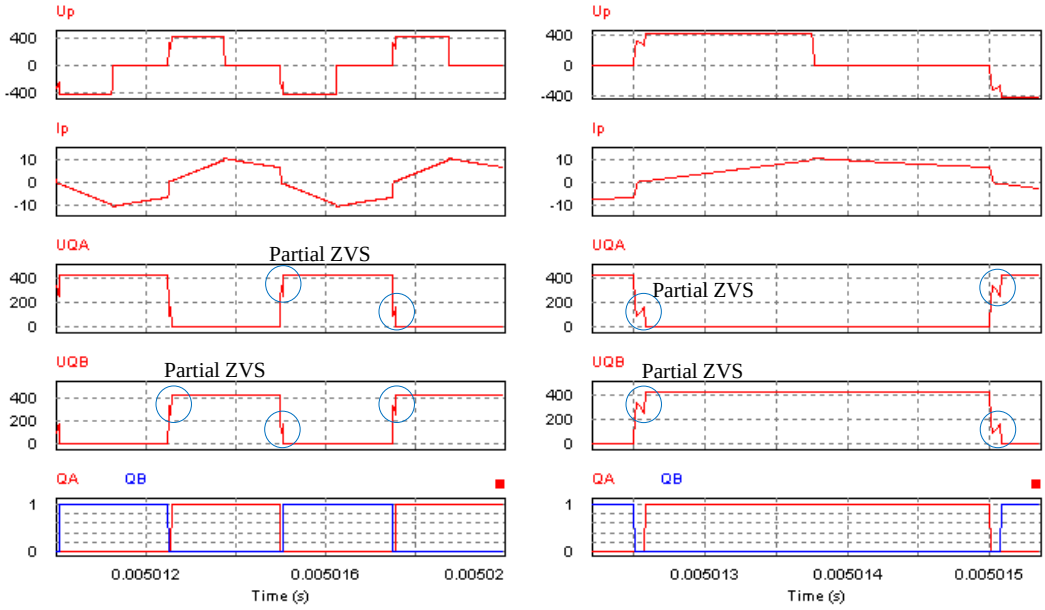

Fig. 10. Simulation of PSFB converter with L_k = 1µH, V_{in} =420V, V_o= 12V and I_o = 60A: a) Full cycle overview, b) Half cycle zoom-in.

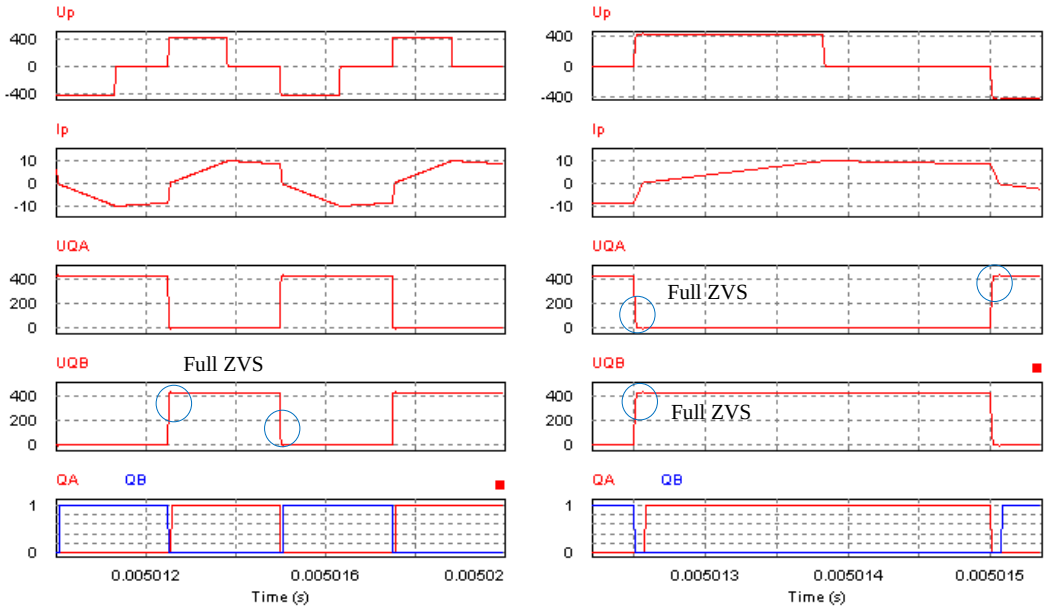

Fig. 11. Simulation of PSFB converter with L_k = 2.84µH, V_{in} =420V, V_o= 12V and I_o = 60A. a) Full cycle overview, b) Half cycle zoom.

The main criteria used as starting point is the minimum output current from where the ZVS for primary switches is required. In the ideal case, the ZVS is desired for the complete output current range, from no load to full load but this presents an important drawback. It leads to large leakage inductance value and significant duty-cycle loss. Depending on the situation, the magnetizing inductance could be used as tuning parameter to extend the ZVS range. By reducing the magnetizing inductance, the transformer primary current is increased and so the leakage inductance energy. This solution has the advantage that does not increase the duty-cycle loss, but it has the drawback that increases the primary circulating current. The optimum solution is often a compromise between leakage inductance value and magnetizing current.

R E F E R E N C E S

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