AN INNOVATIVE METHOD FOR LOW-EMI PWM GENERATION IN INVERTERS

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This paper shows an innovative but rather simple method to implement a pulse width modulator for inverters, in compliance with today's EMI standards. This improvement over the previous designs would reunite the lower part count of the square wave inverter, with the minimal distortion specific to a sine wave inverter. The novelty consists in generating a low frequency, low distortion wave by mixing two high frequency square waves. This paper presents theoretical basics, a system-level simulation in Matlab, and an experimental model simulated in LTSpice.

Keywords: Power inverter, PWM generator

1. Introduction

Power inverters [1][2] are used most commonly as power household devices in areas where there is no access to the national power grid. They are used to raise the voltage from a battery pack or an unconventional energy generator (wind mill or solar panel) to a signal which has a Root Mean Square value of 230V and 50Hz.

The main issue for the actual inverter represents the PWM generator (usually representing a simple square wave generator with high EMI), the output efficiency and, finally, the EMI which, for the actual electronics devices, represent a true goal [3].

This paper intends to achieve a good EMI using an innovative PWM generator and a good efficiency using cheaper and a lower count of electronic components.

2. Application

Based on the output waveform, there are two important inverter categories:

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a. Square wave inverters. These are the simplest type of inverters, which generates a symmetrical square wave, usually based on a high frequency Dc-Dc converter.

b. Sine wave inverters. These are more complicated than the square wave inverter. A common method is to generate a 50Hz sine wave which is applied to a class B or class D power amplifier, connected to a line-frequency transformer. This needs a large and expensive transformer and has a low efficiency.

The square wave inverters are simple, have a high efficiency but are not suitable for inductive loads (such as transformers or electric motors), because they have a high level or harmonics. The sine wave inverters are more complex, more expensive, and usually have a lower efficiency, a very low level of THD (Total Harmonic Distortion) than square wave inverters. Consequently, the sine wave inverters have the lowest EMI.

3.**Basic operation**

This article aims to present a new PWM generator which could assure a better efficiency and EMI, with cheaper electronic components and better integration – high electronic density. The concept is based on the following diagrams presented in Fig. 1 A and B.

Fig. 1A presents the block schematic of the inverter. Fig. 1B depicts the simplified schematic of the PWM generator.

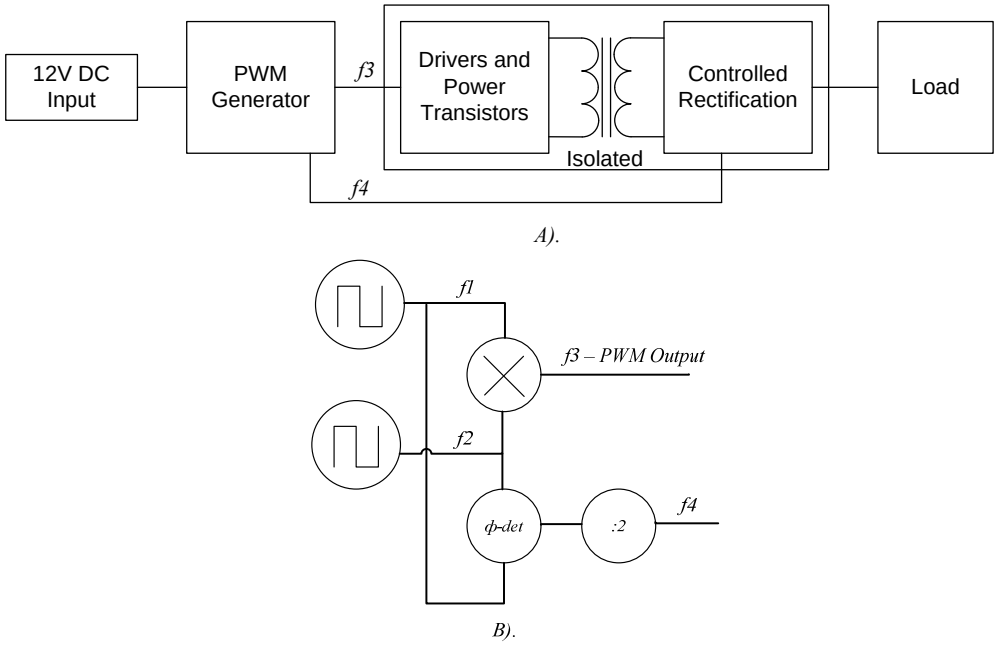

Fig.1. Block Diagram of the proposed inverter

In this diagram, two oscillators generate square wave signals which have frequencies with a difference of 50 Hz. The two signals are named f_1 and f_2 and are mixed using a multiplying mixer. The resulting signal has a fundamental frequency equal to $| f_2 - f_1 |$ and is actually a square wave with a variable duty cycle between 0% and 50%. This signal is depicted in the figure below – Fig. 2.

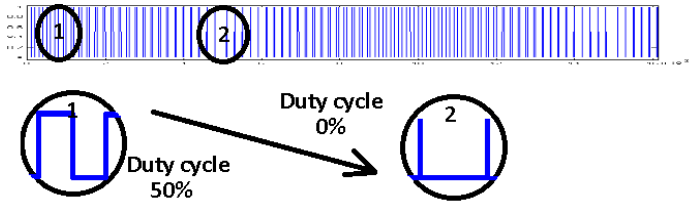

Fig. 2. PWM signal with variable duty cycle

The square wave obtained at the output of the mixer enters a Dc-Dc converter. This converter will be analyzed using the formula of the output voltage of the forward converter, working in continuous mode. The ideal output voltage of this converter is proportional with the duty cycle, according to formula 1:

$$V_{OUT} = D\frac{N_S}{N_P}V_{IN} \tag{1}$$

Formula 1. Output voltage of a Dc-Dc forward converter

In this formula, D is the Duty Cycle, N_S/N_P is the transformer turns ratio, V_{IN} is the supply voltage of the converter and V_{OUT} is the output voltage.

According to the waveform in Fig. 2, the duty cycle varies between 0 and 50%. Thus, the output of the Dc-Dc converter varies between a maximum value corresponding to $D = 0.5$ and zero, according to Formula 1.

Besides entering the mixer, those two signals are also entering a phase detector, marked in fig. 1 with "*ϕ-det*". Each time the phases of the signals cross, the phase detector changes its output from "0" to "1". This corresponds to the moment when the duty cycle of the mixed signal reaches 0 %.

The output of the phase detector enters the one-bit counter, marked in fig. 1 with "*:2*". Therefore, the output of the counter changes every time the duty cycle of the mixed signal crosses 0 %. The signal at the output of the phase detector is useful to change the sign of the output voltage.

The switch box at the output is made of power MOSFETs, which has the purpose of inverting the output voltage. When the output of the one-bit counter is "1", the power output is positive. When it is negative, the output voltage of the converter is connected in reverse, at the output, so the output voltage becomes negative.

4. Simulation at system level

The model of our proposed converter was simulated using a concept model in Matlab, followed by a circuit-level model in LTSpice.

For simulating the concept, we chose two oscillators with 4.9 kHz and 5 kHz. The difference between the two frequencies is 100 Hz. One period of the 100 Hz fundamental frequency consists of 50 periods of 5 kHz signal and 49 periods of the 4.9 kHz signal.

Matlab may process discrete-time signals. To be able to represent both signals, the sampling frequency should be a multiple of the least common multiple between 4900 Hz and 5000 Hz. In order to obtain an even number of samples per period for both signals, we will take the first even multiple. This means the sampling frequency should be 245000 Samples/s multiplied by 2, equal with 490000 Samples/s. This way, one period of the 4.9 kHz signal would have 490000 Samples/s divided by 4900 Hz = 100 samples, while one period of the 5 kHz signal would have 490000 Samples/s divided by 5 kHz = 98 samples.

The two signals from the square wave generators are defined by the following lines:

```
t=linspace(0,.02*periods,9800*periods);
f1=kron(ones(98*periods,1),y);
y =[zeros(49,1);ones(49,1)];
f2=kron(ones(100*periods,1),y);
```

By mixing f_1 and f_2 will result the function f_3, which can easily be done with an AND function, as follows:

$$f_3 = f_1 * f_2 \tag{2}$$

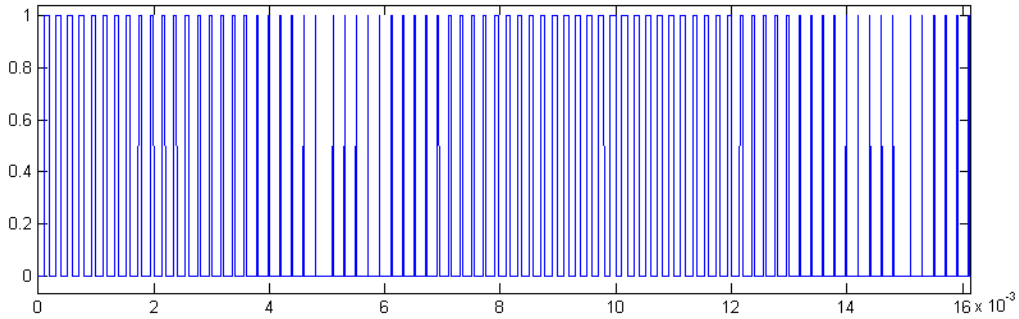

Fig. 3. f_3 waveform obtained from mixing f_1 and f_2

The new waveform is a square wave with variable duty cycle. In Fig. 3, the duty cycle starts at 50 % and drops to 0% after 5 ms. Another maximum value of 50 % is reached at 10 ms, and then drops to 0 % at 15 ms. Thus, the period at

which the duty cycle has a full variation from 0% to 50% and back to 0% is 10 ms, which gives a fundamental frequency of 100 Hz.

To transform the f_3 function into a 50 Hz zero offset waveform, two things have to be done: filtering and DC cancelling.

For cancelling the DC component, the signal has to be symmetrical. For this purpose, f_3 has to be inverted each time its duty cycle passes through zero. For this purpose, the switching function f_4 is defined below.

```
y=[-1.*ones(2450,1);ones(2450*2,1);-1.*ones(2450,1)];
f4=kron(ones(periods,1),y);
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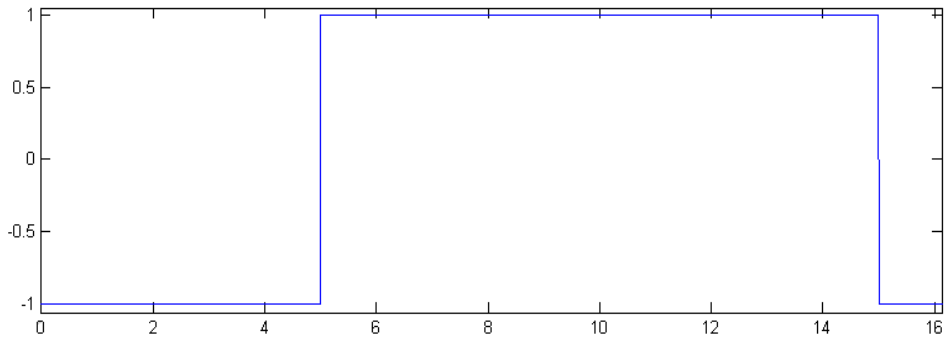

Fig. 4. Signal f_4

The synthesised signals f_3 and f_4 are multiplied together and scaled to a maximum of 310V into the function f_5.

The filtering of the higher order harmonics is done using a first order Butterworth filter, thus obtaining the function f_6. The two functions, f_5 and f_6, for one period, are depicted in Fig. 5 - *Time Domain representation of signals f_5 (PWM) and f_6 (Filtered).*

"The Butterworth low pass filter features a horizontal amplitude frequency response that changes direction abruptly at the cutoff frequency, depending on the order number. However, the square pulse response of this filter shows a considerable overshoot when compared to the Bessel filter which is as close as possible to a real RLC low-pass filter" [10]. This filter exists at the output of the inverter model, and it consists of: the load (R),the filter inductor (L) and the filter capacitor (C).

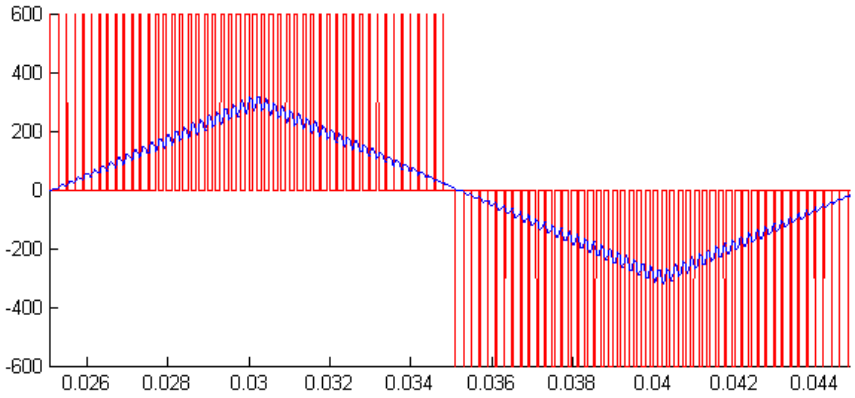

Fig. 5. Time Domain representation of signals f_5 (PWM) and f_6 (Filtered)

According to the representation of signal f_6, the resulting waveform is close to a triangular signal.

The Fig. 6 presents the comparison between the f_6 signal (obtained with the actual presented algorithm) and a pure sine wave.

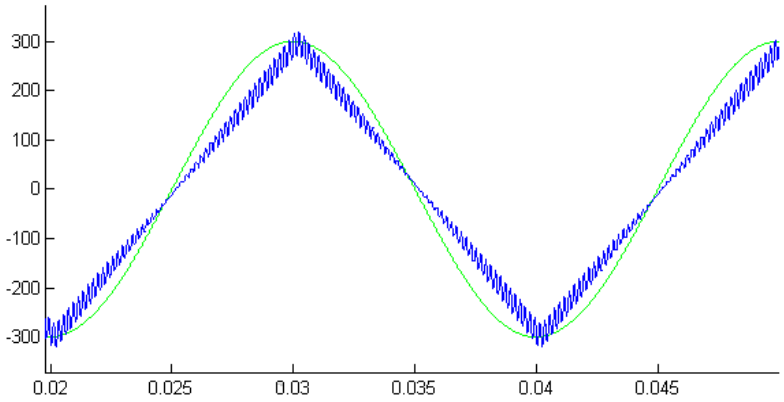

Fig. 6. Signal f_6 compared with a real sine wave

After the filtering process, the output waveform is close to a triangular signal. The amplitude of this signal follows the duty cycle of the function *f3*. There is a small high-frequency ripple resulting from the insufficient filtering of the switching signal *f3*. The ripple of *f6* is proportional with its amplitude.

f6 signal has the same sign as *f4*, and *f4* changes its sign when *f3* has a duty cycle close to zero. Therefore *f6* changes its sign at a minimum value, giving a smooth zero crossing. This way the voltage transient is much smaller than in a

square wave inverter, and therefore the EMI is greatly reduced. This change of sign also cancels the offset, making *f6* waveform symmetrical.

5. Circuit Implementation

In order to generate the two square waves corresponding to the functions f_1 and f_2, there are several methods available. Those will be presented below.

a. RC oscillators [11]. This is the simplest method, requiring a minimal number of components. The main disadvantage is the accuracy of the generated frequency. Thus, for two signals with the frequencies of 5 kHz and 4.9 kHz and a frequency accuracy of 0.01 % the resulting runaway of the output frequency would be 1 Hz, which is acceptable.

b. Frequency dividers [12]. Starting from a high frequency multiple of 100 Hz, using digital frequency dividers/counters, one may easily obtain the two frequencies needed. The mixing of these two may also be done with a digital gate. This way, the entire PWM generator could be implemented into a digital chip, such as a FPGA, a microcontroller or an ASIC. This is the simplest method among the ones presented. It is also the most immune to external EMI.

c. Phase Locked Loops (PLL) [13][14][15]. Starting from a 50 Hz square wave oscillator, using two PLLs, one can obtain the two frequencies which need to be mixed. This mixed signal method is the most complex one. It needs a large area on the PCB or the silicon die to be implemented.

A working schematic for the concept is depicted in the Fig. 7. The square wave generators are V1 and V2. There are three main parts of the schematic: the signal generator (represented by V3 – 12V dc, and V1, V2 which are the two signals with a 100 Hz difference), Flyback converter (represented by M1 switching transistor and output isolated transformer – L1, L2 and L3) and output active rectification (using M2-D1 and M3-D2).

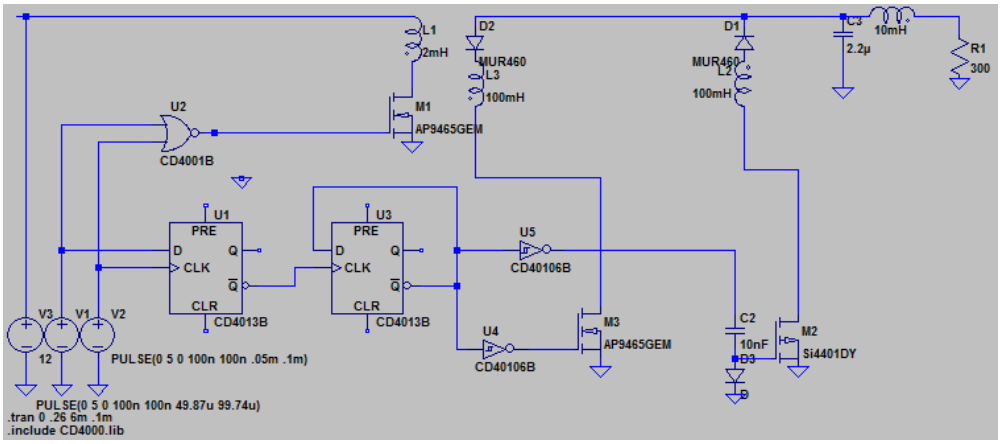

Fig. 7. Schematic used in the LTSpice electrical simulation

The signals generated using one of the three methods above are mixed using a CMOS NOR gate type CD4001B, which is named U2. The signal obtained this way is applied to the primary winding of the flyback converter transformer. When the duty cycle of the mixed square wave reaches 50 %, the peak current is at its maximum. When it reaches 0, the current drops to 0 and no power is transferred through the converter.

In order to use low $R_{DS,ON}$ transistors, the output voltage was limited to 40V peak to peak. In a real case, higher voltages are obtained by modifying the turns ratio of the transformer. The load is simulated using a 300 ohm resistor.

The output waveform, according to the simulation, is shown in the following picture.

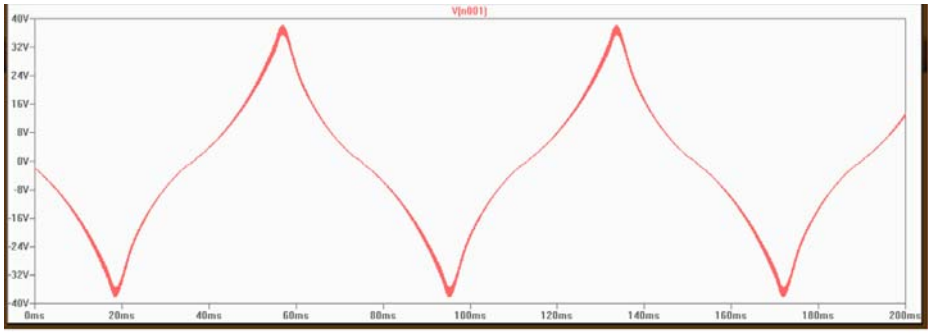

Fig. 8. Output waveform of the inverter

The above image presents the output waveform of the inverter. The signal is symmetrical, so the DC offset is equal to zero. The fundamental frequency of the resulting signal is 50 Hz. There are some high-frequency, low amplitude oscillations when the output voltage is close to a maximum value. These oscillations appear due to weak filtering of the switching harmonics.

In order to show the harmonic distortion of the signal above, a Fast Fourier Transform (FFT) was applied to the signal. The result is depicted in Fig. 9.

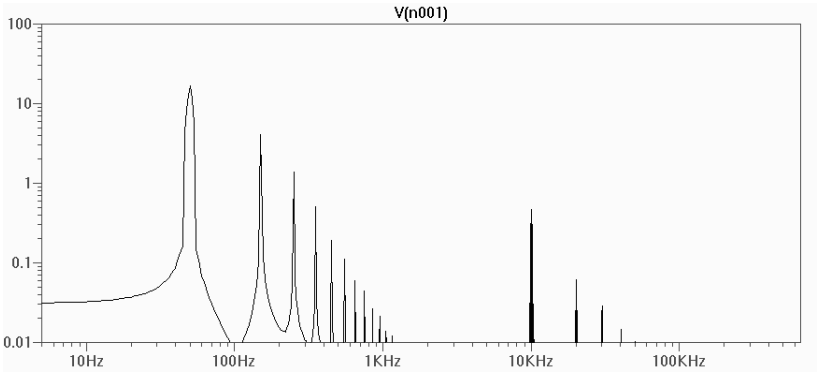

Fig. 9. FFT of the output waveform of the inverter

The fundamental frequency has a RMS value of 16V. The even harmonics are missing. The odd harmonics which have the amplitude larger than 100mV are emphasized in the following table.

Frequency (Hz)	50	150	250	350	450	10kHz
Amplitude (V)	16	3.3	1.28	0.41	0.150	0.221

The FFT of the output of a square wave inverter is depicted in Fig. 10. The level of the harmonics is higher than the one described in this paper. Also, the harmonics have a higher dispersion in frequency.

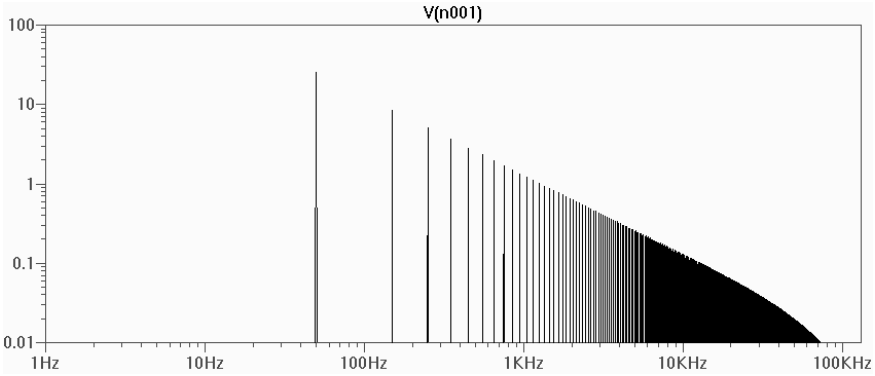

Fig. 10. FFT of the output waveform of a square wave inverter

6. Conclusions

The operation of the novel circuit was validated both by simulation using Matlab and experimental model using Spice electrical. The circuit presents a good compromise between circuit complexity and EMI level.

The main advantages of the model are listed below:

1. Low component count. The PWM generator can be synthesized as a digital block on an ASIC of FPGA.
2. Low component cost. The inverter does not contain a large iron core transformer, like a sine wave inverter does. Instead, it uses a much smaller, high-frequency ferrite core transformer.
3. Low EMI. Due to the nature of the output waveform, the harmonic oscillations and, therefore, the EMI emissions are reduced compared to a classic square wave inverter.

The main practical issues are:

1. Keeping a constant frequency difference between the two square wave signals. Suppose that the frequency the two oscillators is 20 kHz and 20.1 kHz. The frequency difference is 100 Hz, and should be kept within the range of

+/-10 %. This means that the relative tolerance of the oscillators should not exceed 100 ppm.

2. When the duty cycle becomes close to zero, very short PWM pulses appear. This leads to a drop in efficiency due to increasing switching losses. Those pulses may be filtered using simple digital filters.

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