DESIGN OF A SIGMA-DELTA MODULATOR WITH 14-BIT RESOLUTION FOR BIOMEDICAL APPLICATIONS

Mahdi REZVANYVARDOM [1*], Vahid KHALILI SADAGHIANI [2], Amin MIRZAEI [3]

This paper investigates a new second order, 14-bit resolution, 800nW power consumption sigma-delta modulator which is suitable for biomedical applications. The proposed modulator is designed in the sub-threshold region and used 0.18um TSMC CMOS technology. In this paper, the maximum value of saturation is achieved by using of the coefficients of second order modulator which is approximately 5-DBFS. Moreover, the CDS technique is used to eliminate the flicker noise. Also, the Nyquist-rate, the sampling frequency and the maximum SNDR of the proposed modulator are 100Hz, 12.8 KHz and 86dB, respectively. The proposed structure improves bandwidth frequency, oversampling frequency and time resolution of the sigma-delta modulator.

Keywords: Sigma-delta modulation, CDS technique, Comparator, Switched capacitor circuits, Analog-to-digital converter, Common mode feedback

1. Introduction

Nowadays, time-to-digital converters (TDCs) and analog-to-digital converters (ADCs) [1-6] are the main building blocks in the design of digital signal processing circuits which have developed CMOS integrated circuits (ICs) technology for digitizing the input signals [7-9]. It is necessary to measure the medical signals by the portable electronic devices. Therefore, ADCs would be improved and more reliable. In the new CMOS technology, portable or implantable medical devices can determine the features of the biomedical signals such as electrocardiograph (ECG) and electroencephalogram (EEG) signals [10-13]. Because of fundamental limitations of power consumption in the biomedical systems, the power consumption rate in the input and output stages must be decreased by an ADC which has optimized its power consumption [14, 15]. ADCs are classified into two main groups: Nyquist-rate and oversampling ADCs. In the Nyquist-rate converter, an input analog signal is sampled at the Nyquist-rate such

[1] * Department of Electrical Engineering, Faculty of Engineering, Arak University, Arak, Iran, e-mail: m-rezvanyvardom@araku.ac.ir
[2] Islamic Azad University, Arak Branch, Arak, Iran, e-mail: vkhalili93@iau-arak.ac.ir
[3] Department of Electrical Engineering, Faculty of Engineering, Arak University, Arak, Iran, e-mail: a-mirzaee@araku.ac.ir

as pipeline, flash, folded, interpolating and SAR structures. These converters are designed for high-speed and low-accuracy applications. The design of these converters for high-accuracy applications is not easy due to non-ideal parameters of an analog circuit. In the oversampling converter, the sampling rate is equal to some multiple of the Nyquist-rate. These converters use the quantization noise shaping technique which generates a high-precision conversion [14, 15]. The Nyquist-rate converters are more sensitive to the non-ideal parameters than the oversampling converters. For example, a high-precision 18-bit ADC can be built by using a single-bit comparator. A sigma-delta converter is composed of two distinct parts. The first part is a sigma-delta modulator which is analogously implemented. The second part contains the decimation filters, which are digitally implemented [16-18]. In Section 5, a perfect comparison of the characteristics of the similar converters with the proposed converter is presented.

This paper proposes a new second order 14-bit resolution, 800nW power consumption delta-sigma modulator. The proposed modulator improves the bandwidth frequency, oversampling frequency and resolution to 50 Hz, 12.8 KHz and 14 bits, respectively in 0.18 um TSMC CMOS technology while the supply voltage is 1 V. A system-level design for the optimized modulator is investigated in section 2. In the third section, the analysis of noise in the proposed circuit is described. Section 4 investigates a circuit-level design for the proposed modulator. The description of the simulation results is introduced in the fifth section and conclusions drawn from this paper are presented in the last section.

2. System-level Design

This section studies a system-level design for the proposed structure. It includes the design of a modulator and a suitable gain amplifier.

2.1. Modulator design

Delta-Sigma modulators (DSMs) are suitable for the analog-to-digital interface system which is a class of oversampling ADCs. It performs quantization noise shaping. As a result, the signal to noise ratio (SNR) of DSMs is high by using oversampling and noise shaping techniques [19-22]. Fig. 1 shows a conventional block diagram of a second order sigma-delta modulator which is used for biomedical applications [10]. According to the coefficients of the system shown in Fig. 1, this structure can provide the maximum SNDR 81 dB for biomedical applications. The main features of a conventional ADC, which is suitable for biomedical applications are summarized in Table 1 [10]. In order to optimize the coefficients, SCHREIER toolbox functions are applied and the mentioned structure is simulated again [23]. Consequently, SCHREIER toolbox provides the better coefficients for conversion and the maximum rate of SNDR is improved to 86 dB as shown in Fig. 2. Unfortunately, in the optimized structure,

there are many differences between the inputs of integrators. Hence, a circuit-level implementation is difficult. In fact, it is difficult to provide a capacitor that its capacitance value is 10 times greater than others. Subsequently, the block diagram of the modified system is shown in Fig.3.

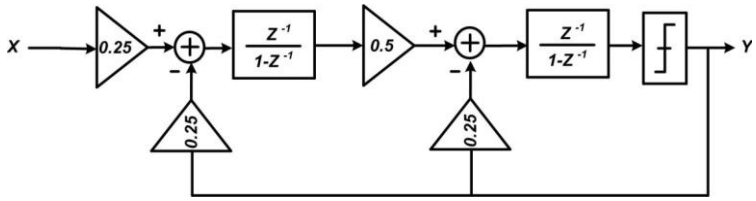


Fig. 1- The conventional second order modulator [10]

Table 1

The main features of a conventional ADC in the medical applications

Input voltage range	2 V differential
Resolution	10 bits
Supply voltage	1.2 V
Power consumption	Less than 200 nW
Nyquist frequency	50 Hz

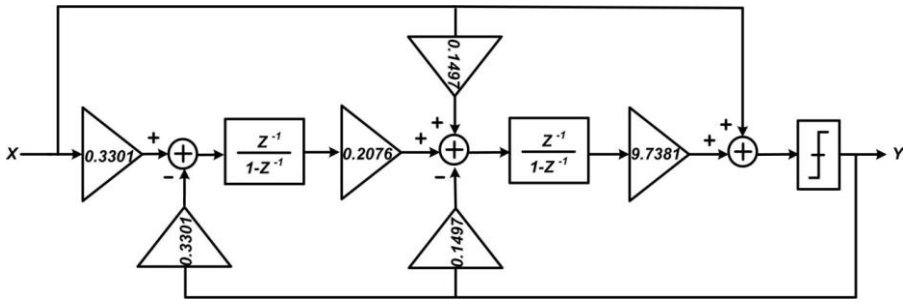


Fig. 2- The optimized second order modulator.

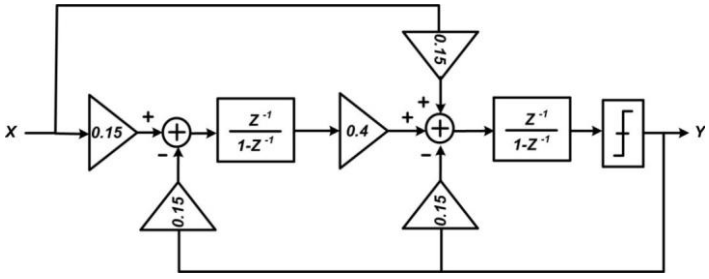


Fig.3- The modified second order modulator.

As shown in Fig. 3, by changing some parameters such as removing the feed-forward path and providing the optimal and well-rounded coefficients, the structure can provide 86 dB SNDR approximately. The dynamic range (DR) of

the SD modulator is calculated by the ratio between the input signal power to the noise power.

$$DR_{input} = 10\log_{10}\frac{P_{sig}}{P_{thermal} + P_{flicker}} \quad (1)$$

where, P_{sig} is the input signal power. Similarly, $P_{thermal}$ and $P_{flicker}$ are the thermal noise and the flicker noise power of the proposed modulator, correspondingly [12]. The dynamic range curve of the improved structure is illustrated in Fig. 4. In section 4, a circuit-level implementation of the improved system is described.

2.2. Amplifier gain

When the gain of amplifier increases more than a specific amount, the operation of the modulator is proper. According to Fig. 5, by simulating the system in MATLAB, the minimum required gain for the amplifier is computed. Moreover, the minimum value of the amplifier gain is 25 dB as displayed in Fig. 5.

3. Noise analysis using CDS technique

Flicker noise is a colored-noise source which has high amplitude in the low frequency domain. Correlated Dual Sampling (CDS) technique is used to remove the noise. Fig. 6(a) shows an equivalent switching circuit that can remove the flicker noise. As well, the equivalent switching circuit in phase 2 is depicted in Fig. 6(b). As can be seen in Fig. 6(a), in phase 1 (ø1), the voltage of flicker noise is saved in C_{CDS} that is added to the input signal in phase 2 (ø2). Therefore, in this operation mode (ø2), flicker noise is removed. Thermal noise is determined by internal capacitors with excellent approximation properties. The differential noise is calculated as follows [24]:

$$\bar{V}_n = \frac{4KT}{C_{S1}} \quad (2)$$

Thermal noise has great importance within the first stage of the modulator. Since, this form of noise along with other forms of noise limits the sensitivity of the circuit. This noise is transmitted to the output as a signal. Thermal noise of the second stage is spectrally shaped by a second order noise-shaping function. As a result, it is decreased as well as the output of the second stage. In the proposed modulator, thermal noise is equal to the quantization noise. According to -5dBFS and SNDR=83 dB, the output power of the modulator is calculated as:

$$SNR = 10\log_{10}(\frac{P_{sig}}{P_n}) \quad (3)$$

where, P_{sig} and P_n are the power of the output signal and noise, respectively. Thus, the SNR is equal to 83dB.With regards to (2), the value of the sampling capacitor C_{S1} is equal to 5.33 pF. Note, that the value of internal capacitor has been computed by the rate of oversampling. The following equation is expressed for the oversampling rate.

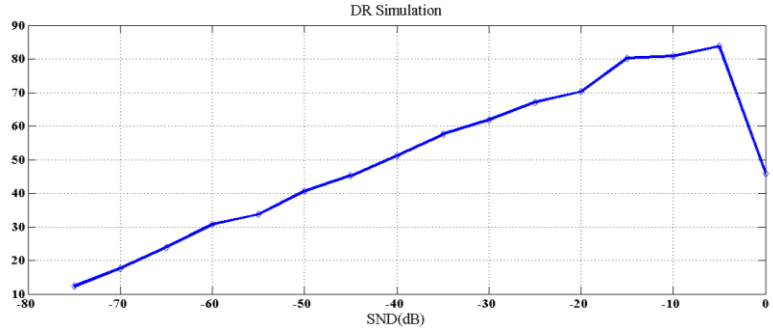


Fig. 4- The dynamic range curve of the optimized structure.

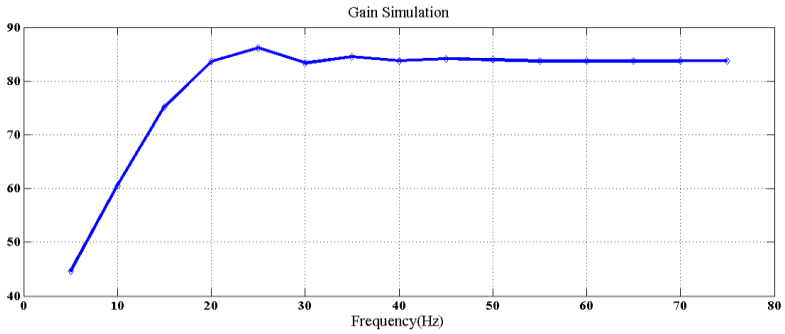


Fig. 5- The graph of simulated SNDR according to the amplifier gain.

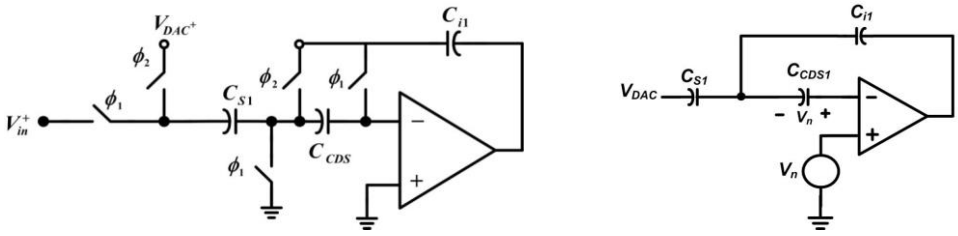


Fig. 6- (a) An equivalent switching circuit for removing the flicker noise and (b) equivalent circuit in ø2.

$$OSR = \frac{f_s}{2 f_{sig}} \tag{4}$$

where, f_s and f_{sig} are sampling and signal frequency, correspondingly. Therefore, the oversampling rate (OSR) is equal to 128. According to the value

obtained for OSR, 41.6 fF is achieved for the sampling capacitor which is similar to the value of parasitic capacitors. For that reason, it is selected to be 200 fF.

4. Circuit-level design of the modulator

In this section, the circuit parameters of the proposed modulator are explained. Furthermore, a circuit-level design for the proposed modulator is performed.

4.1. Switch capacitor circuit design

The structure of the switch capacitor circuit is illustrated in Fig. 7. Also, the clock frequency is 12.8 KHz which is equal to twice the oversampling rate of the signal. As can be seen in Fig. 7, this circuit is operating in two *different* phases, ø1 and ø2. Sampling and integrating of the input signal are carried out in ø1 and ø2, respectively. According to the value of capacitor calculated by (2) and the coefficients of the system, the value of integrating capacitor C_{i1} is calculated as:

$$H(Z) = \frac{C_{S1}}{C_{I1}} \cdot \frac{Z^{-1}}{1 - Z^{-1}} \tag{5}$$

Table 2 indicates the values of integrating capacitors that are used in Fig. 7.

Table 2

The value of the integrating capacitors in the proposed SC structure.

Capacitor name	Value
C_{S1}	210 fF
C_{i1}	1400 fF
C_{S2}	560 fF
C_{S3}	210 fF
C_{i2}	1400 fF

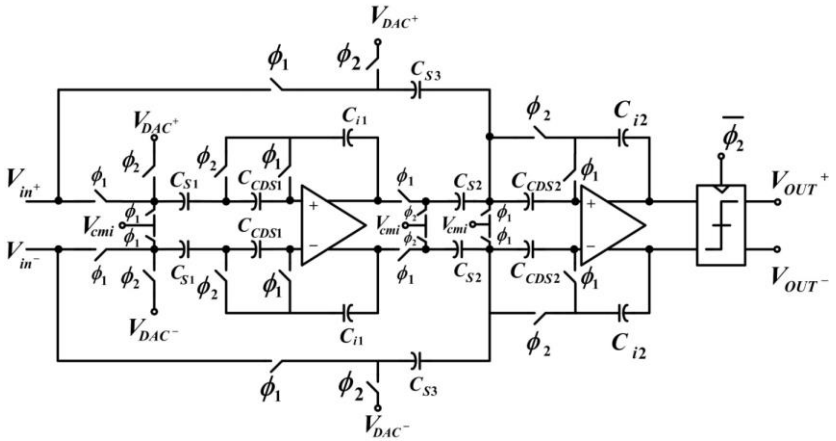


Fig. 7- The proposed switch capacitor structure.

4.2. Switch capacitor circuit design

For the proposed modulator, a single-stage amplifier is suitable. No compensation is needed due it is carried out by the load capacitor. For a single-stage amplifier with a trans-conductance (g_m) and load capacitor (C_L), the following gain-bandwidth is achieved:

$$GBW = \frac{g_m}{C_L} \tag{6}$$

In this amplifier, the minimum value of trans-conductance is 400 nano-siemens that is adequate regarding to the rate of unit gain-bandwidth (UGBW). The applied amplifier is a folded-cascade amplifier that is presented in Fig. 8.

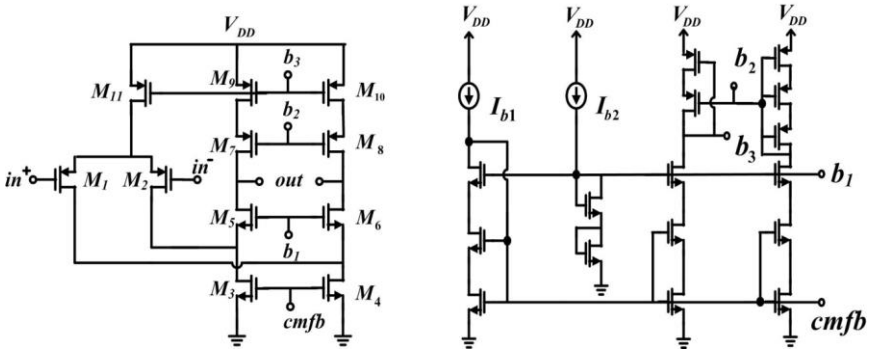


Fig. 8- The applied folded-cascade amplifier with its bias circuit.

As can be seen in Fig. 8, in the bias circuit, a series of transistors are applied which have provided a bias voltage supply for the amplifier.

Fig. 9 shows the circuit of the switch capacitor which is used in the proposed amplifier. This circuit is a common mode feedback structure.

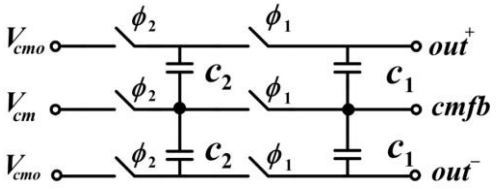
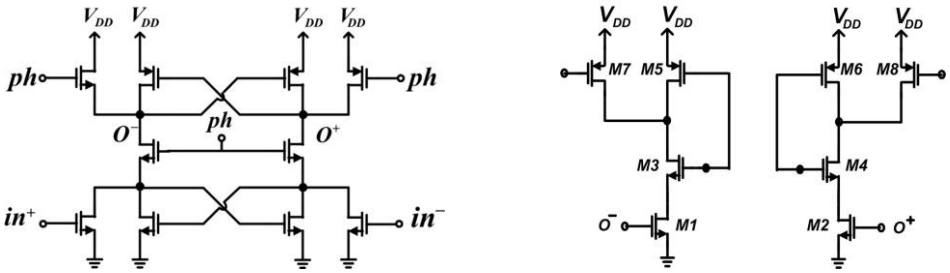


Fig. 9- The common mode feedback structure

This circuit is designed in the sub-threshold region leading to drive currents in the scale of nano-amperes and to reduce the power consumption. Comparators are the main building block in the MDS structures which are proposed to reduce the power consumption and improve the speed [24]. Fig. 10(a) shows the circuit of a comparator that is usually used on the second stage of an integrator. To keep the current states and results, a D-Flip Flap (DFF) is used which is displayed in Fig. 10(b) :



(a) (b)

Fig. 10- (a) The applied comparator circuit, (b) The applied D-Flip Flap circuit.

5. Simulation results

The proposed circuit is designed in the sub-threshold region and uses 0.18 um TSMC CMOS technology. The layout prototype of the proposed circuit is shown in Fig. 11, where the active area is 525µm × 210 µm.

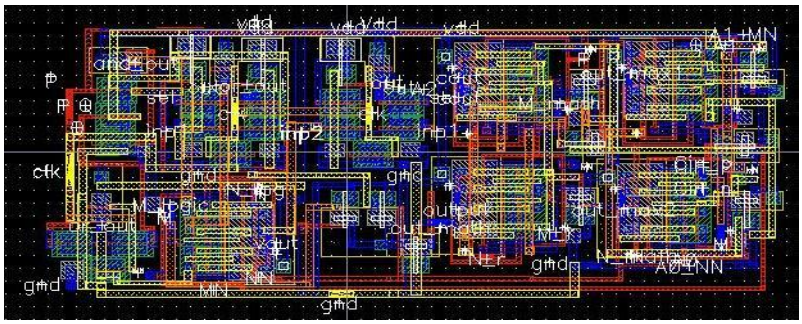


Fig. 11- The layout prototype of the proposed circuit.

The post-layout simulation results are presented in this section. Also, the proposed modulator is simulated in different corners of CMOS technologies and its output waveforms are demonstrated in Fig.12, Fig. 13 and Fig. 14, accordingly.

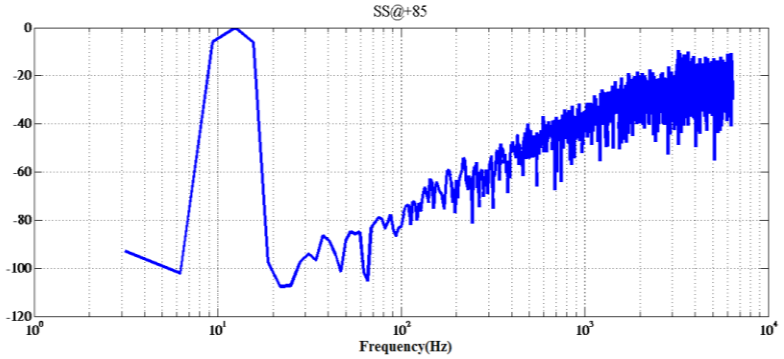


Fig. 12- The spectrum of output signal of the proposed modulator in SS@85

The sampling frequency is 12.8 KHz. In the proposed structure, the SCHREIER toolbox functions are applied to optimize the coefficients of the system. A sinusoidal signal with a frequency of 12.5 Hz and amplitude of 500 mV is used as the input signal.

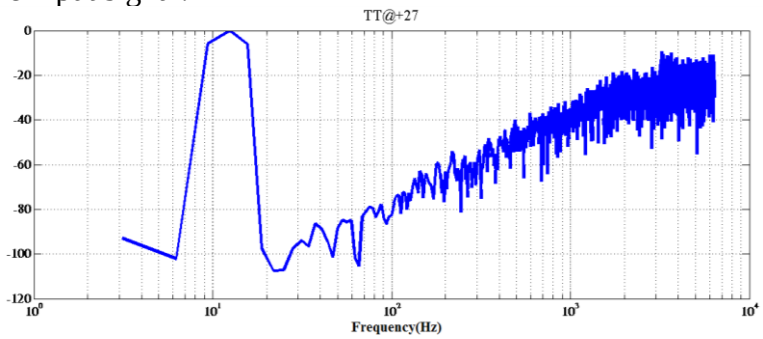


Fig. 13- The spectrum of output signal of the proposed modulator in TT@+27

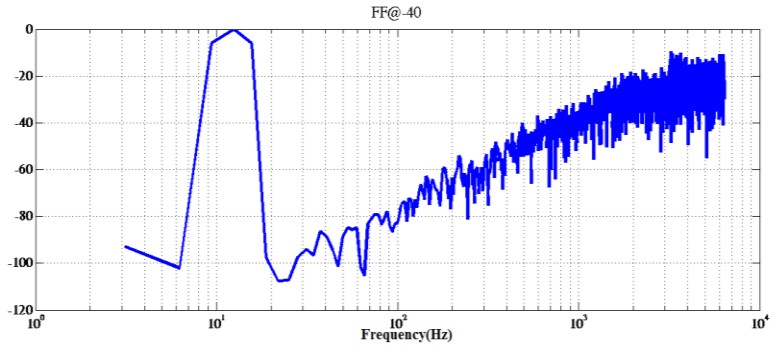


Fig. 14- The spectrum of output signal of the proposed modulator in FF@-40

The proposed structure is simulated in Hspice software. Then, the production output of the proposed modulator is transferred to MATLAB software. Besides, a Hann-window is used for the spectral-analysis of the output signal. By applying window functions, the ability of Fast Fourier Transform (FFT) to extract spectral data from the output signal is used. These simple functions improve the sensitivity of FFT spectral-analysis techniques. The dynamic range of the post-layout simulated modulator versus SNR (dB) is shown in Fig. 15.

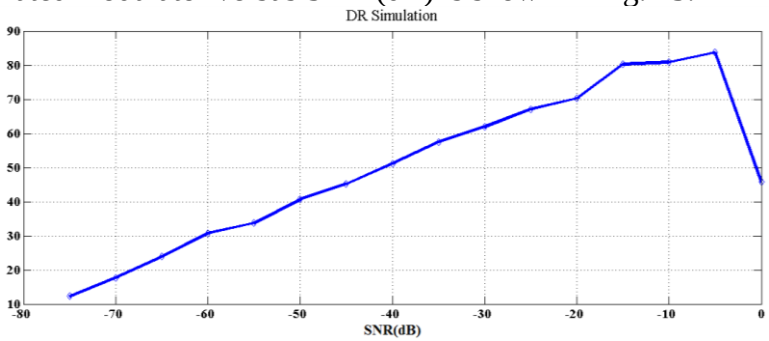


Fig. 15- The dynamic range of the post-layout simulated modulator.

The dynamic range of the proposed modulator is 86 dB as depicted in Fig. 15. Furthermore, a Monte Carlo simulation which displays the mismatch effect of the comparator offset is shown in Fig. 16.

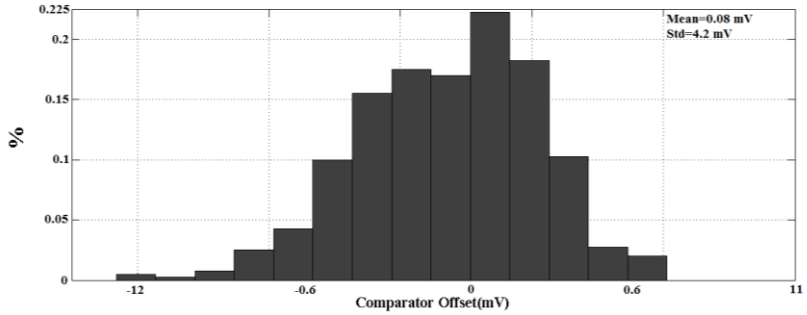


Fig. 16- Monte Carlo histograms for mismatch simulation of the comparator offset (Runs=500 and σ=4.2 mV).

The measured power consumption and Figure of Merit (FoM) are 800 nW and 0.64pj/con, respectively which are suitable for biomedical applications. The FoM is achieved by the following equation:

$$FoM = \frac{Power}{BW \times 2^{N+1}} \tag{7}$$

where N is the number of effective bits. The performance of the delta-sigma modulator is summarized in Table 3 and compared with other suggested high-resolution modulators which are applied in biomedical applications.

Table 3.

Comparison of modulator characteristics between this work and other recent articles

References	Year	ENOB	B.W.(Hz)	Power	Supply	Process	FoM
Ref [10]	2008	10.7	25	0.14 μw	1.2 v	0.5μm	1.6 *pj*/con
Ref [11]	2007	14	5 E+5	38 mw	1.8 v	0.18μm	2.3 *pj*/con
Ref [12]	2010	7.7	250	816 n	0.8	0.18	7.84 *pj*/con
Ref [13]	2005	8	2.6 E+3	1.8 μw	1.8 v	0.5μm	0.13 *pj*/con
Ref [14]	2005	10	1.6 E+5	75 μw	3 v	0.35μm	2.3 *pj*/con
Ref [15]	2011	11.1	1 E+4	60 μw	0.9 v	0.18μm	1.13 *pj*/con
Ref [16]	2011	9.8	1E+4	7.5 μw	0.25 v	0.13μm	42 *pj*/con
Ref [17]	2013	7.2	0.25E+1	540μw	0.6 v	0.18μm	7.43 *pj*/con
This Work	2017	13.5	50	1μw	1 v	0.18μm	0.64 *pj*/con

According to Table 3, the proposed modulator improves the power consumption. As well, a high accuracy is reached with a well-defined design process while the supply voltage is less than the standard supply voltage in this CMOS technology. The power consumption of the modulator is improved if the value of the capacitor is reduced, which is applicable to the newer CMOS technologies. Consequently, FoM can be improved by using the newer generations of CMOS technologies.

6. Conclusion

In this paper, a second order delta-sigma modulator for biomedical applications with 128 KHz rate of oversampling rate and 14-bit of resolution is designed and simulated in Hspice software. The proposed modulator uses a gain amplifier as same as other modulators applied in low-speed applications. The measured power consumption of the proposed sigma-delta modulator is 800 nW. In this study, the CDS technique is applied to remove the flicker noise. Also, the SCHREIER toolbox functions are used to optimize the coefficients of the system. The Nyquist-rate, the sampling frequency and the maximum SNDR of the proposed modulator are 100 Hz, 12.8 KHz and 86dB, respectively. Also, FoM of the circuit is improved to 0.64 pj/con. Therefore, the proposed modulator is suitable for biomedical applications. The theoretical and simulation results confirm the merits of this modulator operation.

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