VOLTAGE SAG MITIGATION USING MULTILEVEL INVERTER AS A DYNAMIC VOLTAGE RESTORER

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Voltage sag is the most frequently encountered power quality issue in the power distribution network. Dip in terminal voltage affects the performance of all the equipment's connected. Therefore, it is necessary to compensate for the voltage dip. A Dynamic Voltage Restorer (DVR) based on Cascaded H-Bridge Multilevel Inverter (CHBMLI) of 11 levels is proposed in the paper with suitable control technique to compensate voltage sag due to non-linear loads. Many pieces of equipment are controlled using power converters which account for non-linear loads. Since power converter-based control is becoming popular, the non-linearities are proportionately getting added to the distribution network. The simulation results and experimental validation of the proposed configuration are presented in this paper.

Keywords: Power Quality; Voltage Sag; Cascaded H-Bridge Multilevel Inverter; Dynamic Voltage Restorer, Total Harmonic Distortion

1. Introduction

In most recent times, power converters are widely used for many industrial applications as well as in power supplies because of efficiency and ease of control over wide range. The power electronic devices in the system introduce harmonics and non-linearities. There are many power quality issues. Few issues which are quite common are such as voltage sag/swell, under frequency and flickering etc. [1-2]. Power converters are also used to integrate the distributed generator into the grid. Inverters are used to inject solar power to the grid. If the inverter switching frequency is not adjusted properly, it leads to major power quality issues [3]. The load is unpredictable and the increase/ decrease in load introduces voltage sag/swell in the supply. It is always desired to maintain the terminal voltage at load constant for proper functioning of the equipment's. Otherwise, the lifetime of the equipment will be dramatically reduced [4-5]. Therefore, voltage sag/swell should be taken care of.

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There are many techniques proposed by researchers to address power quality issues in distribution networks, microgrids and hybrid AC/DC grids of low and medium voltages [7-9]. The causes of power quality issues in maritime microgrid and the urgency for addressing those problems were discussed in detail in [10].

There are many solid-state controllers which are used. Static Synchronous Compensators (STATCOMs), unified power flow controllers and dynamic voltage restorers and are the Flexible AC Transmission controllers which are very widely used to handle power quality issues in transmission and distribution networks [11-14]. A DVR is a series compensator connected in series with the distribution network though a coupling transformer. DVRs are very effective for voltage compensation [15-16]. Therefore, the further studies are focused on DVR as a voltage compensating device, because the work focuses on voltage sag mitigation. DVR acts as a series filter. To ensure that the load terminal voltage is constant, series compensators will inject the voltage of required magnitude at power frequency. The DVR mainly integrates an additional source with the existing supply with the help of a power converter [17]. A CHBMLI based power quality compensator was proposed to take care of power quality issues in railway power systems [18] because multilevel inverter-based DVR are the best choice for high voltage applications since they generate almost a nearly sinusoidal output. Multilevel inverters are non-isolated inverters and CHBMLI inverters do not require dynamic voltage balancing. Therefore, CHBMLI is considered. Compared to other multilevel inverter configurations, such as diode clamped and flying capacitors, In CHBMLI the same number of levels can be generated using lesser number of switches compared to other topologies to get the same voltage levels. [18-21]. This makes the CHBMLI an appropriate choice for DVR [22-24].

Five level and seven level CHBMLI were used in DVR configurations proposed in the literatures [25-27]. The inverter was controlled using PQ theory. Enhancing the number of levels in inverter output will reduce harmonics in the voltage and try to generate a smooth sinusoidal voltage which can be injected to the grid to solve voltage sag issues. Therefore 11 levels CHBMLI with a smaller number of switches is used as a DVR.

DVRs are very effective for voltage compensation. This paper aims at addressing voltage sag issues due to the presence of non-linear loads. An RL load whose voltage and currents are controlled using controlled rectifier is considered as a non-linear load. Addition of this load leads to voltage sag. To compensate for a dip in voltage, a CHBMLI based DVR is proposed in the paper. The number of levels in CHBMLI can be adjusted with proper switching. Here, 11 levels are considered. CHBMLI do not require dynamic voltage balancing which is why there are considered in this work. The proposed configuration will compensate for the voltage dip very quickly and is synchronized with the supply by means of a phase locked loop. The simulation results are experimentally validated. The CHBMLI based DVR was proposed in [28] and the simulation results were presented. This paper is an extension of the work in [28]. The configuration is experimentally validated in this paper.

In this paper, the DVR configuration, CHBMLI and control strategy are discussed in section II. Simulation is carried out in Matlab Simulink and the results are presented in Section III. The simulation results are experimentally validated and the same is presented in Section IV. The work is concluded in section V.

2. Proposed DVR Configuration

Voltage sag is considered to be a severe problem which can damage the equipment. Such problems are dealt with using custom power devices like DVR which is a series compensator. The proposed CHBMLI based DVR configuration is shown on Fig. 1.

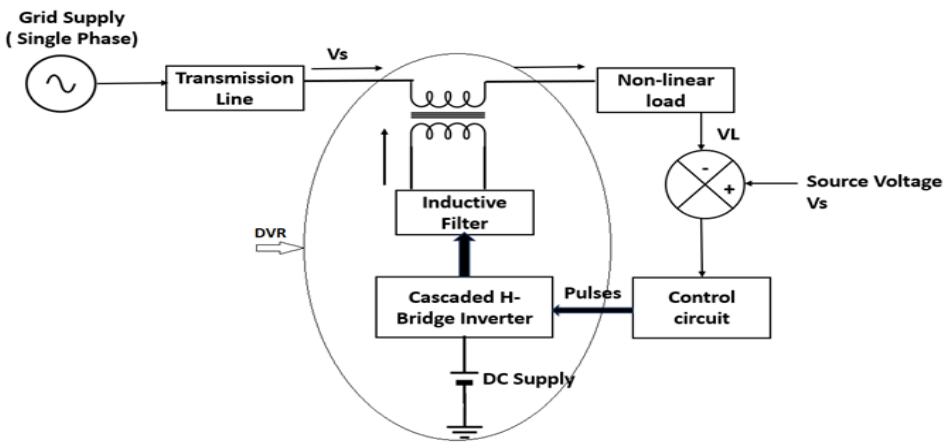

Fig 1. Proposed CHBMLI based DVR Configuration

The DVR consists of a voltage source inverter. DC supply given to the inverter is from battery. Instead of battery, the power from photovoltaic panels can also be used. The inverter output is given to harmonic filter. There is a DC charging circuit, control and protection system. A coupling/injection transformer is connected to the filter end. In the proposed configuration an 11 level CHBMLI is used. The CHB topology is as shown in Fig. 2. This multilevel inverter uses dc sources and switches which are connected like a cross. The relation between the number of levels and the DC supply for CHBMLI topology [24] is given in (1) & (2).

$$\mathbf{N_L = 2N_{DC} + 1} \quad (1)$$

$$\mathbf{N_S = 2(N_{DC} + 1)} \quad (2)$$

Where,

$\mathbf{N_L}$ = Number of levels
$\mathbf{N_S}$ = Number of switches and
$\mathbf{N_{DC}}$ = Number of DC voltage sources

From (1) and (2), the relation between $\mathbf{N_L}$ and $\mathbf{N_S}$is given in (3)

$$\mathbf{N_S = N_L + 1} \tag{3}$$

The number of power devices used for obtaining the desired number of voltage levels is considerably reduced from the basic CHBMLI configuration [23-25]. The switching pulses for the inverter obtained using sinusoidal pulse width modulation.

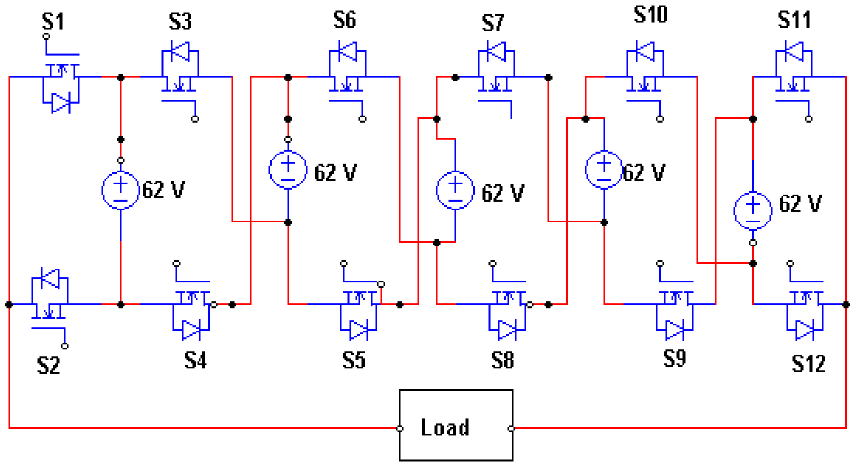

Fig 2. Single phase 11 levels modified CHB Multilevel Inverter

The switching pattern for the multilevel inverter switches to obtain the desired output voltage with a step of 62 volts is given in Table1. From Table 1, it is observed that the switching transition from one level to the next is one. Therefore switching losses will be less.

Table 1

Switching Pattern for the 11 Levels Chemli

Switching Combination	Voltage Level
S2, S4, S6, S8, S10, S12	0
S1, S3, S6, S8, S10, S12	62
S2, S3, S6, S8, S10, S12	124
S2, S3, S6, S7, S9, S11	186
S2, S3, S6, S7, S10, S11	310

A unique and simple compensation algorithm shown in Fig. 3 is developed to compensate for voltage sag. The source voltage and the load voltage peak amplitudes are continuously monitored and compared. When there is no voltage sag, the comparator output will be zero, hence the gating pulses for the inverter switches are not released. When there is a sag in supply voltage, the comparator output goes high; this will energize the relay coil, which in turn will release the pulses to inverter switches. The CHBMLI provides the required compensation. Zero crossing detector is used to ensure in phase synchronization of inverter voltage with supply.

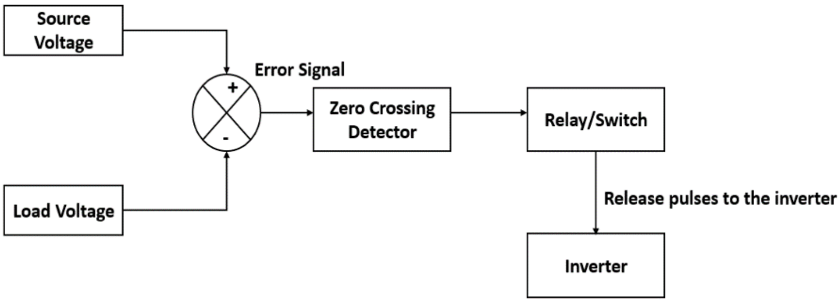

Fig 3. Block diagram representation of control strategy

3. Simulation Results and Analysis

The simulation is carried out in Matlab/Simulink platform for a single-phase system where the voltage compensation is provided by a single phase 11 level CHBMLI. The specifications are given in Table 2.

Table 2

Specifications of Power Circuit

Parameter	Value
Supply voltage	325V
Line inductance	0.5mH
Line resistance	0.1Ω
Load inductance	200mH
Load resistance	100Ω
Load capacitance	1.56μH

The simulation model is shown in Fig. 4. The supply voltage of 230 V is shown in Fig. 5. When an additional inductive load is connected for about 0.04 sec. there will be reduction in load voltage from 0.02 sec. to 0.06 sec. which is shown in Fig. 6. To inject the required additional voltage during sag, an additional DC storage battery is used. This DC voltage is inverted to an AC voltage of 50 Hz using CHBMLI of 11 levels. The CHBMLI configuration is shown in Fig. 2. The inverter output voltage is shown in Fig. 7.

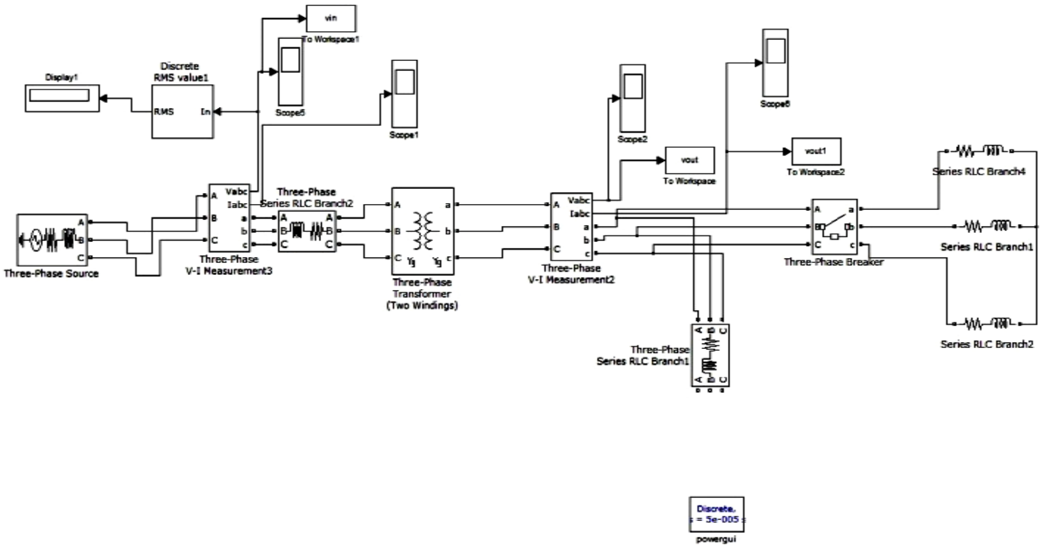

Fig 4. Simulation Circuit

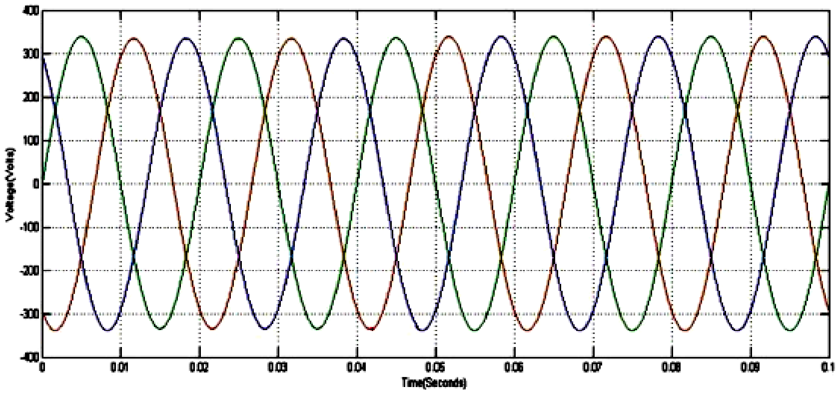

Fig 5. Supply Voltage

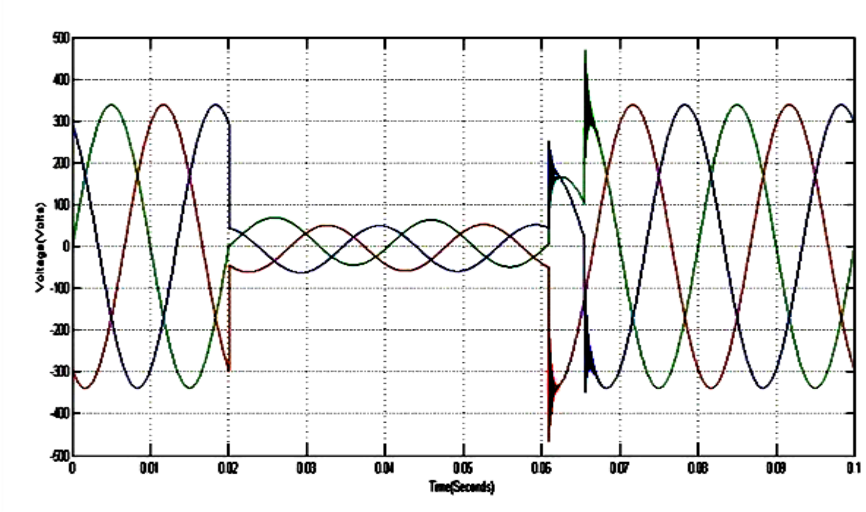

Fig 6. Load voltage

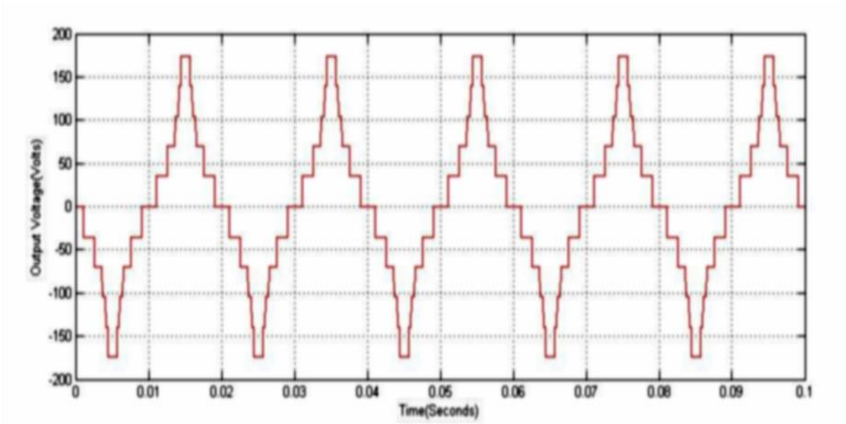

Fig 7. CHBMLI output voltage

The control scheme used for mitigating voltage sag is shown in Fig. 8. The load voltage after compensation using DVR shown in Fig. 9. From Fig. 9, it is observed that during the increase is load demand, the additional requirement is met from DVR. Hence, the voltage sag problem has been taken care of.

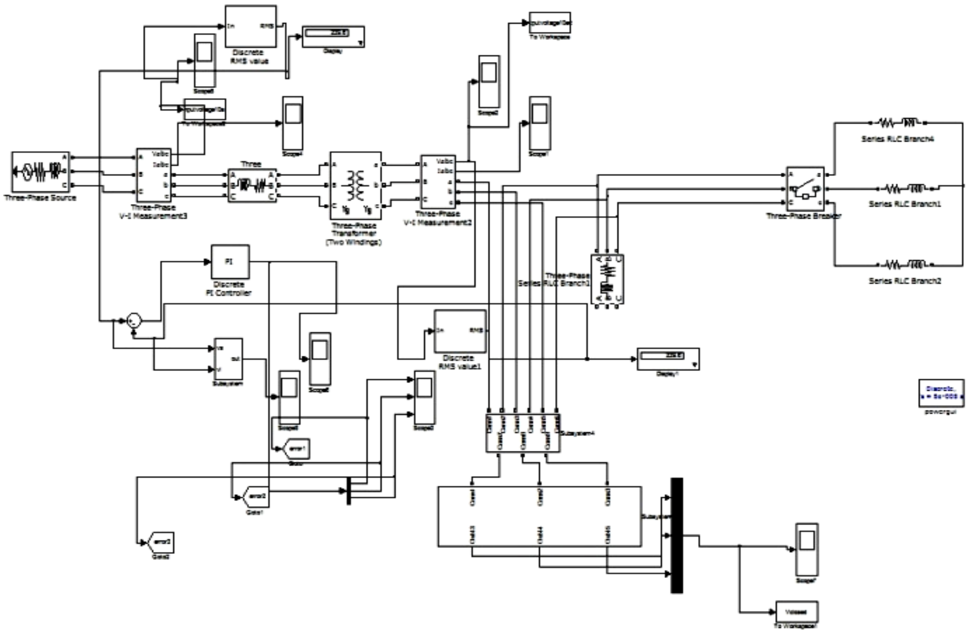

Fig 8. Control Circuit

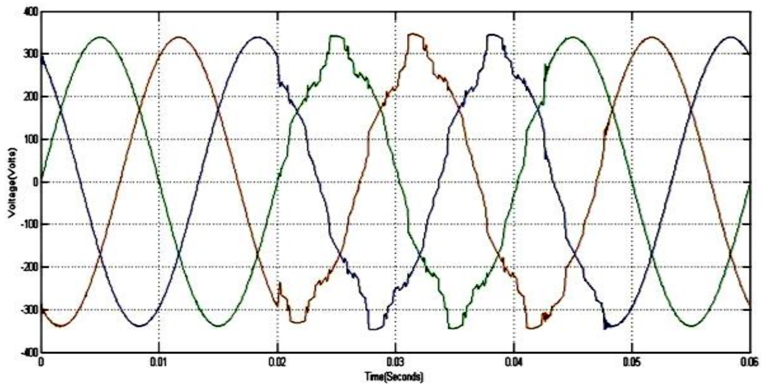

Fig 9. Output voltage after compensation

Harmonic analysis of the output voltage was carried out. It was found that before the compensation, the Total Harmonic Distortion (THD) in the output voltage to be 24.97%. With the addition of DVR, in open loop, the THD in the load voltage was reduced to 5.43%. Since the THD should be less than 5%, closed loop control is necessary to reduce the harmonics further. The rms voltage during compensation was found to be approximately 226 V, which is slightly less than the required value.

To control the amount of voltage being injected to the grid, through inverter a closed loop control is used to control the output of CHBMLI. The output of

CHBMLI is controlled by using a PI controller. The closed loop control is used to get the required load rms voltage.
The output voltage with closed loop control is shown in Fig. 10.

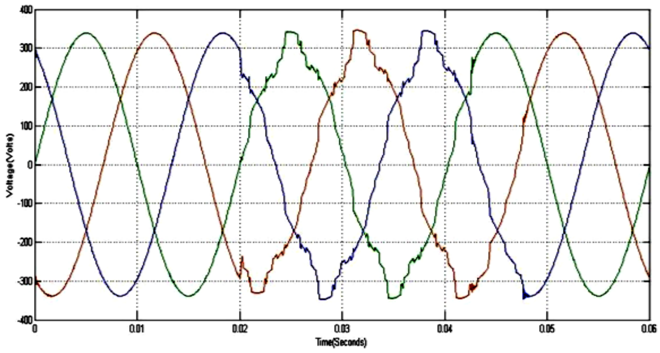

Fig 10. The load voltage with closed loop control of CHBMLI

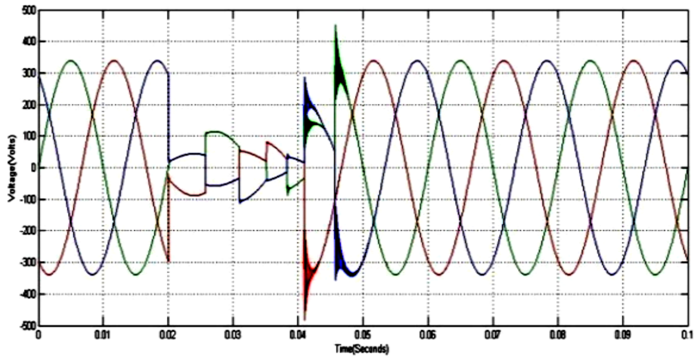

Fig 11. Load voltage when rectifier fed RL load is connected to the grid

With closed loop control of the DVR, the harmonic content was further reduced to 3.76% and the source voltage THD is 0.8%. The load voltage was almost 230 V (RMS).

To validate the proposed control scheme for various types of loads, a nonlinear load is considered. It consists of a controlled rectifier fed RL load. When this load is added, there is a decrease in the voltage which is indicated in 11. From the simulation results, it is observed that as the load demand increases, there was a dip in the load voltage. DVR a sensing circuit senses this dip and triggers DVR output to provide additional voltage support. Therefore, DVR can be used to provide additional real power demand. The THD of the load voltage which was almost 25% was reduced to 3.76% with closed loop control. The compensation is taking place within the next cycle of supply. Therefore, the dynamic response of DVR is appreciable. The source voltage and the load the load voltage distortions are compensated using the Cross Switched CHBMLI. The load voltage after compensation is shown on Fig. 12. It is observed from Fig. 12, even for nonlinear loads, the control algorithm ensures compensation of voltage during sag. With closed loop DVR injection, THD in load voltage is reduced to1.07% which is appreciable. The THD in the supply after compensation is found to be 0.72%.

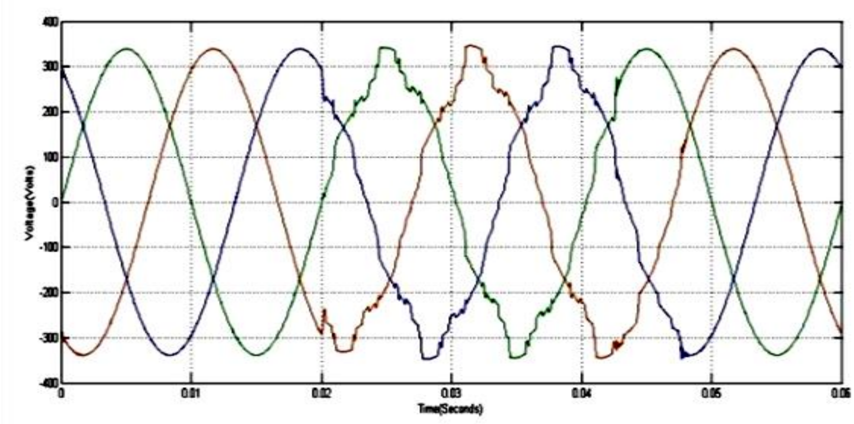

Fig 12. Load voltage for RL load after the closed loop injection

4. Experimental Results and Analysis

The CHBMLI based DVR is experimentally implemented and the experimental setup is shown on Fig. 13. The pulse pattern required for the multilevel inverter switches are generated using the microcontroller DSPIC30F4011 microcontroller. The inverter switching pulses are shown in Figs. 14-18. The inverter output is shown in Fig. 17. This multilevel output was then passed through an LC filter. The multilevel inverter along with the LC filter is then realized as a DVR.

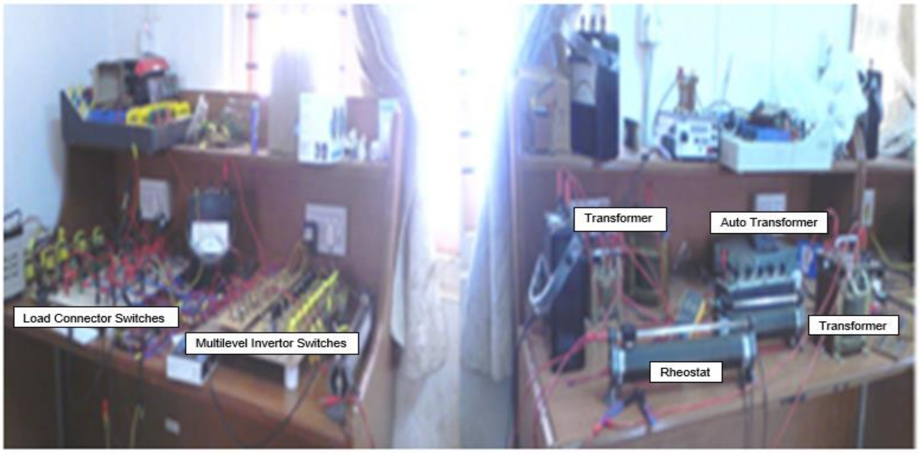

Fig 13. Eleven level Cross Switched Multilevel Inverter Power Circuit-Experimental Setup

Channel 1: Pulse for switches 2 and 3
Channel 2: Pulse for switches 1 and 4

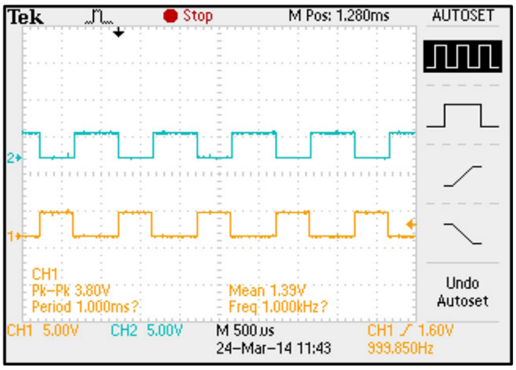

Fig 14. Gate pulses for switches S2, S3 and S1, S4

Channel 1: Pulse for switch 5
Channel 2:Pulse for switch 6

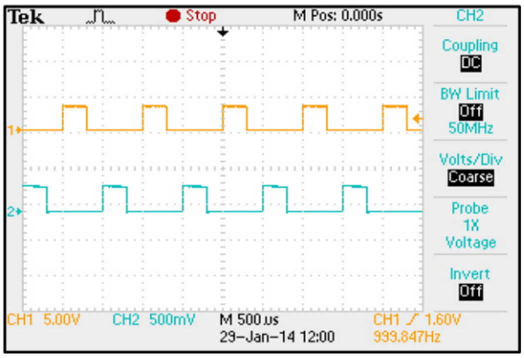

Fig 15. Gate pulses for switches S5 and S6

Channel 1: Pulse for switch 7
Channel 2: Pulse for switch 8

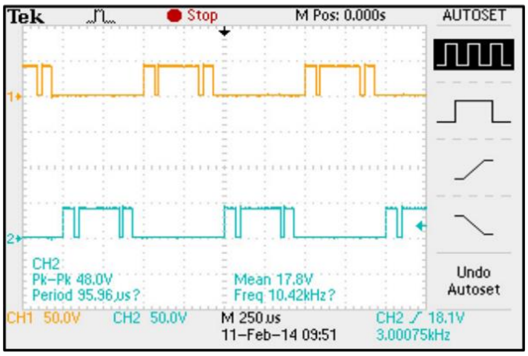

Fig 16. Gate pulses for switches S7 and S8

Channel 1: Pulse for switch 9
Channel 2:Pulse for switch 10

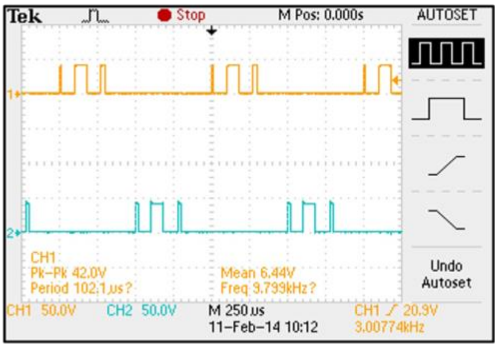

Fig 17. Gate pulses for switches S9 and S10

Channel 1: Pulse for switch 12
Channel 2: Pulse for switch 11

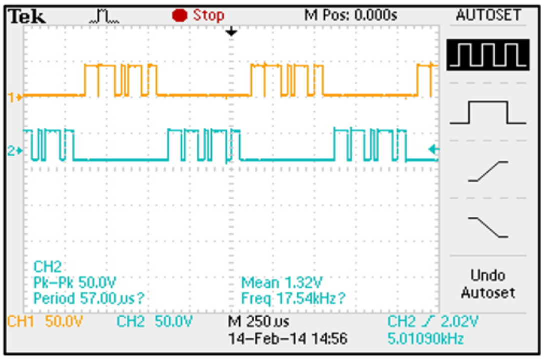

Fig 18. Gate pulses for switches S12 and S11

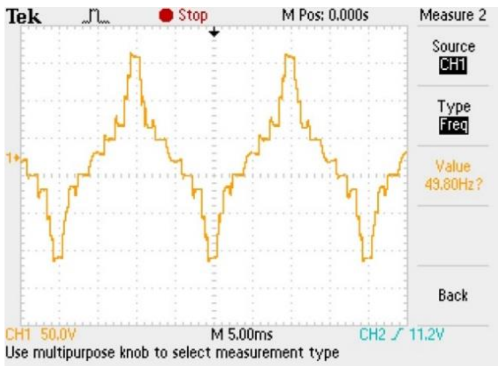

Fig 19. CHBMLI Output voltage

The supply voltage before applying load is shown in Fig. 20. The RMS voltage is 230 V. The voltage when load is connected is shown in Fig. 21.

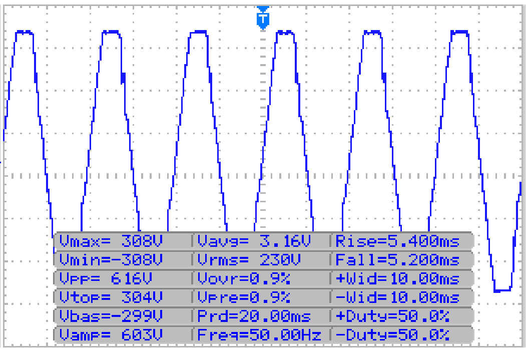

Fig 20. Voltage on no load

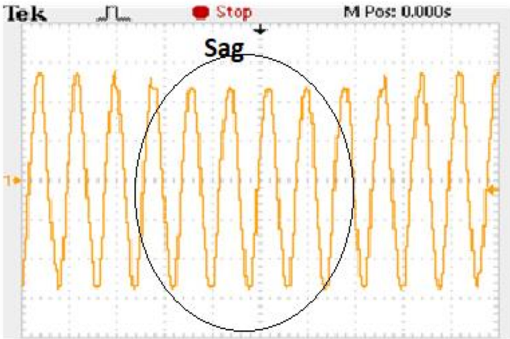

Fig 21 Voltage when the load is connected

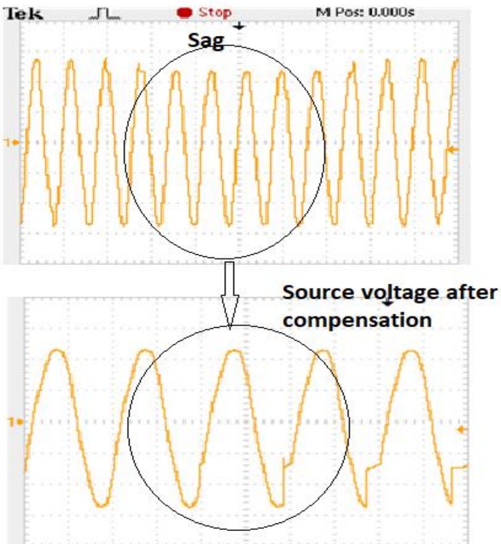

Fig 22. Source voltage after compensation

It is observed from Fig. 21, that there is voltage dip during the presence of additonal load. The compensated load voltage is shown in Fig. 22.

6. Conclusions

A 11 levels single phase CHBMLI was designed to obtain a peak voltage of 310 V at 50 Hz frequency and the same was simulated using Matlab. Voltage sag for approximately 0.04 sec. is introduced in the supply voltage by adding an additional inductive load of 200 mH. The THD in load voltage was 24.97% before compensation. A control circuit was designed to inject the voltage from CHBMLI at common point of coupling during voltage sag to compensate for the voltage dip. A novel control technique was introduced to sense the dip in voltage and release the pulses to CHBMLI which in turn will inject the voltage from a DC source to take care of decrease in which due to additional load demand. The THD in the load voltage was reduced to 19.71% with injection from DVR in open loop mode and was further reduced to 18.14% with closed loop control of DVR. In table 3 the comparison of the proposed work with the previous work [28] is compared.

Table 3

Results Evaluation

	Open Loop Control	Closed Loop Control
Proposed work	19.71%	18.14%
[28]	31.9%	29.13%

The results show that the proposed work efficiently works on the non-linear load for voltage swell compensation. Further the work can be extended to three phase system and a fuzzy controller can be used to control the CHBMLI output voltage.

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