NEW MOS SATURATION ANALYTICAL MODEL

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Modelele actuale pentru tranzistoarele MOS ce descriu variaţia curentului de drena în regim de saturaţie folosesc preponderent parametrii empirici. Şi aceasta din cauza limitărilor impuse de caracterul bidimensional al canalului tranzistorului MOS. Aproximaţia graduală nu mai este valabilă pentru întreaga analiza a tranzistorului din cauza scurtării lungimii efective canalului. Dar aproximaţia graduală este valabilă pe lungimea efectivă rămasă a canalului tranzistorului. Acesta s-a dovedit a fi un bun punct de pornire pentru un model analitic al tranzistorului în saturaţie. Această lucrare îşi propune să prezinte un asemenea model analitic ce este în strânsă legatură cu modelul fizic, foloseşte doar date experimentale pentru extracţia parametrilor şi este bazat pe un raport determinat a fi constant al rezistenţei canalului în regiunea de saturaţie în funcţie de rezistenţa corespunzătoare din regiunea liniară.

Actual MOS transistor models only use empirical models for describing the variation of the drain current in saturation. This is mainly due to the bidimensional character of the MOS transistor channel. Gradual approximation is no longer valid for the whole transistor analysis due to the channel length modulation. But the gradual approximation still stands for the effective channel length of the transistor. And this proved to be a good starting point to an analytical model for saturation. This paper proposes to present one such analytical model that is closely related to the physical model, only uses experimental data for its parameter extraction and is based on a determined constant ratio of the channel resistance in the saturation region with respect to the same resistance in the linear region.

1. Introduction

The MOS transistor is an active electronic component with 4 terminals: drain, source, gate and bulk. The bulk is generally considered as the potential reference. The MOS transistor is a symmetric structure according to the position of the drain and the source. Therefore, the drain is defined as the end that has a potential V_D higher than the other end V_S. The source-bulk and drain-bulk junctions are reverse biased so $V_S>0$ and $V_D>0$. The gate voltage V_G has to control the channel between the source and the drain.

For any given V_{DS} voltage the transistor can operate in 3 inversion regimes depending on the gate voltage V_G: weak, moderate and strong inversion.

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The limits of these regimes can be considered in a narrow region around the threshold voltage, more specifically within $\pm 3\varphi_t$ around $2\varphi_F$, the value of the surface potential corresponding to the threshold voltage V_T. For any given V_{GS}, the transistor can operate in 2 regions depending on the value of the V_{DS} voltage: linear and saturation. The boundary between these regions is defined as the saturation voltage V_{DSsat} and it varies from approximately $3\varphi t$ in weak inversion to V_G-V_T in strong inversion. This variation in the weak and moderate inversion makes it complicated to accurately measure the saturation voltage. Also the needs of actual analog designs are targeted towards the strong inversion region where the transistor operates above threshold. That is why the discussion regarding the analytical model proposed by this paper will be done on the strong inversion regime. But the model is also valid in weak and moderate inversion regimes

2. Strong inversion considerations

A transistor is considered to operate in strong inversion if this regime is assured for the source end of the channel. The drain can remain in strong or go into weak inversion. Actual models for strong inversion offer analytical relations for the static characteristics of the transistor only in the linear region. For saturation, a constant drain current is considered [1] or an increasing one based on certain channel length reduction models which are more or less based on empirical parameters.

Considering the source-bulk voltage 0, if strong inversion is guaranteed at the source end of the channel and if $V_D = V_S$, the drain end will also be strongly inverted. If the drain potential is raised, the level of inversion there will decrease and, eventually, strong inversion at that point will cease. Strong inversion at both ends ensures strong inversion throughout the channel since the surface potential varies monotonically from the source to the drain. In strong inversion the current is almost totally due to drift.

The general drain current expression used by all strong inversion models is:

$$I_D = \beta[f(V_G, V_S) - f(V_G, V_D)], \tag{1}$$

where $f(V_G,V_{CH})$ is a primitive of the charge function over the channel, Q_I/C_{ox}:

$$f(V_G, V_{CH}) = \int \frac{Q_I(V_G,V_{CH})}{C_{ox}} dV_{CH}. \tag{2}$$

All models that describe strong inversion set the primitive function $f(V_G,V_{CH})$ only when the channel is in strong inversion over its whole length. This is viable for small $V_{DS}=V_D-V_S$ voltages corresponding to the linear region. As the drain voltage V_D is increased, the analytical expression (1) offers a maximum point and then the decrease of the drain current. This behavior does not reflect reality and it is due to the drain end of the channel exiting from strong inversion. This is equivalent to the channel's length modulation. According to these observations, the voltage corresponding to the separation point between the linear and saturation region, V_{DP}, also called pinch-off voltage, results from the maximum point condition:

$$\left.\frac{\partial I_D}{\partial V_D}\right|_{V_D=V_{DP}} = 0. \tag{3}$$

Ihantola-Moll model [2] was the first model that dealt with MOS transistor behavior in strong inversion. It is based on the observation that the surface potential φ_S for a MOS capacitor in strong inversion remains constant with the variation of the gate voltage V_G. The model has a good accuracy but its biggest constraint is the complicated equations which lead to increased simulation times. One simplification comes from some observations and approximations that can be done on the volume charge. But for most transistors these approximations might lead to considerable errors in the drain current. Merckel-Borel-Cupcea model [3] helps reduce these errors and also keeps the equations at a simplified mathematical form.

But strong inversion models offer analytical expressions for the static characteristics only in the linear region of the transistor characteristics. For the saturation region they consider a constant drain current or one that varies with the drain voltage but based on specific channel modulation models that use empirical or fitting parameters. Experiments have shown that in the saturation region the current has indeed a slight increase with the applied V_{DS} voltage. The effect is more pronounced as the length of the channel is shorter. The description of this effect can be made using the channel modulation concept. According to the strong inversion models, the channel exists only if the surface electron concentration satisfies the condition:

$$n_S(y) \geq N_A. \tag{4}$$

If the gate is biased over threshold ($V_G>V_T$) and the transistor works in the linear region ($V_S<V_D<V_{DP}$) the relation (1) is fulfilled from source to drain. If it goes further into saturation ($V_S<V_{DP}<V_D$), the drain end of the channel does not

fulfill the condition (4). Then an effective channel length L_{eff} is defined and it represents the most distant point from the source that still fulfills condition (4):

$$n_S(L_{eff}) = N_A. \tag{5}$$

This implies that the potential in the effective channel equals the pinch-off voltage V_{DP}. As the drain voltage is increased the channel shortens even more but the voltage drop across it remains constant (V_{DP}-V_S). Therefore an inverse proportional relation between the drain current at saturation and the effective channel length can be given:

$$I_D = I_{DSS}\frac{L}{L_{eff}} = I_{DSS}\frac{L}{1-\frac{\Delta L}{L}}, \tag{6}$$

where $\Delta L = L - L_{eff}$ is the channel modulation. Its dependence upon the voltage applied on the drain is done using the depletion approximation. This is because the surface zone between the end of the channel and the drain is depleted of both holes ($\varphi_s > 0$) and electrons (Q_I=0). This zone sustains a potential difference of V_D-V_{DP}. Therefore the channel modulation can be described as:

$$\Delta L = \propto \sqrt{V_D - V_{DP}}\,;\; V_D \geq V_{DP}, \tag{7}$$

where α is an empirical parameter that gives the closest approximation to reality of the variation. But equation (7) cannot be used into (6) because in simulation programs this leads to a discontinuity point of the first derivative $\partial I_D/\partial V_D$ for V_D=V_{DP} when it is joined with the drain current expression for the linear region (in this region the first derivative is 0). That is why a preferred relation for (7) is one extended for the whole work domain of the transistor:

$$\Delta L = \propto \sqrt{V_D - V_S}\,;\; \forall\, V_D > V_S. \tag{8}$$

The length correction of the channel in the linear zone, opposite to the physical model, is insignificant for low V_{DS} values. Another empirical approximation version considers a linear dependence of the drain current to V_D-V_{DP}:

$$\Delta L = \propto '(V_D - V_{DP}), \tag{9}$$

where α' is a parameter determined from measures. Taking into account that the channel modulation effect is weak for long channel transistors, introducing equation (9) into (6) leads to a drain current:

$$I_D = I_{DSS}[1 + \lambda(V_D - V_{DP})], \tag{10}$$

where $\lambda = \alpha'/L$ represents the output conductance at the point of entering saturation. This relation indicates a linear increase of the drain current with the drain voltage, which corresponds reality. A similar relation to (10) is also used by the Merckel-Borel-Cupcea model for describing the drain current in saturation:

$$I_D = I_{DSS}\left(1 + \frac{V_D - V_{DP}}{V_E + V_{DP} - V_S}\right), \tag{11}$$

where V_E is the Early voltage for the MOS transistor. Its value is found at the intersection of V_{DS} axis with the extrapolated linear characteristics from the saturation region.

Ihantola-Moll model offers an equation for saturation region closer to the general drain current expression (1) but adapted to fit real behavior:

$$I_D = \beta[f(V_G, V_S) - f(V_G, V_{DP})]. \tag{12}$$

The pinch-off voltage V_{DP} which results from applying the continuity conditions can be seen below:

$$V_{DP} = V_S + V_E\left[\sqrt{1 + \frac{2(V_G - V_T)}{V_E(1+\delta)}} - 1\right], \tag{13}$$

for Merckel-Borel-Cupcea model, where δ is the slope of the tangent line in $V_{CH}=V_S$ of the charge variation function over the channel and

$$V_{DP} = -2\varphi_F + \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_G - V_{FB}}\right)^2, \tag{14}$$

for Ihantola-Moll model.

As it can be seen above, describing the behavior of the drain current in saturation takes into account several approximations and empirical parameters. Therefore the drain current equations for saturation given by both presented models can be considered as empirical ones. What would be of interest is an analytical model that is closer to the physical model, reflects much better the real behavior of the transistor and that only uses measured data for its parameter extraction.

3. Analytical model background

The starting point of such an analytical model is a MOS transistor moderate inversion model [4] based on the charge sheet model [5]. It is basically an extension of the gate-junction circuit shown in Fig. 1. Diodes D_S and D_D model

the surface region of the source-substrate and drain-substrate junctions. The MOS transistor function is considered as the injection of charge through the source-channel (D_S) and channel-drain (D_D) junctions.

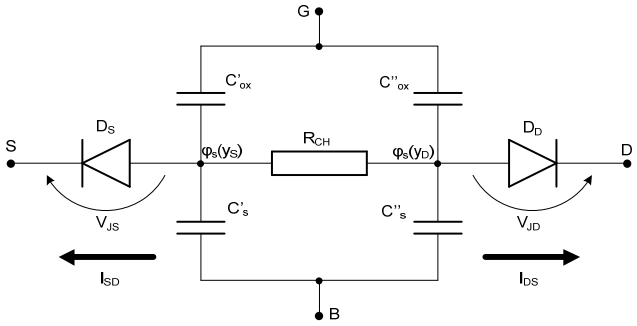

Fig. 1. Equivalent circuit of a MOS transistor.

The total channel resistance is noted R_{CH}. The cathodes of the two diodes represent the source and drain of the transistor. The anodes of the diodes have the potentials $\varphi_s(y_S)$ and $\varphi_s(y_D)$ and represent the potentials at the channel limits so at source and drain one.

This moderate inversion model uses the two components of the drain current, diffusion current and drift current and it is based on their ratio in the total drain current to give a general expression for the drain current available in moderate inversion region:

$$I_D = \frac{1}{r_{d0}} \cdot \frac{\varphi_t}{R_{CH0}} \cdot \left[1 - exp\left(-\frac{r_{d0} \cdot V_{DS}}{\varphi_t}\right)\right], \tag{15}$$

where R_{CH0} and r_{d0} are channel resistance respectively diffusion current ratio when $V_{DS} \rightarrow 0$ and φ_t is the thermal voltage.

It can be proved that this expression also describes the transistor in weak and strong inversion. For example in strong inversion the diffusion current is negligible ($r_{d0} \rightarrow 0$). Developing in series the exponential function:

$$exp\left(-\frac{r_{d0} \cdot V_{DS}}{\varphi_t}\right) \cong 1 - \frac{r_{d0} \cdot V_{DS}}{\varphi_t}, \tag{16}$$

we obtain the equation:

$$I_D = \frac{V_{DS}}{R_{CH0}}. \tag{17}$$

This proves the „resistive" behavior of the MOS transistor in strong inversion.

But this model is valid only in the linear zone of a transistor's characteristics, where the gradual approximation can be used. What would be of interest is what happens beyond, in saturation, and to find an analytical way of describing the increase in the saturation current with the increase of the source drain voltage.

4. Channel resistance ratio

The proposed method is by using the ratio R_{CHsat}/R_{CH0} of the channel resistance at saturation and the incipient channel resistance. This is calculated by parameter extraction from the measured data of a transistor.

Measurements and calculations were done on a long channel NMOS transistor. This was chosen not to get into second order short channel effects. Measured characteristics were $I_D(V_{GS})$ at a fixed V_{DS} for various V_{SB} and $I_D(V_{DS})$ for V_{SB}=0 and various V_{GS}. The only needed transistor parameters for a proper usage of its measured characteristics are the physical dimensions width W and length L and the oxide thickness t_{ox}. For the ease of calculations V_S was grounded.

4.1. General parameters determination

The starting point is the extraction of the threshold voltage from $I_D(V_{GS})$ characteristics at each V_{SB} by using the transconductance derivative method [6]. This is afterwards needed for the determination of the flat band voltage V_{FB}, the substrate factor γ, the acceptor ions concentration N_A and Fermi level potential φ_F. The threshold voltage referred to the source is:

$$V_T = V_{FB} + \varphi_{sT} + \gamma \cdot \sqrt{\varphi_{sT} + V_{SB}}. \tag{18}$$

This can be considered as a function $V_T = f\left(\sqrt{\varphi_{sT} + V_{SB}}\right)$ so V_T has a linear dependence with $\sqrt{\varphi_{sT} + V_{SB}}$. Therefore the slope of this function is the substrate factor γ and the intersection of the function with Oy axis is $V_{FB} + \varphi_{sT}$ where $\varphi_{sT} = 2 \cdot \varphi_F + n \cdot \varphi_t$ (n=[1...3]) is the surface potential when the gate is biased with the threshold potential (V_G=V_T). The coefficient n was chosen 1.

The extraction procedure is iterative. A typical value is first chosen for φ_{sT} (e.g. 0.6V). With this value and $V_T(V_{SB})$ characteristic calculated earlier, the $V_T = f\left(\sqrt{\varphi_{sT} + V_{SB}}\right)$ graph can be built from where γ and $V_{FB} + \varphi_{sT}$ can be determined. Afterwards N_A and φ_F can be calculated from:

$$N_A = \frac{\gamma^2 \cdot C_{ox}^2}{2 \cdot q \cdot \varepsilon_S} \quad , \quad \varphi_F = \varphi_t \cdot \ln \frac{N_A}{n_i}. \tag{19}$$

After having determined the value for φ_F, the extraction procedure can be restarted by correcting the value φ_{sT} with the new φ_F calculated. The process can be repeated until a desired error tolerance from the previous iteration is obtained.

4.2. The channel resistance R_{CH0}

The first step in the calculation of the incipient channel resistance R_{CH0} is to calculate the surface potential at the source end of the channel, $\varphi_s(y_S)$. This is done for each V_G used in measuring $I_D(V_{DS})$ characteristics. The calculation can be done recursive from:

$$V_G = V_{FB} + \varphi_S(y_S) + \gamma \sqrt{\varphi_S(y_S) + \varphi_t \exp\left(\frac{\varphi_S(y_S) - 2\varphi_F}{\varphi_t}\right)}. \tag{20}$$

Having determined $\varphi_s(y_S)$, the inversion charge at the source end of the channel can be calculated from:

$$Q_I(y_S) = -\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A}\left(\sqrt{\varphi_S(y_S) + \varphi_t \exp\left(\frac{\varphi_S(y_S) - 2\cdot\varphi_F}{\varphi_t}\right)} - \sqrt{\varphi_S(y_S)}\right). \tag{21}$$

The next step is determining the effective surface mobility. Above threshold this is defined as:

$$\mu = \frac{\mu_0}{1 + \theta_G \cdot (V_G - V_T)}, \tag{22}$$

where μ_0 is the surface mobility when the transversal field is 0 (or very small) and θ_G is a model parameter. They are determined in a similar way to the extraction of the flat band voltage V_{FB} and the substrate factor γ [7].

Having determined the inversion charge at the source and the effective surface mobility, R_{CH0} can be calculated from:

$$R_{CH0} = \frac{L}{W \cdot \mu \cdot Q_I(y_S)}. \tag{23}$$

4.3. The channel resistance at the saturation point R_{CHsat}

The channel resistance at the saturation point is defined at $V_{DS}=V_{DSsat}$. Looking at Fig. 1, the drain-source voltage V_{DS} can be described as:

$$V_{DS} = \varphi_S(y_S) + R_{CH} \cdot I_D + V_{JD}. \tag{24}$$

The saturation point, so the pinch-off voltage, can be defined as the moment when V_{JD}=0. So at this point:

$$V_{DSsat} \equiv V_{DP} = \varphi_S(y_D). \tag{25}$$

From (24) and (25) the channel resistance in saturation can be written as:

$$R_{CH_{sat}} = \frac{\varphi_S(y_D) - \varphi_S(y_S)}{I_{D_{sat}}}, \tag{26}$$

where I_{Dsat} is the drain current in saturation.

The surface potential at the drain end of the channel, $\varphi_s(y_D)$ can be calculated from:

$$V_G = V_{FB} + \varphi_S(y_D) + \gamma\sqrt{\varphi_S(y_D) + \varphi_t \exp\left(\frac{\varphi_S(y_D) - 2\varphi_F - V_{DS}}{\varphi_t}\right)}. \tag{27}$$

As consequence, considering a fixed gate voltage V_G, for each V_{DS} there is a specific $\varphi_s(y_D)$ that fulfills equation (13). But the one of interest here is when V_{DS}=V_{DSsat}. The current I_{Dsat} is then extracted from the measured $I_D(V_{DS})$ characteristics and R_{CHsat} can then be calculated using (26).

For a considered transistor with physical dimensions W=L=10μm and oxide thickness t_{ox}=12.5nm, the ratio R_{CHsat}/R_{CH0} obtained is shown in Fig. 2.

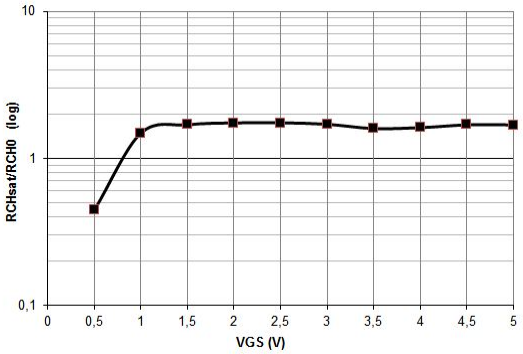

Fig. 2. Channel resistance ratio.

It can be seen that the ratio R_{CHsat}/R_{CH0} has a constant value, ct≈1.65, across the whole strong inversion regime. In weak and moderate inversion there is

a further need for a very good accuracy in both measurements and calculations. This is due to very small differences in potentials at source and drain, so a few millivolts error in their calculation (which can be triggered by measurements or numerical approximations in parameter extraction) is propagated and amplified in the R_{CHsat}/R_{CH0} ratio. Basically in weak and moderate inversion the error is in a direct relation with measurement and parameter extraction accuracy.

5. Analytical model for the drain current in saturation

The constant ratio result is of great importance as it can give an analytical approach to the problem of defining the drain current beyond saturation point.

In Fig. 3a the R_{CHsat}/R_{CH0} ratio can be better „visualized" and understood. In the upper part, when $V_{DS}\approx 0$, the charge distribution across the channel is uniform and so the resistance can be seen as a „rectangle" model. In the lower part, when $V_{DS}=V_{DSsat}$ the charge distribution is no longer constant but decreasing from source's initial $Q_I(y_S)$ value to 0 at the drain. So the resistance of the channel can be defined by a „triangle" model. So the constant ratio R_{CHsat}/R_{CH0} can be therefore seen as a „triangle/rectangle" ratio.

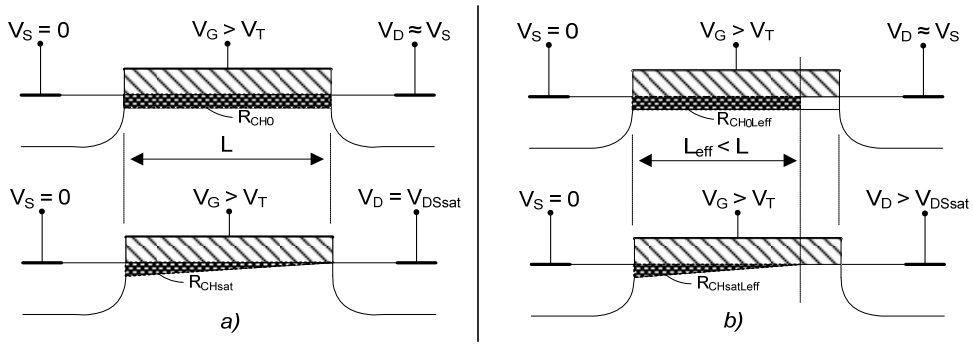

Fig. 3. Channel resistance variation and models

a) incipient saturation → $V_D = V_{Dsat}$,

- R_{CH0} → incipient channel resistance defined for the whole length of the channel L
- R_{CHsat} → channel resistance in incipient saturation (so defined for the whole channel length L)

b) deep saturation → $V_D > V_{Dsat}$

- $R_{CH0Leff}$ → ideal resistance defined with respect to R_{CH0} as an incipient channel resistance but for the modulated length of the channel
- $R_{CHsatLeff}$ → channel resistance in deep saturation (so defined for the modulated length of the channel L_{eff})

When $V_D=V_{DSsat}$, the inversion charge at the drain reaches 0 (fig. 3a). If V_D is increased, the channel shortens to an effective length L_{eff} (fig. 3b). The new phenomenon that appears here is the disappearance of the channel (inversion

layer) near the drain and the appearance of a fully depleted region between the inversion channel and the drain region. Between the ends of the effective channel the voltage drop remains a constant V_{DSsat} this being the base premises of the drain current saturation. The increase in the drain current is only due to channel effective length shortening with the drain-source voltage increase. As the shortening is a weak effect, so is the increase in the drain current. From the end of the effective channel to the drain, the current closes due to the contribution of a longitudinal field that appears in this region pointing from the drain region toward the inversion channel. Carrier electrons in the channel that reach the depletion boundary are swept across the depleted region into the drain.

The way to determine the drain current in the saturation region is to use the same approach for calculating the drain current at the saturation point, where the channel length is still L, at a point where the channel shortens to an effective channel length of L_{eff} (fig. 3b).

When $V_{DS}>V_{DSsat}$, the channel length will be L_{eff} and the channel resistance will be $R_{CHsatLeff}$. The voltage drop on the channel resistance remains the same. But the channel resistance is scaled by L_{eff}. The incipient channel resistance for the considered shortened channel L_{eff} and having an uniform inversion charge $Q_I(y_S)$ is defined as $R_{CH0Leff}$:

$$R_{CH0Leff} = \frac{L_{eff}}{W \cdot \mu \cdot Q_I(y_S)} . \tag{28}$$

We can then apply the same „triangle/rectangle" concept. As consequence:

$$\frac{R_{CHsatLeff}}{R_{CH0Leff}} = \frac{R_{CHsat}}{R_{CH0}} = ct. \tag{29}$$

The effective channel length in strong inversion is calculated from:

$$L_{eff} = L - W_{JD} \cdot \left(1 - \sqrt{\frac{\varphi_{sL}}{V_D + V_{Bi}}}\right), \tag{30}$$

where V_{Bi} is the internal potential difference and W_{JD} is the width of the depletion region at the drain defined by:

$$W_{JD} = \sqrt{\frac{2 \cdot \varepsilon_S}{q \cdot N_A} \cdot (V_D + V_{Bi})} . \tag{31}$$

So from equations (26) and (29) the current in the saturation region can be written as:

$$I_{DsatLeff} = \frac{\varphi_s(y_D) - \varphi_s(y_S)}{R_{CHsatLeff}} = \frac{\varphi_s(y_D) - \varphi_s(y_S)}{ct \cdot \frac{L_{eff}}{W \cdot \mu \cdot Q_I(y_S)}} \quad . \tag{32}$$

Calculations have been made for 4 gate voltages in strong inversion and Fig. 4 shows the measured and calculated drain current in the saturation region.

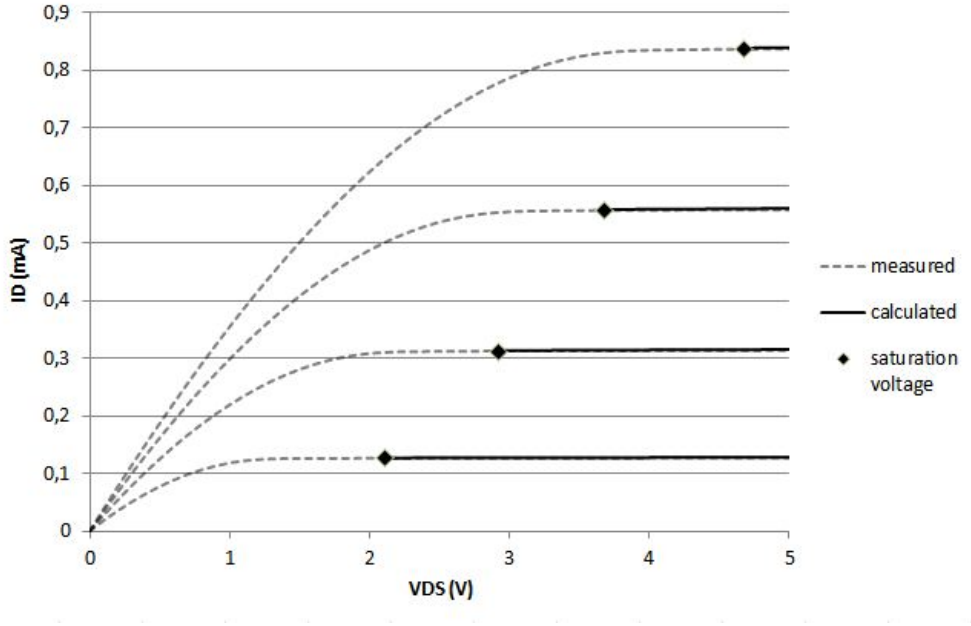

Fig. 4. Measured and calculated drain current using channel resistance ratio model with highlight of the calculated incipient saturation points

The same calculation of the drain current in saturation was done using the two other models for strong inversion previously described, Merckel-Borel-Cupcea and Ihantola-Moll. The results can be seen below (in fade grey is the representation of the calculated drain current in the linear region):

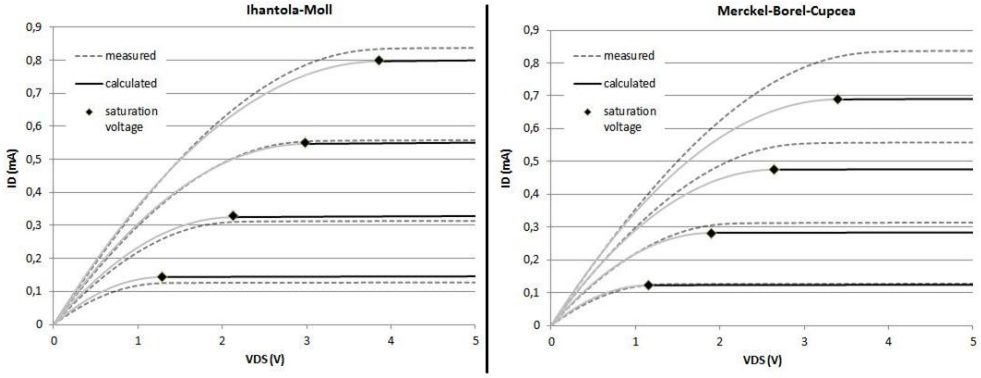

Fig. 5 Measured and calculated drain current using Merckel-Borel-Cupcea and Ihantola-Moll models with highlight of the calculated incipient saturation points

The saturation voltages at pinch-off point that have been highlighted by dots in Figs. 4 and 5 were obtained using the corresponding equation for each model, (25) for the channel resistance ratio model, (13) for Merckel-Borel-Cupcea model and (14) for Ihantola-Moll. These values can also be seen in Table1. The classic model relation $V_{DSsat}=V_G-V_T$ was also added for comparison.

Table 1

Saturation voltage at pinch-off

Model	Gate Voltage (V)			
	V_G=2V	V_G=3V	V_G=4V	V_G=5V
$V_{DSsat}=V_G-V_T$	1.54	2.54	3.54	4.54
Channel resistance ratio	2.11	2.92	3.67	4.68
Merckel-Borel-Cupcea	1.15	1.90	2.65	3.39
Ihantola-Moll	1.29	2.13	2.98	3.85

As it can be observed in Figs. 4 and 5 the calculated drain current with the presented method based on the channel resistance is very close to the measured one, compared to the other two models used. In the table 2 there is a comparison of the medium relative errors for the 3 models at all 4 voltages used in calculation.

Table 2

Medium relative error

Model	Medium relative error (%)			
	V_G=2V	V_G=3V	V_G=4V	V_G=5V
R_{CH} ratio	0.44	0.41	0.35	0.27
Merckel-Borel-Cupcea	2.68	10.44	16.94	20.84
Ihantola-Moll	12.53	4.27	1.51	4.77

As it can be seen from table 2, the maximum relative error for the channel resistance ratio model is under 0.5%, meaning a maximum difference of under 1μA between the measured and determined drain current for all $I_D(V_{DS})$ characteristics in the saturation region.

6. Conclusions

This paper has shown a method to analytically determine with a very good accuracy the drain current variation with the drain-source voltage in the saturation region. This is based on a constant ratio found between the incipient channel resistance R_{CH0} determined in the linear region and the channel resistance at the saturation point R_{CHsat} determined at incipient saturation for all gate bias voltages in strong inversion. This ratio has been calculated from measured characteristics. For the deep saturation region so for the modulated channel length, two other resistances have been introduced, $R_{CH0Leff}$ and $R_{CHsatLeff}$, in correspondence to the two previous defined ones. The model key is to ensure that the ratio remains constant for the last two introduced resistances in the whole saturation region. The results offered by this analytical model proved to be much closer to measured characteristics then previous empirical models. With a better accuracy in measurements and improved calculation methods the relative error in the drain current at saturation can be further minimized.

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