DESIGN AND VERIFICATION OF LOW VOLTAGE SERIAL INTERFACE WITH DUAL I2C/I3C COMPATIBILITY

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This paper reveals the design and key verification results corresponding to a mixed-signal integrated circuit equipped with a digital serial interface having dual I2C and I3C compatibility. Main I3C features were added to upgrade an I2C digital controller for responding to the latest market trends in embedded systems applications and for extending the applications range. This architecture distinguishes itself by no usage of internal sampling clock signal. The circuit was implemented in a CMOS 65 nm technology. It operates in low voltages domain, 1.8 V - 3.6 V, across a large temperature range, -40 ºC ÷ 125 ºC. In I3C mode, our circuit is capable of working with frequencies of at least 12.5 MHz.

Keywords: CMOS 65 nm, I2C, I3C, mixed-signal architecture, serial interface.

1. Introduction

The electronic circuits which are components of complex systems, communicate through different protocols. The Inter-Integrated Circuit (I2C) protocol is a widely used, industrial standard meant to control the communication between multiple devices like CPUs, sensors, memories, AD/DA converters, etc. It is built upon a digital interface, handling synchronous, slow speed digital data, having an advantageous implementation based only on two wires to connect up to 128 devices [1].

In 2016 a new version of I2C interface was launched, namely Improved Inter-Integrated Circuit – I3C. This protocol is meant to add higher operation speeds (12.5 MHz), single or double data rate, an extended set of special commands, new internal registers, and new interrupt capabilities [2], [3].

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The signals involved in an I2C transaction are named: SDA – Serial Data, SCL – Serial Clock. These wires are OD – Open Drain, thus an external pull-up resistor is needed [1], for I2C. On the other hand, during an I3C communication, the user can select the I2C mode with open drain pads being activated, or the I3C mode can be selected, thus push-pull inputs/outputs are being active [3]. Also, I2C communication is characterized by filtering the input signals having pulse widths in the range up to tens of nanoseconds [1].

The current market is still dominated by I2C architectures [4], [5], [6]. Although the I3C products are not highly available [7], they represent a strong future direction to chip-to-chip communication. This paper is intended to cover the gaps in design of I3C interfaces which preserve the I2C compatibility. Therefore, we propose an implementation containing an array of eight registers (each one byte) which can be accessed through a digital interface which is I2C compliant, but also compatible with the main features of the I3C interface. The circuit adds I3C mode detection, I3C read/write commands reception, and several registers containing chip characteristics.

The paper is structured as follows: Section 2 presents a description of the system's protocol functionality, followed by a detailed presentation of the designed architecture in Section 3. Section 4 contains the simulation results which validate the proposed system. Finally, conclusions are drawn.

2. Functional description

I2C communication is based on pulling the line low for transmitting 0 and releasing the line for a value of 1. The mechanism of byte acknowledgement assumes the transmitter releases the SDA line corresponding to the 9-th clock pulse and the receiver is expected to pull low the SDA line. After all data is transmitted, the bus must be freed, by a stop condition. The stop assumes a low to high transition of SDA while SCL is high [1], [2].

A typical I3C mode detection and operation flow is depicted in Fig. 1. The I3C communication starts in I2C mode, by issuing the 0x7E address. An I3C device can recognize this call and acknowledge it, allowing the controller to continue sending the command (Fig. 1). The specific feature of this protocol is the insertion of parity bit (T) instead of ACK (acknowledgement) bit for confirming to the master about the reception and integrity of data [2], [3].

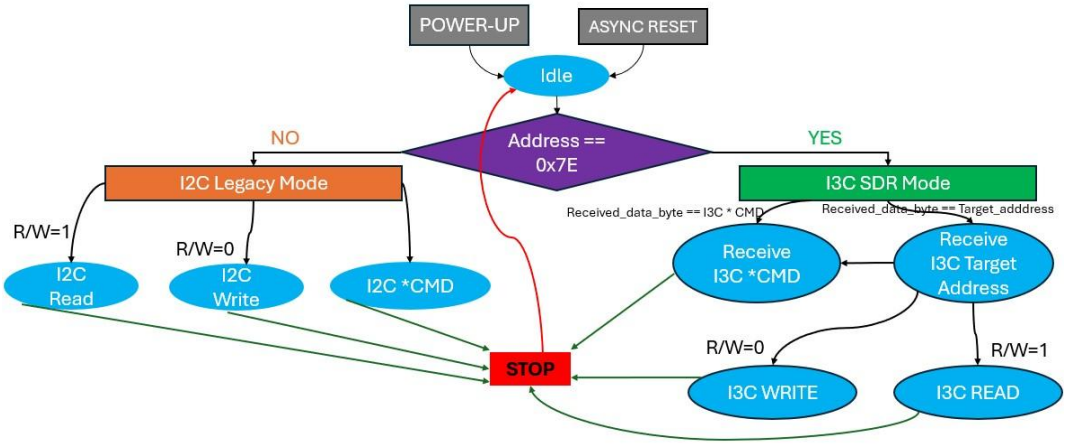

Fig. 1. I2C/I3C mode detection and communication

The Inter-integrated protocols operations flow is based on the functionality and timing and electrical specifications. Design of I2C/I3C circuit is built upon a synchronous architecture combined with asynchronous structures and including delays, filters, and custom I/O pad structures.

3. Digital Core Architecture

A diagram representing the proposed system is depicted in Fig. 2. The focus of this circuit is the I2C/I3C digital controller. It oversees communication and updates the content of the volatile storage registers.

The digital interface contains a multi-register structure that is updated by Write operations. To completely validate this block, the auxiliary analog blocks were designed and integrated with the digital controller into an entire chip containing input buffers, SDA bidirectional configuration, input filters, and power on reset (Fig. 2).

Fig. 3 shows the architectural concept of the digital controller implemented. This digital interface contains two structures meant to recognize the I2C events of START and STOP. All the data being transmitted on SDA and synchronized with SCL must be counted, by means of bit counters (one active on rising of SCL, another one active on falling of SCL) and a byte counter. The data being transmitted on SDA is shifted into an input-shift register containing eight bits (Fig. 3). There are two address detectors, one for the I3C compliance and another one corresponding to the address of the device itself. Another structure is the operational mode detection, op_mode. Circuitry for handling usage of characteristics registers is included. The main part of the interface is the finite state machine, able to control through the following states: IDLE, Receive Address, Receive Register Index, Read

state or Write state. The storage includes eight 8-bit volatile registers. An output control circuitry is provided for handing data that must be transmitted to the master (ACK, T, data bits) (Fig. 3).

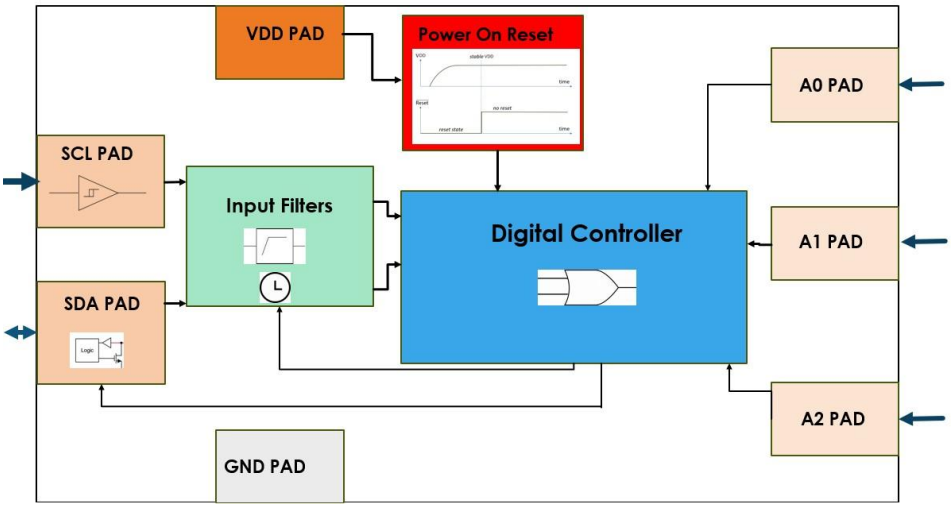

Fig. 2. Diagram of the chip

The asynchronous reset functionality of the digital controller was provided by the Power-On-Reset block [8]. It was designed to target a threshold value of 1.2 V for supply voltage [4], [5], [6].

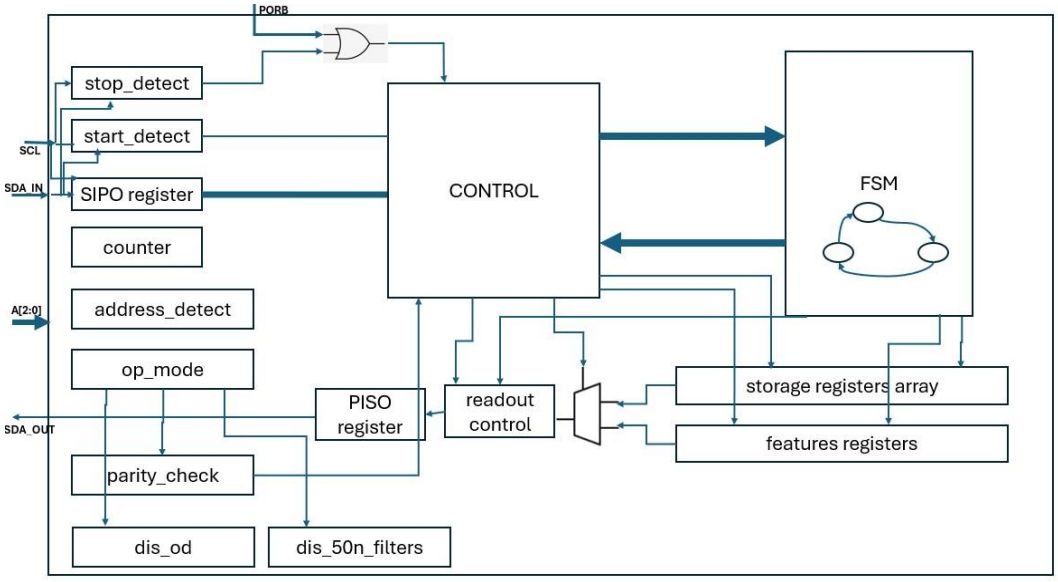

Fig. 3. Digital controller's internal architecture

The SCL and address inputs (A0, A1, A2) have pads structures containing input triggers. The bidirectional SDA configuration is depicted in Fig. 4.

SDA structure has the possibility to activate open-drain or push-pull capability, depending on the control signal, named dis_od. When sda_out signal is active, input path is deactivated.

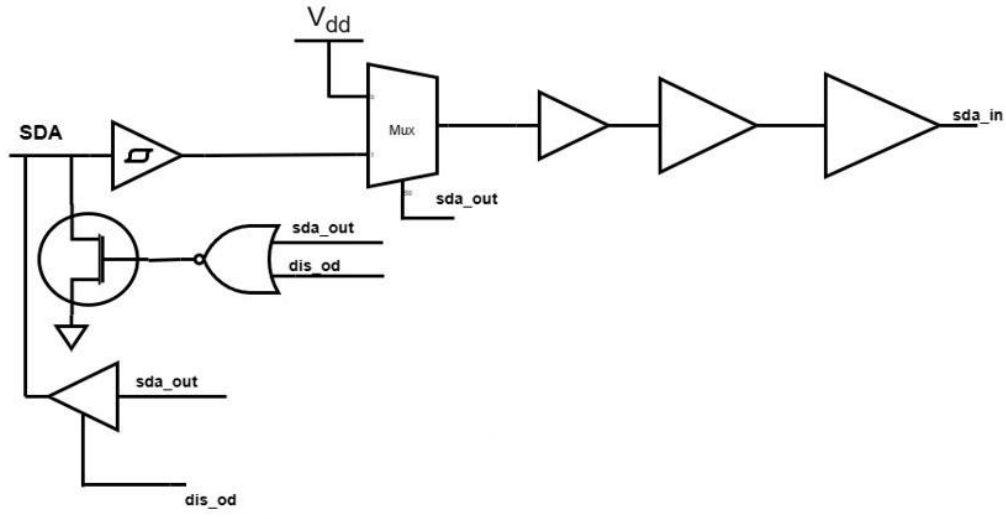

Fig. 4. Schematic of SDA configuration

The input filters schematic [9] contains a selection input, able to block the input signal from being filtered. Otherwise, an internal cell introduces a delay to the input signal and the logic gates forming an SR latch deletes the spikes. The user has the possibility to enable or disable the spikes filtering by means of EN input which serves as selection input for the multiplexer. In I2C mode communication, these input filters must be enabled for preventing SCL and SDA (SDA_IN) with pulse widths smaller than 50 ns to reach the digital core (Fig. 3). In I3C mode communication, which involved higher operating frequencies, these filters are disabled.

This architecture was implemented in a 65 nm CMOS technology. We targeted a 3 V compliant architecture, thus supply voltages of 1.8 V - 3.6 V are used. A digital mixed-signal methodology was used for this design. The digital interface was built with standard cells, through the process of synthesizing the RTL code with Cadence Genus™ technology. This design approach followed the avoidance of internal sampling clock, to be more efficient from area, and current consumption perspective.

4. Results. Discussion

The verification of this design is made by means of digital simulations, digital gate level simulations, Static Timing Analysis, and transistor level - SPECTRE® simulations.

For the Power-On-Reset block simulations, the supply voltages considered were 1.2 V - 3.6 V (Fig. 5). Across a temperature of -40 ºC up to 125 ºC, for all process corners, a minimum value of 1 V and a maximum value of 1.5 V have been obtained. PVT (process-voltage-temperature) mean value of 1.228 V, very close to the 1.2 V target, is proven.

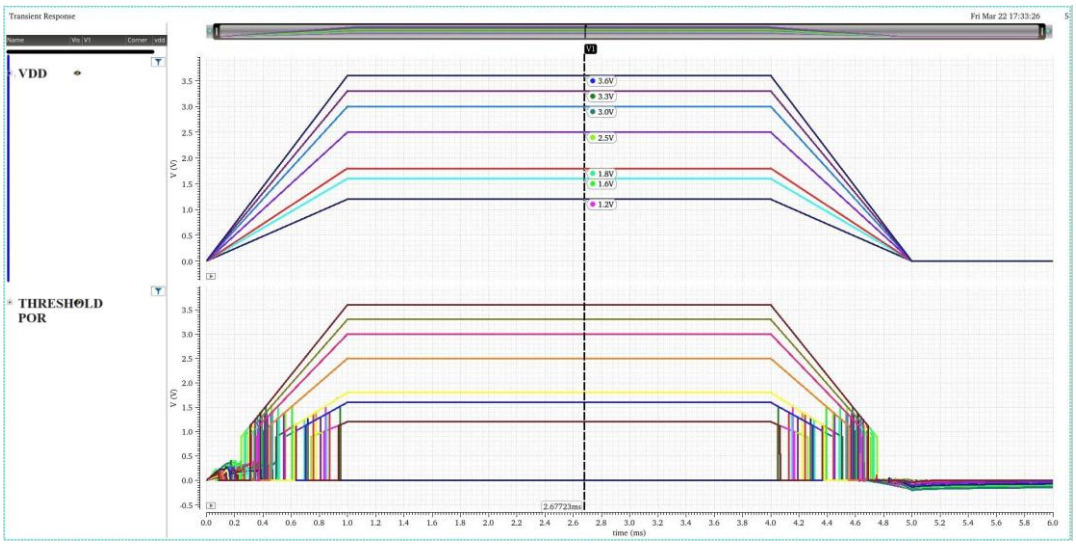

Fig. 5. Waveforms Power-On-Reset Block Simulations

The performance of the input filters is presented in Fig. 6. It is confirmed that the interface does not respond to those input signals received on SDA or SCL having pulse width smaller than 50 ns for voltages between 1.8 - 3.6 V, and a temperature between -40 ºC ÷ 125 ºC, in nominal process corner.

Fig. 7 shows the filter response to a succession of pulses with different widths. The pulses with a smaller duration than 50 ns are ignored.

Fig. 8 depicts an I3C write scenario comprising several instructions for requesting the I3C mode, calling the target device, sending the register address, and the data. The sequence starts with the 0x7E I3C mode call, which is recognized by the controller-dis_od and dis_50n_filter signals are activated (indicated by the left blue arrow in Fig. 8).

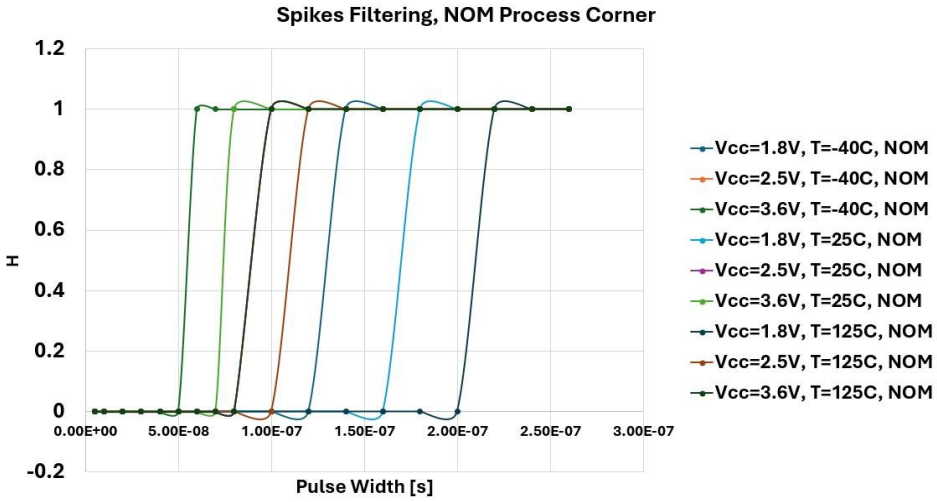

Fig. 6. Input Filters performance: passing signals with widths over 50 ns only

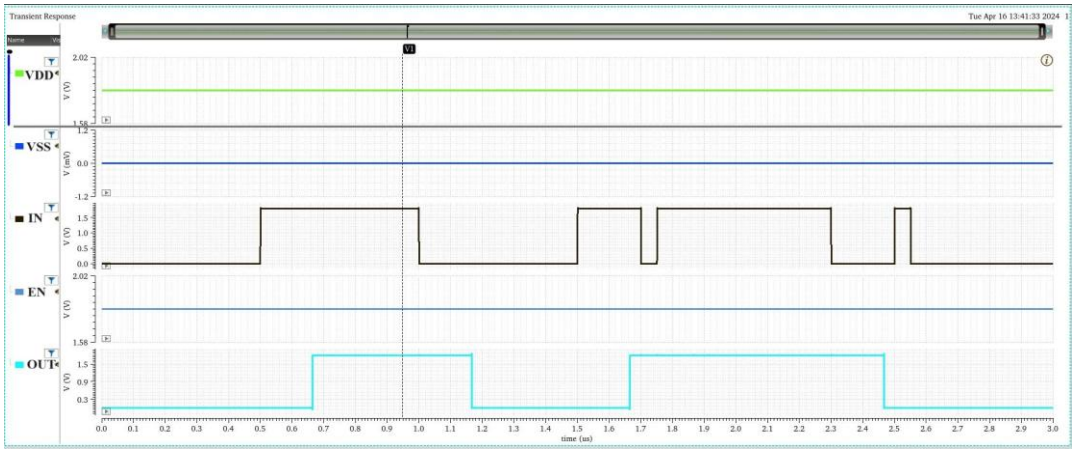

Fig. 7. Input Filters performance: input/output filter waveforms with rejection of below 50 ns signals

The following byte sent by the master contains the interface's address. Consecutively, the address of the internal register is sent, 0x02 which is being acknowledged by the parity check (highlighted in the violet rectangle). Next byte contains the data 0xAA to be written in the addressed register. These were obtained in post-synthesis gate level simulations.

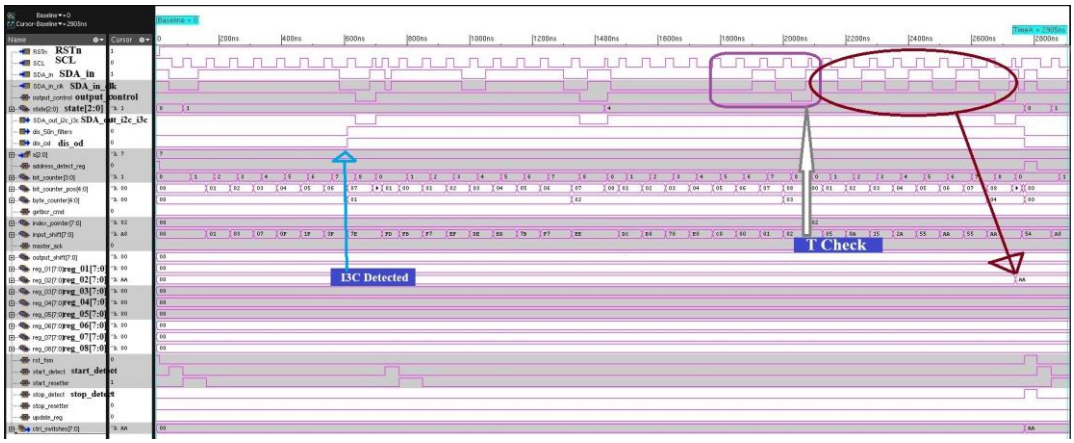

Fig. 8. Digital waveforms I3C mode

Fig. 9 shows the waveforms corresponding to a transistor level SPECTRE® simulation run at block level on the digital controller. Both I3C and I2C read and write were performed. 1.8V and 3.6 V signals, at a temperature of 125ºC, in the fast process corner are shown for SCL, SDA_IN, SDA_out and mode commuting signals, dis_50n_filter or dis_od are depicted (Fig. 9). A write instruction is performed followed by a read of the same addressed register, being noticed how the data byte firstly sent on SDA_IN is transmitted back on SDA_OUT (highlighted with violet in Fig. 9). The simulations waveforms depicted prove the functionality at 13.7 MHz for the digital interface, which guarantees the ability to work at 12.5 MHz as the I3C standard specifies.

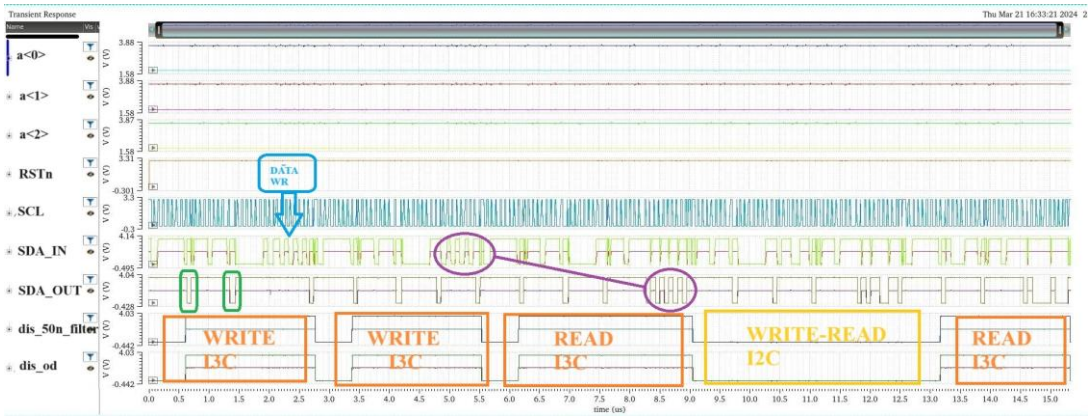

Fig. 9. Waveforms to prove I2C/I3C compatibility

A chip level simulation waveform is shown in Fig. 10 for read and write instructions. By internal activation of dis_od and dis_50n_filter, the automated shift from I2C to I3C communication is detected. This functionality simulation was run for a supply voltage of 3 V, in nominal process corner at 25 °C, showing an I2C operation.

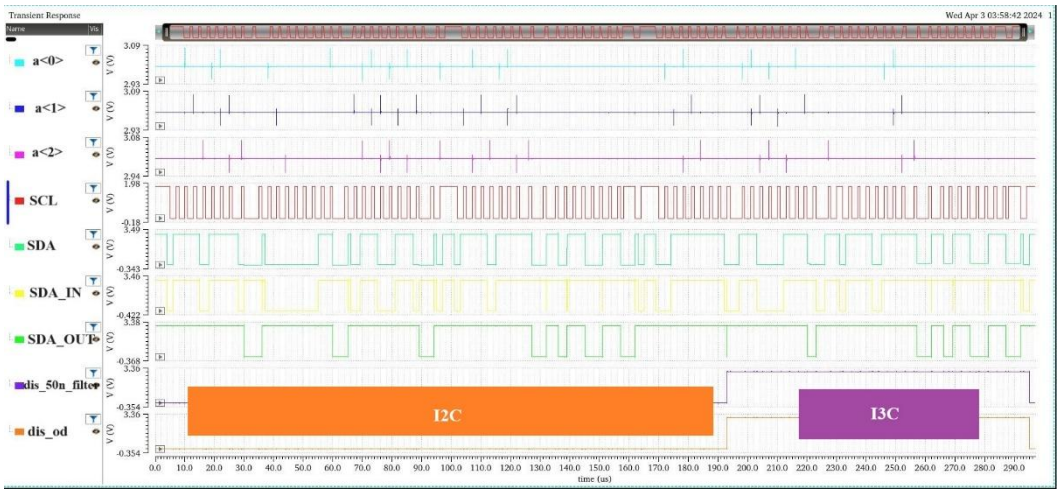

Fig. 10. Waveforms Top Level Simulations

Fig. 11 depicts the layout designed in 65 nm technology, for the proposed digital controller. The logic gates are routed on metal M1, and interconnection between cells is done on metals M2-M3, and M4 – top metal. The area of the digital controller is 16900 μm^2.

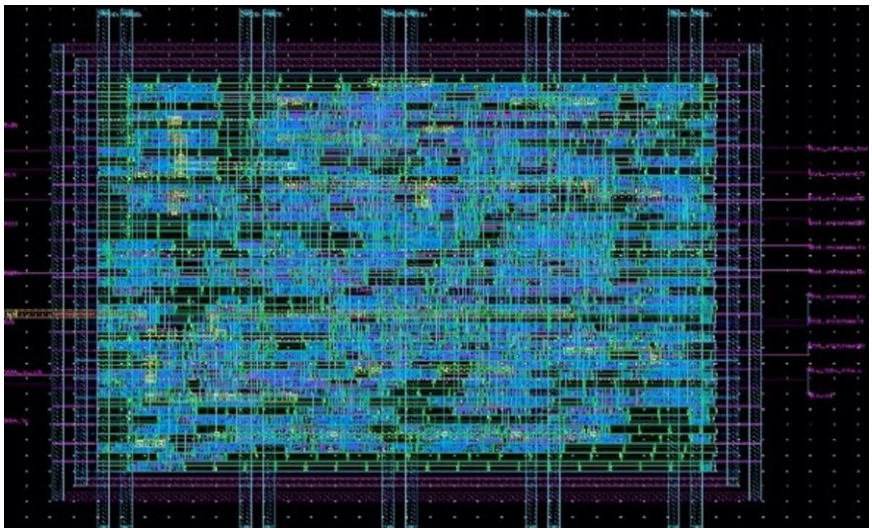

Fig. 11. Layout digital block

Table I shows a literature comparison of the proposed architecture performance with other contributions published in literature papers. Noted is the fact that our architecture has dual compatibility I2C/I3C. This circuit can work with a range of voltages as low as 1.8 V. The active interest in I2C circuits is shown by the efforts of getting architectures able to work with low voltages, like 1.8 V. The area we have obtained is slightly increased for the digital block, but it incorporates

main I3C features, involving supplementary logic circuitry. Our circuit was implemented in a 65 nm technology and can operate with frequencies of at least 12.5 MHz – the frequency of I3C standard (higher than I2C frequencies). The entire construction of our controller relied on the interface clock SCL, and we did not implement a digital topology using internal sampling clock given by an oscillator block. The results marked with * refer only to the digital controller.

Table 1

Comparison with academic research papers

Parameter	**ISOCC'17 [10]**	**ICET'23 [11]**	**ISSE'15 [12]**	**ICEICM'21 [13]**	**This Paper**
Protocol	I2C	I2C	I2C	I2C	I2C/I3C
Technology [nm]	180	180	180	40 nm	65 nm
Operating Voltage [V]	1.8	Not mentioned	1.8	0.9	1.8 – 3.6
Frequency	Not mentioned	3.4 MHz	100 KHz	100 MHz	12.5 MHz
Area [μm^2]	5712	14729	Not mentioned	6770	16900 *
No. of Gates	650	285		Not mentioned	403
Current Consumption	87 µA @ 1.8 V	Not mentioned	5.9 µA @ 1.8 V	Not mentioned	106 µA @ 1.8 V *
W/O Sampling Clock	With	Without	With	With	Without

Table II shows a comparison with other I2C or I3C compatible products from the market. Our circuit distinguishes with both I2C/I3C compatibility. The proposed circuit has a current consumption smaller than the I2C circuit in [13] and [15], and higher frequency operation. Unlike [13], [4] and [15] which are 5V designs, our circuit compatible with I3C targets lower voltages as [7] does.

Table 2

Comparison with I2C/I3C commercial pro

Parameter	**[14]**	**[4]**	**[7]**	**[15]**	**This Work**
Protocol	I2C	I2C	I3C	I2C	I2C/I3C
Supply Voltage	2.3-5.5	2.3-5.5	1.8 – single suppl	2.5-6.0	1.8-3.6
Data Rate	1	1	12.5	0.1	12.5
Consumed Current	175 µA @ 100 kHz	80 µA @ 100 kHz	Not mentioned	200 µA @ 100 kHz	106 µA @ 12.5MHz block simulation

6. Conclusions

An I2C digital controller upgraded with the main features of Single Data Rate I3C protocol was proposed. Frequencies up to 12.5 MHz for voltages ranging between 1.8 V ÷ 3.6 V, across a temperature range of -40 ºC ÷ 125 ºC were proven in both digital and transistor level simulations. An average current consumption of 106 µA at 1.8 V is typically observed in simulations (Nominal process corner, temperature of 25 ºC). The schematic and layout were designed into a 65 nm CMOS technology. An area of 16900 μm^2 is obtained.

To fully verify the robustness of the digital core block, it was integrated together with input/output structures, power-on-reset block and input filters into a chip. Transistor level chip level simulations prove the dual I2C-I3C functionality. Design and verification of an I2C digital core with I3C features compatibility are demonstrated.

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