MEANS OF IMPROVING THE HIGH FREQUENCY ELECTROMAGNETIC INTERFERENCE IN POWER SWITCHING APPLICATIONS

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The paper presents an improved power switch control mechanism suitable for automotive and industrial applications. A negative feedback control is described to enhance the electromagnetic compatibility of the integrated switch with the surrounding environment.

A new and improved way of controlling the shape of the gate charge current is implemented in order to decrease the electromagnetic interference of the power switch at high frequency in PWM switching systems.

Computer simulated results for the state of the art implementation and the new improved configuration are compared to prove the efficiency of the new architecture.

Keywords: Power, switch, feedback, edge control, gate current.

1. Introduction

Intelligent switches or smart power switches are nowadays more and more used to control electric power transfer [1], [2]. In both Automotive and Industrial applications the interest of replacing relays with semiconductor integrated circuits has grown a lot due to the ability of the electronic switch to protect both the load and itself. These integrated switches are nowadays called intelligent because a great deal of protection functions is implemented within the IC.

2. Application

Usually the amount of power that needs to be delivered to a load in a certain amount of time is controlled by the use of *PWM*. This implies a very important trade-off that a designer or an application engineer has to keep in mind:

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In order to minimize the energy loss at the on and off switching, the engineer minimizes the turn on and off times as much as possible; this is shown in Fig.1. The trade-off is an increased electromagnetic compatibility of the switch with the close environment. Fast transients on the supply line, because of long wires that possess high inductance, are now disturbances for the other circuits in the vicinity and more than that for the circuits supplied from the same power source. This is explained by equation 2.1 and 2.2 which is the envelope of the amplitudes of the Fourier expansion coefficients due to a trapezoidal wave signal.

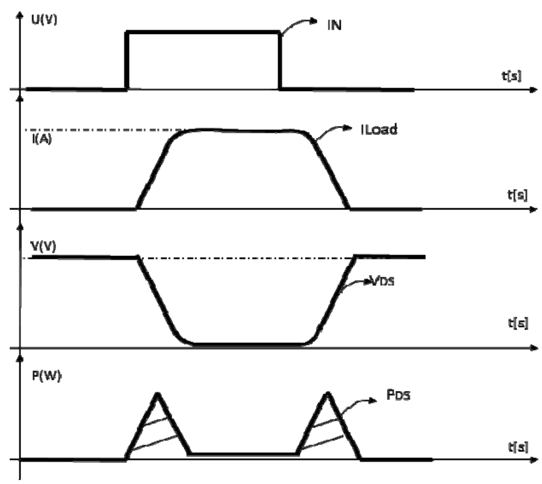

Fig.1. Power loss

The proof of this comes from the *Fourier series* of the signal and is accurately described and calculated in [3], [4].

– (2.1)

– (2.2)

The envelope in Fig.2 is flat until a frequency determined by the duty cycle τ of the switching waveform. This frequency is lower than the fundamental because of the π term at the denominator.

— (2.3)

The frequency where the envelope starts to drop with *40dB/dec* is controlled by the rise and fall times $\tau_F = \tau_R$ of *PWM* signal, so basically the maximum energy that the application can lose.

— (2.4)

The high frequency harmonics need to be reduced as much as possible because in automotive applications noise in the AM and FM band is undesirable for the end user [5].

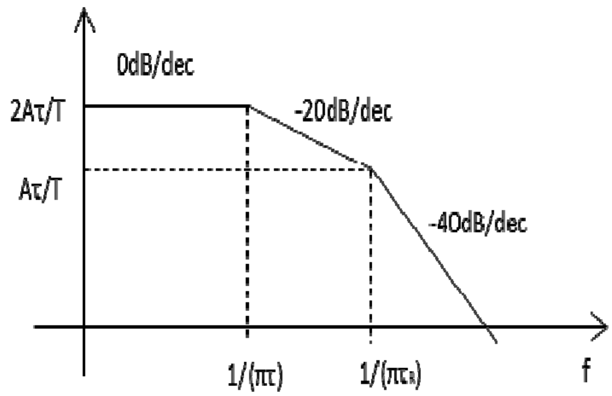

Fig.2. Spectral envelope of trapezoidal waveform

One of the reasons for electromagnetic emissions at frequencies higher than *f2* is the edges of the switching wave form.

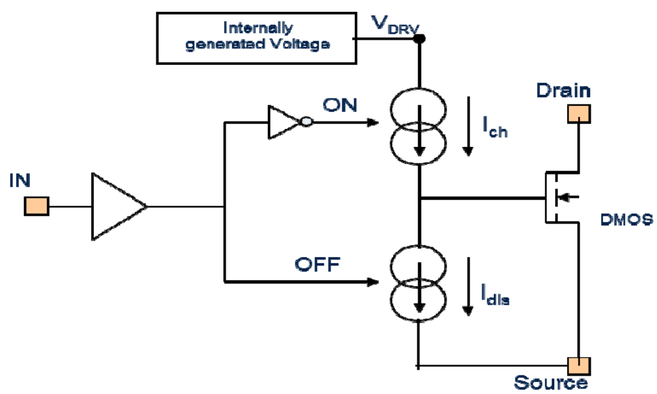

Fig.3. Classic gate control mechanism

These corners are not normally controlled an depend only on the properties of the power transistor itself – the second order behavior of the drain current due to the gate to source voltage of the dMOS switch.

The first approach in order to improve the high frequency EMC spectrum is to use instead of switch control, constant current sources to charge and discharge the gate of the transistor [6], [7]. The state of the art from Fig.3 is used in many of today's applications and has the advantage of simplicity and easy PWM control by turning on and off the current sources.

3. Implementation

This paper presents a new and improved way of controlling the shape of the gate charge current to decrease the electromagnetic interference at high frequency. The first consideration is the need for matched charge and discharge currents. This will make sure that the emissions due to rise and fall times are kept at minimum.

The additional consideration suggested by this paper is to further control the shape of the charge and discharge gate current. This is presented in Fig.4. By forcing an additional current that starves the current source more at the beginning of the turn on and off and then less and less, a new rounded charge and discharge current is thus obtained. The resulted gate current will make an exponential behavior in the output current waveform, in the area where the high frequency harmonics are most influential, which according to the signal theory should give a better electromagnetic spectrum (low amplitude harmonics).

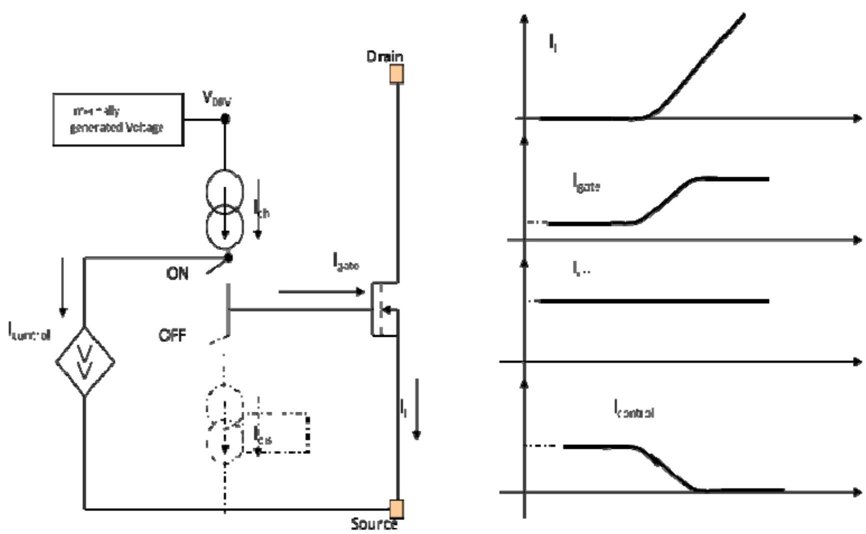

Fig.4. Gate current

The way of controlling this additional current and correlate its effect exactly at the time required to control and round the shape of the output signal is done by means of negative feedback. The feedback takes information from the output and feeds it at the gate adjusting accordingly the required control current. The implementation that accomplishes this is shown in Fig.5. The internal circuits are supplied by an internal generated voltage source. This power supply voltage is regulated to keep its electromagnetic influence at minimum. The current sources are cascoded to provide good noise rejection and supply ripple immunity. The dominant high impedance node is found at the gate of the power switch where both high *ac* resistance and capacitance exist. This is used also as compensation node to achieve loop stability. No compensation capacitor is needed because the large gate source capacitance is used to create a dominant pole at a low enough frequency.

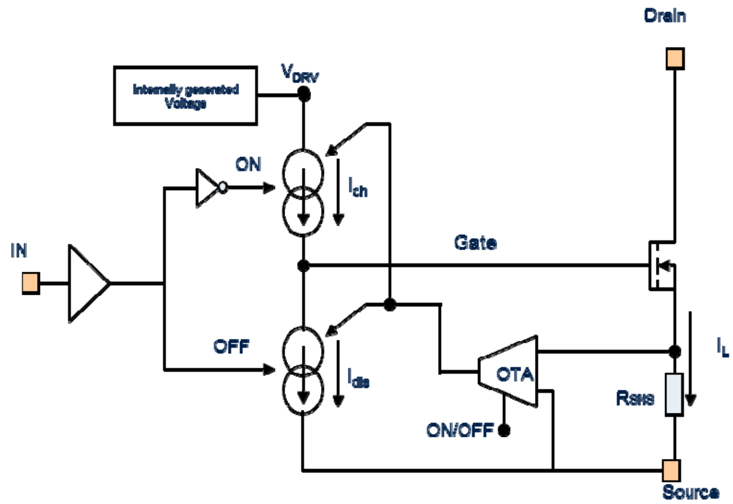

Fig.5. Feedback implementation

The exponential behavior of the gate current can be described following the concept from Fig. 5.

(3.1)

Where *β* is a parameter dependent on the size and process of the DMOS transistor, and *Vth* is the threshold of the device.

(3.2)

t being the time in which the *Cgs* gate capacitance is charged by the current *Igate*.

(3.3)

With Rsns being the sense resistor and gm being the trans-conductance of the OTA.

— (3.3)

Equation 3.4 confirms the expected exponential behavior of the gate current by showing that the gate current is being proportional with the square of *Igate*.

Because in usual applications the power switch can be either high side or low side this paper is presenting a method that can fit both configurations. So either the drain of the nMOS can be connected to a power supply or the source to a power ground plane. An nMOS is usually preferred in power applications because of the better R_{ON} compared to the complementary pMOS thus the area gain will provide lower silicon costs. A series feedback resistor is used as a current sense and the voltage thus obtained is generating via an operational trans-conduction amplifier the feedback current that is added to the charge/discharge gate current. The series resistor is in this case implemented in the source of an nMOS transistor thus simplifying the compensation of the loop. If the sense resistor would be implemented in the drain an additional high impedance node will give rise to a pole because the nMOS will act as a common source amplifier and not as a simple voltage follower. Also and additional on/off signal that controls the feedback current is implemented in order to disconnect the edge rounding circuit when the output voltage has changed by a certain amount. This is done in order to make the control circuit independent of the load current required by the application.

4. Simulation and Results

A circuit was designed and implemented in a BCD process to prove the theoretical approach presented can minimize the electromagnetic emissions to the environment at high frequencies. In Fig.6 the real implementation is presented and the explanation of how the actual charge discharge control mechanism is functioning at transistor level. A current sense finger of the DMOS is supplying the I_s current to the sense resistor R_s. This is done to minimize the power lost in the sens resistor. The resulted voltage is translated into a current by the OTA. The current supplied by the OTA is ten times smaller to accommodate to practical values of I_1. It is imperative that I_1 with I_2 are matched, and I_1 kept smaller than I_2. When the gate voltage is not high enough to turn on the DMOS the gate charging current is given by the difference between I_2 and I_1 multiplied by the mirror factor. As soon as the DMOS turns on I_s is activating the loop that starts subtracting current from I_1 reference current.

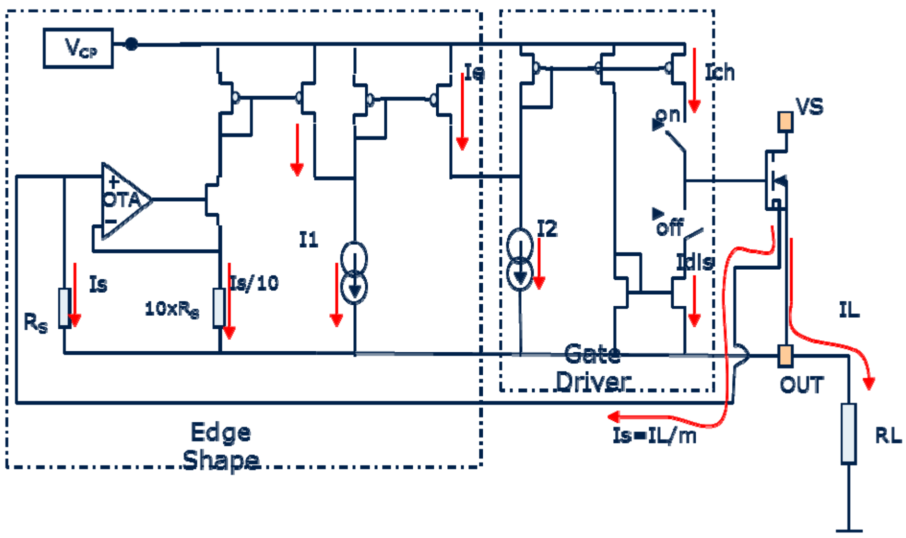

Fig.6. Transistor level Implementation

This means that I_e is starting to decrease from its maximum value given by I_1. The moment that I_s is high enough I_e drops to zero and the charging current limits itself to a constant value given by I_1. In the off phase the current mirror in the Gate Driver is doing the same thing described above. This mechanism is making the steep corners of the wave shape more round thus reducing the overall emissions given by the switching of the DMOS.

In Fig.7 a simulation result comparing both the state of the art and the improved wave shape of the output is shown.

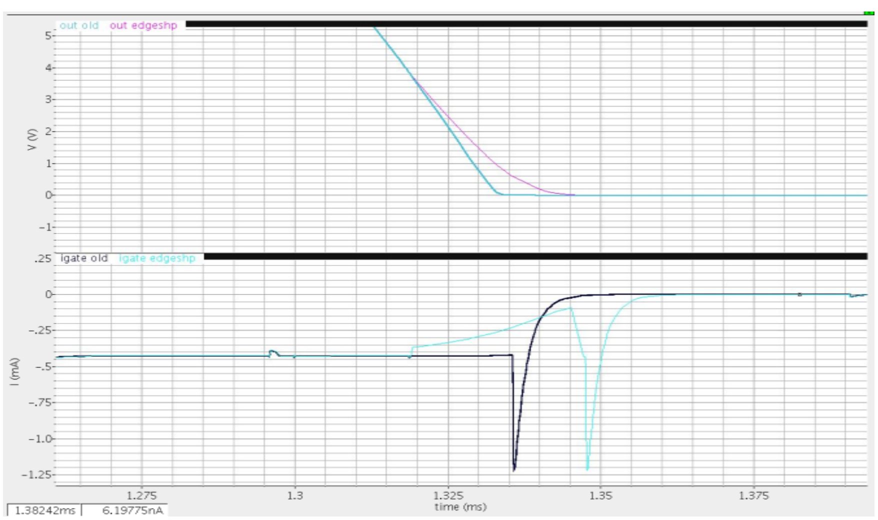

Fig.7. Discharge gate current

The simulation demonstrates a smoother output shape if the gate current is controlled by the feedback network, in respective with only constant current drivers. The figure reveals the discharge part of the switching waveform. In the lower part the gate current from the state of the art with constant current sources and the one used with the mechanism of controlling and rounding it are presented. The jump in the gate current after the V_{DS} voltage is close to zero is implemented in order to discharge the gate capacitance of the power switch after V_{GS} has dropped below the threshold of the device. This is needed to make sure that the power switch is firmly off.

A fast Fourier transform simulation is done on the I_L current wave form to measure the differences in the electromagnetic emissions of the classical implementation and the architecture proposed by this paper. In Fig.8 the two results are compared. The lower waveform is the result with the improved circuitry that makes the edges of the switching wave signals to be smoothened and thus give a better EMC performance of the circuit. It can be seen that starting from frequencies in the order 10 KHz to frequencies of 1 MHz the emissions are lower with a maximum value of 15 dB. The simulation is stopped above 1 MHz because emissions due to other additional circuitry like charge pumps, need to be taken into account and are not the purpose of this paper.

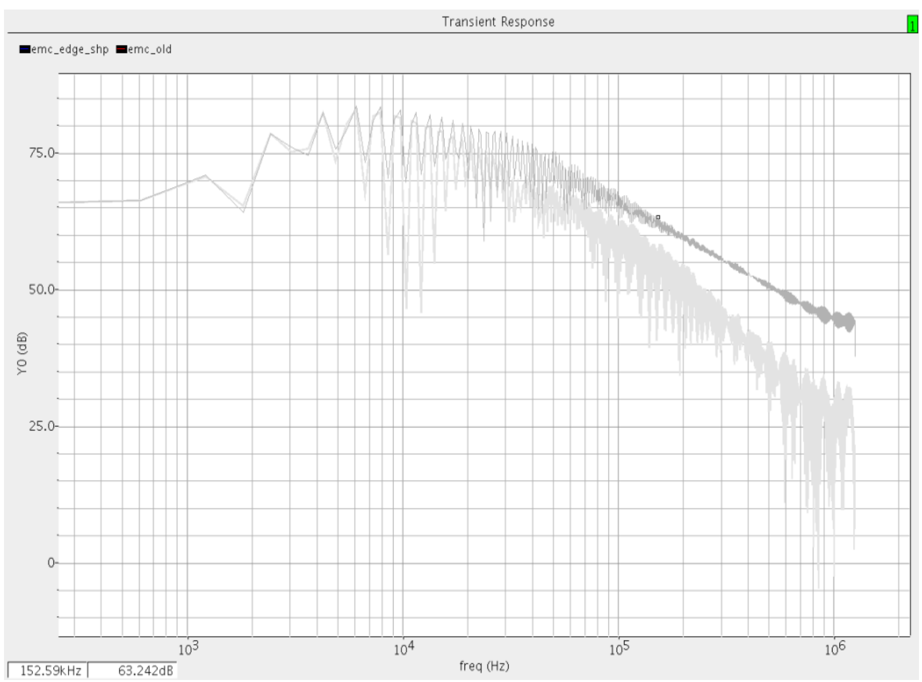

Fig.8. FFT simulation

A clear improvement is observed in the high frequency area (hundreds of KHz). The envelope of the coefficients of the Fourier transform has lower values than in the classical implementation and thus the papers proves that the new implementation provides better electromagnetic compatibility.

At the same time, based on the CISPR-25 level 3 automotive standard shown in Fig.9 and described in [8] and [9] we can conclude that the system proposed fits the hard requirements imposed by the industry.

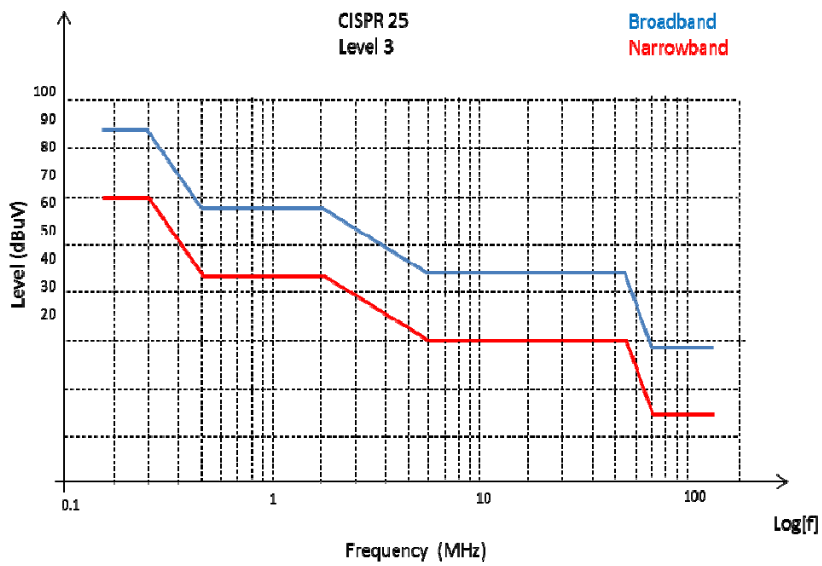

Fig.9. CISPR-25 level 3 automotive EMC standard

5. Conclusions

This paper has presented an improved architecture that controls the gate current of a DMOS power switch in order to decrease the electromagnetic emissions in the surrounding environment. The simulations prove that the new implementation can provide better results than the state of the art used in the industry. The results obtained show an improvement of 15dB compared with the classical implementation. The implementation is useful for both high side and low side switches used in PWM switching applications, [10-12]. The results presented fit with the automotive standards and pass the industry required tests and measurements. The main advantage resulting from the electromagnetic emissions improvement brought by this paper is the possibility to decrease the size of the filtering capacitors used together with this kind of switching applications.

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