LOW POWER HIGH SPEED FinFET BASED DIFFERENTIAL ADDER CIRCUITS WITH PROPOSED CARRY/CARRYBAR STRUCTURES

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This paper proposes twelve differential full adder circuits. They are designed by using six SUM/SUMBAR circuits for SUM function and two proposed CARRY/CARRYBAR structures for CARRY function. Power and energy efficient circuits are proposed utilizing only a smaller number of transistors minimum sized to generate strong output strong levels. They have less delay since their critical path is having only three transistors of minimum size accordingly. The fundamental benefit from the two CARRY/CARRYBAR proposed circuits are the levels of evenness in the logic that eases the layout process. The driving capability of these circuits is good because these designs produce full rail to rail voltage swing at the outputs. Another advantage of these designs is that they could produce differential outputs with lesser number of transistors at low voltages and high frequencies which are used for fault detection. The proposed CARRY/CARRYBAR and Full adder circuits are simulated in a reasonable condition using FinFET 18 nm and MOSFET 45 nm technology files with multiple voltages from +0.4V to +0.6V and +0.4 V to +1.2 V respectively. The simulated outcomes demonstrate that the proposed designs have lesser propagation delay, total power dissipation and PDP.

Keywords: FinFET, Low Power, SUM/SUMBAR logic, XOR/XNOR logic, Driving capability, Full Swing, Full adder, Sum/Sumbar, Carry/Carrybar, Pass Transistor Logic (PTL).

1. Introduction

The CMOS technology is facing the problem of gate leakage currents and sub-threshold currents at submicron threshold region. These problems can be overcome using suitable substitutes like the double gate FinFET devices. This device can lower gate leakage and reduce short channel effects as it has stronger

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gate control. Owing to these features, FinFET avails itself of the benefit of speed, size and work at sub threshold regions. Figure 1 illustrates the top view of the Double Gate-FinFET construction [1] and its representation. FinFETs with independent gates are more flexible and easier to use and hence they are incorporated in the design. As FinFETs provide lesser flicker noise levels at lower supply voltages and higher drive currents they are therefore suited for digital and analog applications [2].

Over the period, many designs on CMOS direct three input XOR and XNOR logic circuits [3-16] have been innovated to ameliorate the operation of the gate compared to the cascaded designs in which a three input XOR/XNOR logic gate is obtained by cascading two 2-input XOR/XNOR logic gates. XNOR logic gate is obtained by adding one inverter at the output of the XOR logic gate. However, all these cascaded designs have higher transistor count thus causing in extra power consumption [8-24]. These direct three input XOR logic functions are used as Sum function for Full adder [25-43].

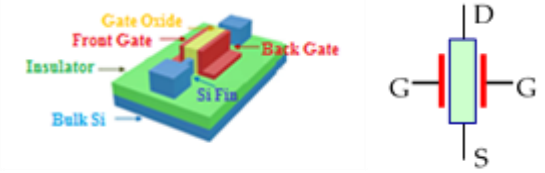

Fig. 1. (a) Top view of double gate FinFET structure [1]; (b) Symbol

This paper presents twelve structures of full adders using differential direct three in-put XOR/XNOR logic gate designs for SUM/SUMBAR functionality and proposed differential CARRY/CARRYBAR designs for carry function of full adder, which have low power dissipation as well as high performance, requiring only 14, 12, 10 and 8 transistors for their logic design implementation which are simulated by using 18nm FinFET technology file.

2. Proposed work

A. SUM/SUMBAR Logic Structures for Full adder

This section describes the SUM/SUMBAR logics of full adder using six structures of XOR/XNOR direct three input logic gate circuits. In this paper, PTL logic based XOR/XNOR circuits for SUM/SUMBAR logic are used as PTL logic provides less area, less propagation delay and less power consumption. In turn, each of the proposed circuits cab be able to realize with TGL logic, although the silicon area becomes doubled. To overcome the voltage loss problem of PTL, inverters connected back to back are used as part of de-sign, the proposed designs

themselves. So, the SUM/SUMBAR gate circuits use the pass transistor logic along with inverters connected back-to-back.

Figure 2 to Figure 7 illustrates the circuit schematics of the three input logic gates using PTL and back-to-back loop connection of two inverters SUM/SUMBAR structures. Full logic swing for both differential outputs can be provided by these circuits using only 14, 12, 10 and 8 transistors respectively considering the availability of differential inputs.

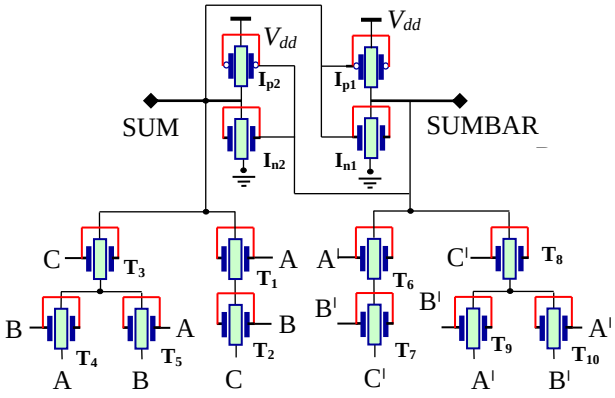

Fig. 2. SUM/SUMBAR Structure-1

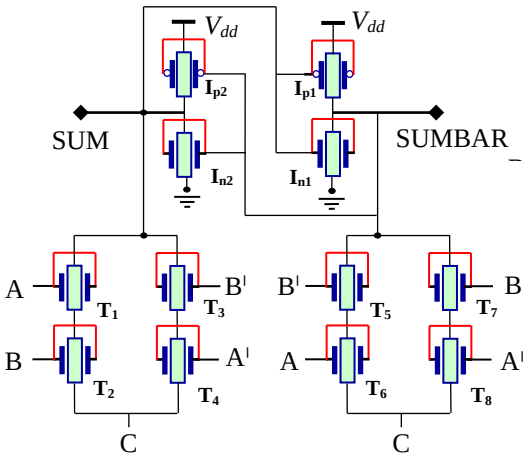

Fig. 3. SUM/SUMBAR Structure-2

Perfect rail to rail swing is the output of all the proposed circuits for every input combination. A, B, A' and B' are used as control signals in the tructure-2 to structure-6 (from Fig. 3 to Fig. 7), and input C or C' is passed to SUM/SUMBAR outputs depending on the control signal values, where as in structure-1 (Fig. 2), all

inputs A, B, C, A', B' and C' are used as both control signals and passing signals to outputs.

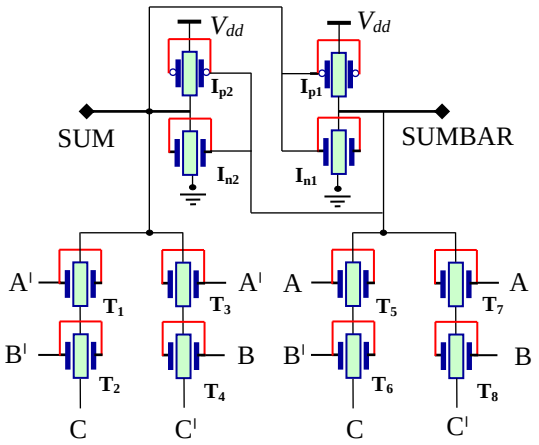

Fig. 4. SUM/SUMBAR Structure-3.

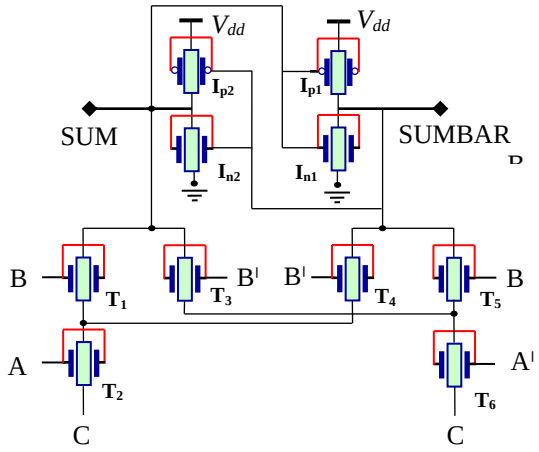

Fig. 5. SUM/SUMBAR Structure-4.

As for the operation in all the proposed circuits, only two switches and one loop is present in the critical path, hence the proposed structures are considered high performance designs. Added benefit in these structures is their low power consumption as they have few transistors in switched ON state in each pattern of the input and that too of least sized each.

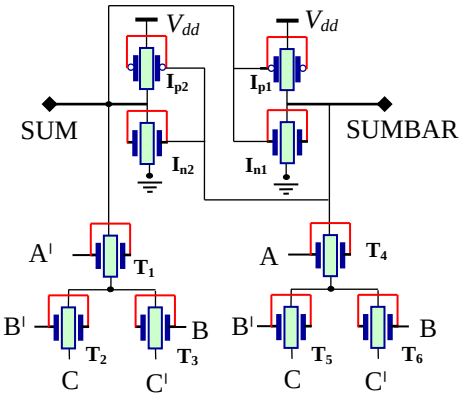

Fig. 6. SUM/SUMBAR Structure-5.

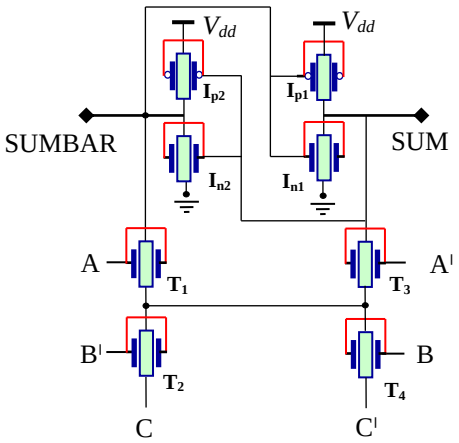

Fig. 7. SUM/SUMBAR Structure-6.

The structure-6 which is demonstrated in Fig. 7 saves the silicon area alongside power. It has the good driving capability too because it obtains full swing at the output. In the structures 2, 3, 4, 5 and 6, for any input pattern only two switches (pass transistors) turn ON and two transistors (either the combination of In1 and Ip2 or the combination of In2 and Ip1) from the inverters turn ON, so totally 4 transistors are switched ON for any inputs and in this, power dissipation is less. The critical path consists of a maximum of three transistors, so propagation delay is too less in all these proposed circuits. The SUM part of the full adder is implemented using SUM/SUMBAR functions, is directly obtained by XOR/XNOR operation of three inputs.

B. CARRY/CARRYBAR Logic Structures for Full adder

For the carry part of the full adder, two new structures are proposed. For the proposed structure-1, carry function is demonstrated in Fig..8. It comprises of 8 pass transistors with two inverters back to back connection. So both CARRY and CARRYBAR functions give full swing. For the proposed structure-2, carry function is presented in Fig..9. It contains 6 pass transistors, two inverters, with back-to-back connection. This structure also produces both CARRY and CARRYBAR outputs at full swing.

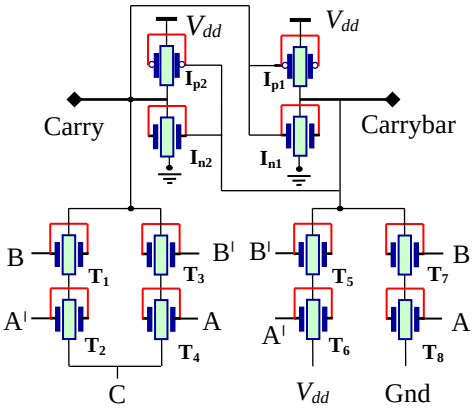

Fig. 8. Proposed CARRY/CARRYBAR Structure 1

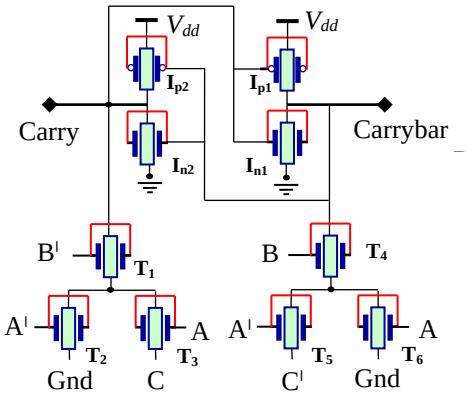

Fig. 9. Proposed CARRY/CARRYBAR Structure 2

C. Full adder logic structures

This paper proposes twelve full adder circuits using six structures for SUM/SUMBAR function and two structures for CARRY/CARRYBAR generation. The sum function uses exclusive-OR operation of inputs. Fig. 2 to Fig. 7 are used for the SUM/SUMBAR function generation. Fig. 8 and Fig. 9 are used for CARRY/CARRYBAR generation. Using these Sum and Carry structures, adders are proposed which are listed in Table 1. Fig. 10 represents the full adder structure proposed. The outputs of all full adders are full swing and produce both differential outputs simultaneously.

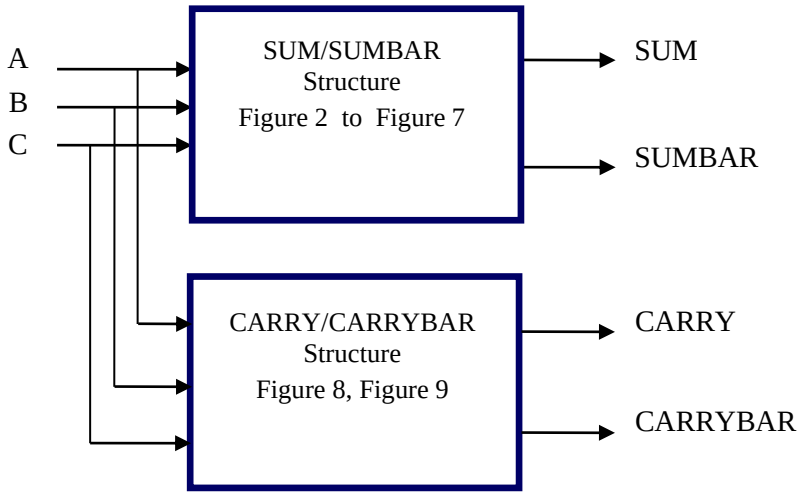

Fig. 10. Proposed Adders structure

Table 1

Proposed Full Adder

S.No	Proposed Adder	SUM Structure	Carry structure
1	Proposed Adder 1	Figure 2	Figure 8
2	Proposed Adder 2	Figure 2	Figure 9
3	Proposed Adder 3	Figure 3	Figure 8
4	Proposed Adder 4	Figure 3	Figure 9
5	Proposed Adder 5	Figure 4	Figure 8
6	Proposed Adder 6	Figure 4	Figure 9
7	Proposed Adder 7	Figure 5	Figure 8
8	Proposed Adder 8	Figure 5	Figure 9
9	Proposed Adder 9	Figure 6	Figure 8
10	Proposed Adder 10	Figure 6	Figure 9
11	Proposed Adder 11	Figure 7	Figure 8
12	Proposed Adder 12	Figure 7	Figure 9

3. Results

Using 18 nm Cadence FinFET technology all the proposed designs were simulated at supply voltages +0.4 V, +0.5 V and +0.6 V respectively from 1MHz to 200MHz frequency. And to compare the proposed designs with the candidate designs, proposed adder 1 to proposed adder 12 were also simulated using Cadence 45 nm MOSFET technology from +0.4V to +1.2V voltages. Output swing of the proposed designs is noticed through the simulations carried out with respect to supply voltages. The transient response of SUM/SUMBAR designs is displayed in Figure 11, and it is to be noted that the output at full swing. The transient response of Figure 8 and 9 is displayed in Fig. 12 and it is observed that both CARRY/CARRYBAR outputs are at full swing. The transient response of proposed full adders is shown in Fig. 13. It shows that both outputs are at full swing. All the SUM/SUMBAR transient response, CARRY/CARRYBAR transient response and full adders transient response are the same, so to avoid the repetition, it is shown only for SUM/SUMBAR structure 6 and CARRY/CARRYBAR structure 2 and proposed adder 12 in Figs. 11, 12 and 13 respectively. Table 2 shows the aspect ratios of transistors in the proposed adder 1 to proposed adder 12. In all the proposed adders, the transistors in inverters I_{p1}, I_{p2}, I_{n1} and I_{n2} used width of 0.02 um and all other pass transistors from T_1 to T_{10} used width of 0.2um.

Table 2

Aspect ratios of transistors in Proposed Full Adders

S.No	Proposed Adder	Width (W) of Transistors in Sum Structure	Width (W) of Transistors in Carry structure
1	Proposed Adder 1	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_{10} – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
2	Proposed Adder 2	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_{10} – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um
3	Proposed Adder 3	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
4	Proposed Adder 4	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um
5	Proposed Adder 5	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
6	Proposed Adder 6	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um
7	Proposed Adder 7	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
8	Proposed Adder 8	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um

9	Proposed Adder 9	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
10	Proposed Adder 10	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um
11	Proposed Adder 11	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_4 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_8 – 0.2um
12	Proposed Adder 12	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_4 – 0.2um	I_{p1}, I_{p2}, I_{n1} and I_{n2} – 0.02um T_1 to T_6 – 0.2um

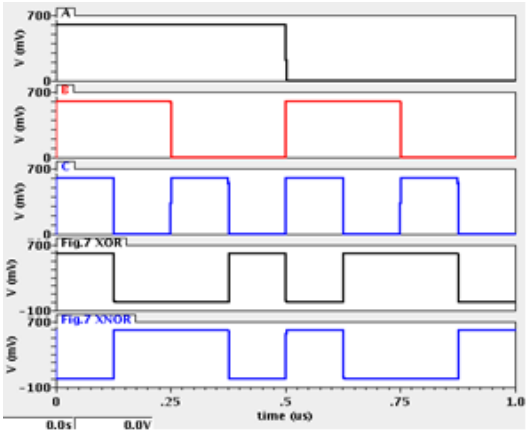

Fig. 11. Transient analysis of SUM/SUMBAR Structures shown in Figure 2 and Figure 7

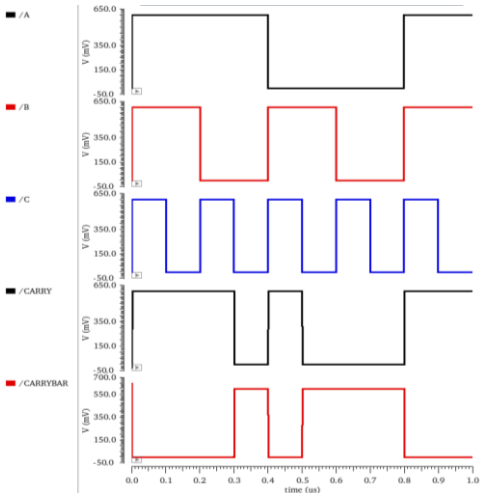

Fig. 12. Transient analysis of CARRY/CARRYBAR structures shown in Figure 8 and Figure 9

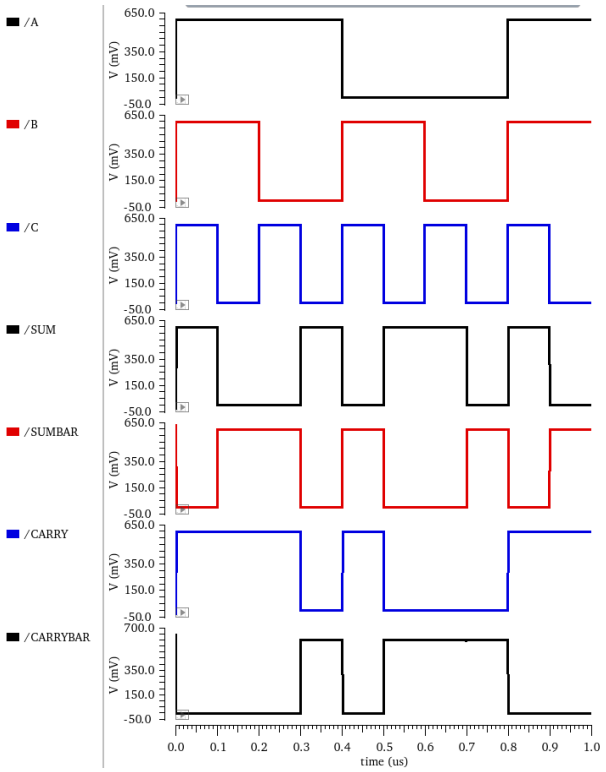

Fig. 13. Transient analysis of Proposed adder shown in Figure 10

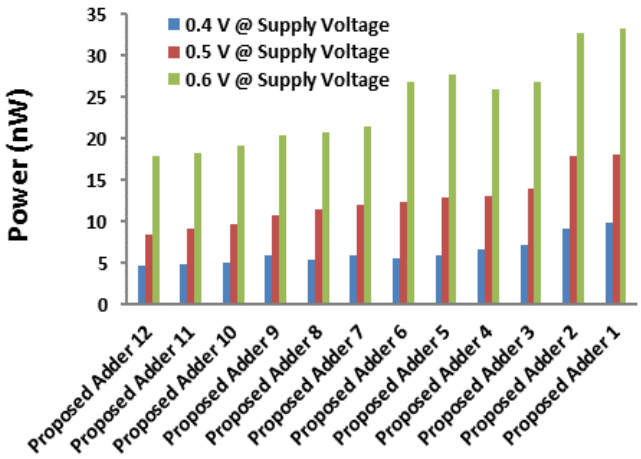

Fig. 14. Power of Full Adder Cells (nW) of FinFET Version

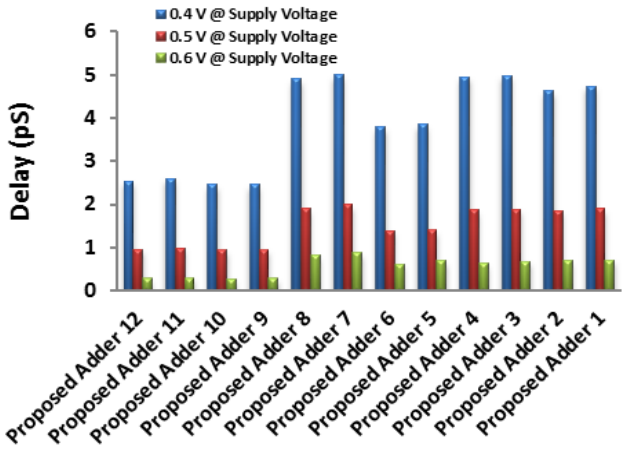

Fig. 15. Delay of Full Adder Cells (ps) of FinFET Version

The power dissipation and transmission delay of all the proposed FinFET based full adders is shown in Figure 14 and Figure 15 at different voltages. It is observed that all the proposed adders have less power and delay and among all the adders proposed, adder 12 has the least power dissipation and delay. Figure 15 shows that PDP values of proposed adder 12 is less among all proposed adders. Table 3 and Table 4 show the comparison of propagation delay and power dissipation of all the proposed MOSFET based full adders along with 21 existing full adders. From Table 3 and 4, it is shown that delay and power values are less for all proposed adders, among which proposed adder 12 has the least values. Figure 17 shows that PDP values of proposed adder 12 is less among all proposed adders and existing adders. Table 5 shows the power, delay and PDP comparison of 4bit RCA implementation using proposed adder structures.

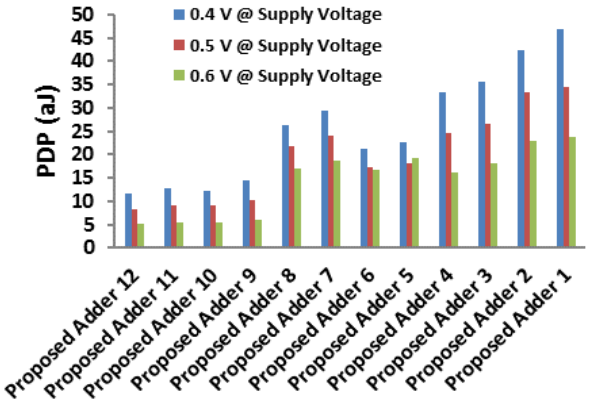

Fig. 16. PDP of Full Adder Cells (aJ) of FinFET Version

Table 3

Delay of Full Adder Cells (nS) @ MOSFET Version

Circuit	0.4 V @ Supply Voltage	0.8 V @ Supply Voltage	1.2 V @ Supply Voltage	Output
Proposed Adder 12	0.3988	0.0899	0.0283	Differential
Proposed Adder 11	0.3891	0.091	0.0285	Differential
Proposed Adder 10	0.4201	0.11092	0.0392	Differential
Proposed Adder 9	0.421	0.1112	0.0304	Differential
Proposed Adder 8	0.5441	0.1802	0.04567	Differential
Proposed Adder 7	0.5541	0.1819	0.04567	Differential
Proposed Adder 6	0.4413	0.1182	0.041559	Differential
Proposed Adder 5	0.4513	0.1282	0.042577	Differential
Proposed Adder 4	0.4497	0.1211	0.04574	Differential
Proposed Adder 3	0.453	0.1286	0.040597	Differential
Proposed Adder 2	0.5617	0.1792	0.05618	Differential
Proposed Adder 1	0.5732	0.1828	0.05645	Differential
Scalable Hybrid [42]	0.5238	0.0657	0.0253	Single
GDI D3 [41]	0.7083	0.0905	0.0397	Single
GDI D2 [41]	0.5476	0.0773	0.0286	Single
GDI D1 [41]	0.5998	0.0988	0.0318	Single
Hybrid 6 [40]	0.6834	0.0814	0.0351	Single
Hybrid 5 [40]	0.6975	0.0968	0.0439	Single
Hybrid 4 [39]	0.6753	0.0816	0.0387	Single
Hybrid 3 [38]	0.8118	0.1013	0.0486	Single
Hybrid 2 [37]	F	0.2314	0.0696	Single
Hybrid 1 [36]	0.9324	0.1891	0.0602	Single
New-HPSC [35]	0.9985	0.1936	0.0715	Single
SRCPL [34]	0.8696	0.1323	0.0504	Single
DPL [34]	0.8356	0.0919	0.0456	Single
HPSC [33]	F	0.0897	0.0386	Single
14-T [32]	F	0.3856	0.0674	Single
24-T [31]	0.9083	0.1284	0.0659	Single
TFA [30]	0.9575	0.1456	0.0668	Single
TGA [29]	0.8934	0.1397	0.0583	Single
CCMOS [28]	0.8093	0.1258	0.0397	Single

12-T [27]	F	0.4474	0.0676	Single
CPL [26]	0.6121	0.0848	0.0373	Single

Table 4

Power of Full Adder Cells (µW) @ MOSFET Version

Circuit	0.4 V @ Supply Voltage	0.8 V @ Supply Voltage	1.2 V @ Supply Voltage	Transistors Count
Proposed Adder 12	0.1631	0.4242	1.2217	24
Proposed Adder 11	0.1654	0.4293	1.2367	26
Proposed Adder 10	0.3192	0.5945	1.4995	26
Proposed Adder 9	0.3273	0.5875	1.5210	28
Proposed Adder 8	0.4612	0.8302	1.9852	24
Proposed Adder 7	0.4664	0.8684	1.9765	26
Proposed Adder 6	0.3901	0.7022	1.8115	28
Proposed Adder 5	0.3998	0.7054	1.8635	30
Proposed Adder 4	0.4448	0.8006	1.9625	26
Proposed Adder 3	0.455	0.8221	1.9712	28
Proposed Adder 2	0.7008	1.2614	2.6496	30
Proposed Adder 1	0.7083	1.2704	2.7999	32
Scalable Hybrid [42]	0.129	0.48	1.17	22
GDI D3 [41]	0.152	0.61	1.32	21
GDI D2 [41]	0.165	0.63	1.49	22
GDI D1 [41]	0.127	0.46	1.09	18
Hybrid 6 [40]	0.133	0.54	1.35	23
Hybrid 5 [40]	0.146	0.58	1.31	21
Hybrid 4 [39]	0.113	0.44	0.98	16
Hybrid 3 [38]	0.169	0.68	1.53	22
Hybrid 2 [37]	F	0.35	0.94	16
Hybrid 1 [36]	0.269	0.78	2.31	24
New-HPSC [35]	0.217	0.77	2.04	24
SRCPL [34]	0.193	0.7	1.79	20
DPL [34]	0.256	0.87	2.11	22
HPSC [33]	F	0.89	2.09	22
14-T [32]	F	1.12	2.34	14
24-T [31]	0.02	0.76	1.68	24
TFA [30]	0.155	0.61	1.33	16
TGA [29]	0.163	0.64	1.41	20
CCMOS [28]	0.159	0.68	1.91	28
12-T [27]	F	1.2	2.54	12
CPL [26]	0.488	1.72	3.89	32

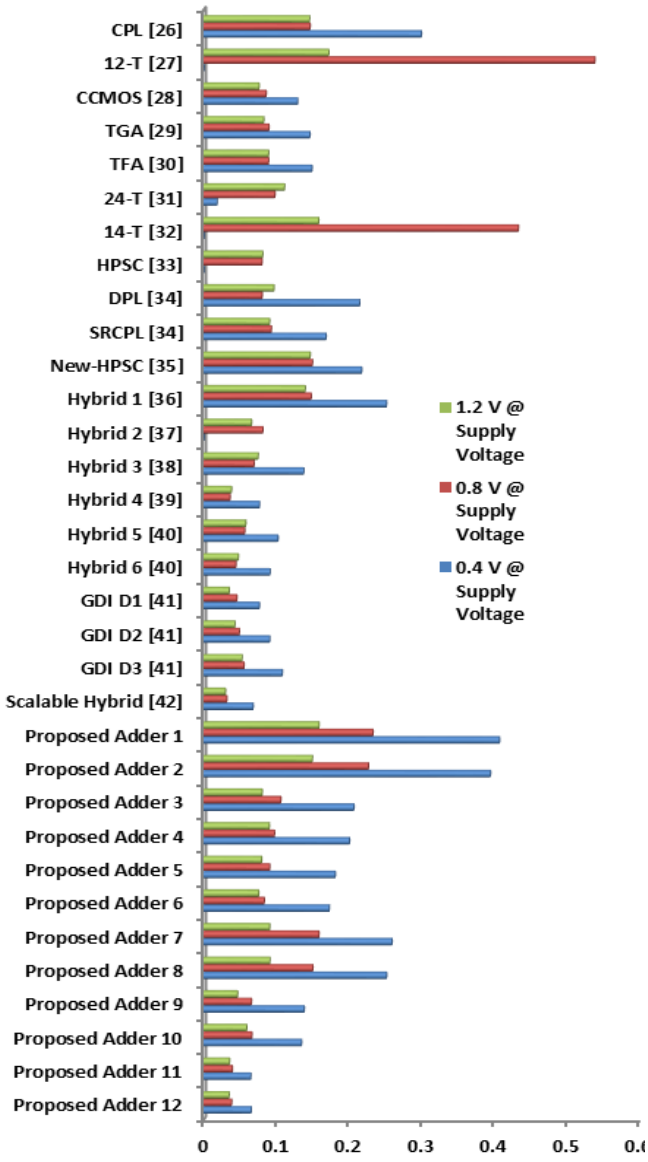

Fig. 17. PDP (fJ) of Full Adders @ MOSFET Version

Table 5

Power, Delay and PDP Values of 4 Bit Adders of FinFET Version

Circuit	Power (nW)	Delay (pS)	PDP (aJ)
Proposed Adder 12	85.37	1.85	157.935
Proposed Adder 11	86.79	1.89	164.033

Proposed Adder 10	91.05	1.76	160.248
Proposed Adder 9	96.99	1.81	175.552
Proposed Adder 8	98.45	5.64	555.258
Proposed Adder 7	101.93	5.44	554.499
Proposed Adder 6	127.97	3.96	506.761
Proposed Adder 5	131.25	4.37	573.563
Proposed Adder 4	123.71	3.91	483.706
Proposed Adder 3	127.21	4.16	529.194
Proposed Adder 2	155.13	4.37	677.918
Proposed Adder 1	158.30	4.45	704.435

4. Conclusions

In this paper, twelve differential full adders have been proposed using six different structures for SUM/SUMBAR logic designs, two different structures for CAR-RY/CARRYBAR logic designs. Based on the transistor count, output voltage swing, power consumption, delay and power delay product, the proposed circuits are compared. The proposed designs are, however, uncomplicated, and simple to layout. They are mostly very apt for high reliability, high speed and low power applications. The proposed adder 12 has a better PDP with less transistor count when compared to all other proposed structures. These circuits are intended to be used often in bio-medical instrumentation systems, communication systems and low voltage processors etc.

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