ADRC-BASED ROBUST DC VOLTAGE CONTROL OF THE GRID-CONNECTED VSC IN DC MICROGRID

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This paper presents a robust DC-bus voltage control method for the grid-connected VSC in DC microgrid. The conventional PI-based DC-bus voltage control with feedforward compensation method is generally employed to improve the disturbance rejection performance of the DC-bus voltage control. However, this method is based on a detailed model and maintains the system stability in a limited range of presupposed operation points. Besides, it also requires an additional sensor for the disturbance measurement. In this paper, the active disturbance rejection control (ADRC) method is employed to improve the robustness of DC-bus voltage control of the grid-connected VSC. The proposed ADRC-based DC-bus voltage control method needs minimal knowledge of model information while achieves good control performance than convention PI-based method. In addition, an adaptive gain-based ESO (AGESO) is proposed for the ADRC to solve the trade-off between disturbance rejection and noise suppression capabilities. Finally, simulation results are presented to verify the performance of the proposed method.

Keywords: DC-bus voltage control, disturbance rejection, adaptive gain, extended state observer.

1. Introduction

Microgrids are proposed as an efficient way to integrate different types of renewable sources and to electrify a remote area [1-3]. As most of renewable sources and electrical loads such as photo-voltaic (PV), battery, computer and electrical vehicle have the characteristic of DC coupling, DC microgrid is a more efficient way for electricity integration and supply despite of the fact that traditional electrical grid is in the form of AC system. In addition, DC microgrid also owns the superiorities of no consideration for reactive compensation, synchronization and frequency stability [4].

DC microgrid can be operated in both grid-connected and standalone modes. Normally, DC microgrid is operated in grid-connected operation and switches to standalone operation when electrical supply from the AC main grid is interrupted. Since there is no utility available, DC microgrid in standalone state requires the capability of autonomous operation. In grid-connected operation, DC

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microgrid can achieve power balance by absorbing and injecting power to the utility electrical grid (AC main grid) via a bi-directional grid-connected converter. Fig.1 shows the structure of a simplified grid-connected DC microgrid. The control of DC-bus voltage is a critical part to maintain power balance and thus voltage stability of the DC microgrid without costly energy storage system. From the DC-bus voltage control point of view, the whole DC microgrid can be regarded as a power load. Load variations in the DC microgrid will create dynamic power disturbance to the grid-connect VSC, which may cause severe fluctuation on DC-bus voltage if not well compensated [5]. Therefore, the robustness of the DC-bus voltage control of the grid-connected VSC is critical to obtain constant DC-bus voltage and maintains power balance in the DC microgrid.
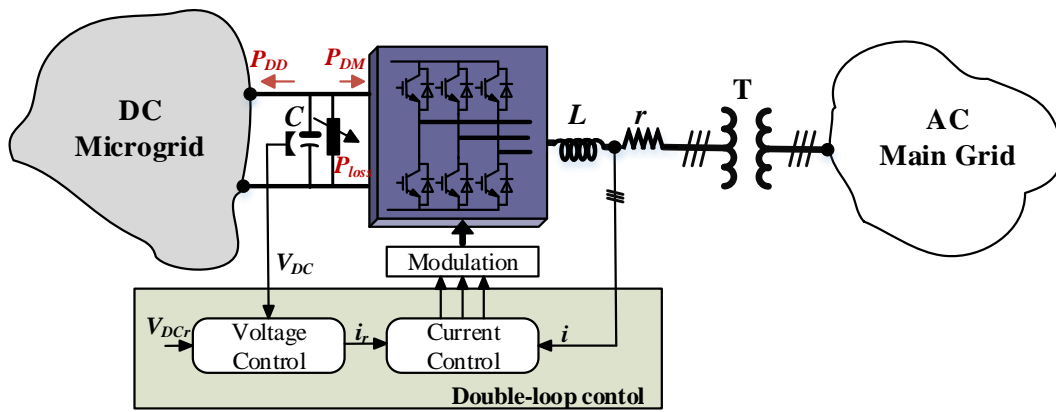

Fig. 1 Studied grid-connected VSC for DC microgrid system.

The DC-bus voltage control of a VSC has been studied in many researches. As shown in Fig. 1, a double-loop control structure is commonly used to control the VSC. The inner current control loop takes the responsibility for current tracking and the outer DC-bus voltage control loop for constant DC-bus voltage tracking. The conventional control strategy is using PI controller for both control loops [6-7]. To improve the DC-bus voltage dynamics behavior in the presence of external disturbances or system disturbances, a feedforward compensation is proposed to be added in the outer DC-bus voltage control loop [8-9]. Although, a real-time feedforward compensation can well offset the system disturbance effectively and consequently improve the disturbance rejection capability of the DC-bus voltage control, it needs additional senor that may increase the cost and complexity of the control system. Recently, sensor-less DC-bus voltage control strategies have been proposed by introducing a disturbance signal based on a disturbance observer [5], [10]. These nonlinear observer-based DC-bus voltage control methods obtain good dynamics and disturbance rejection capability while they need complex stability analysis. Some linear observer-based

DC-bus voltage control methods are proposed in [11-13]. Design of these linear observer-based methods are simpler. However, a trade-off between the disturbance rejection and noise suppression performance exists. In this paper, the ADRC-based DC-bus voltage control is proposed for the grid-connected VSC in DC microgrid. The effect of the bandwidth of conventional ESO (CESO) is investigated. Besides, the convention ESO is improved with adaptive observer gains to ensure better noise suppression performance when both CESO and AGESO are in the same level of disturbance rejection capability.

2. Control Strategy of Grid-connected VSC

The DC-bus power port modeling and double-loop control structure are discussed in this section.

A. Equations in DC-Bus Power Port

The DC-link power port is an important part to keep power balance and hence voltage stability for the DC microgrid to perform power exchange with the AC main grid. The AC main grid will servers as a DC source to compensate power imbalance in the DC microgrid. A large DC-bus capacitor is needed to avoid steep variation of the DC voltage and maintain the power quality in the AC side. Properly controlled DC-bus voltage requires power balance between the two side of the DC-bus capacitor, which can be described as follow:

$$P_{DD} + P_{loss} + \frac{C}{2}\frac{dV_{DC}^2}{dt} = P_{DM} \tag{1}$$

where P_{DD} is the power flowing into the DC microgrid, P_{loss} is the lumped power loss in the DC-bus power port, C is the DC-bus capacitor, V_{DC} is the DC-bus voltage and P_{DM} is the power from the AC main grid. Normally, P_{DD} is determined by the power demands from the DC microgrid and generally can be considered as a time-varying and exogenous disturbance for the grid-connected VSC system. P_{loss} is considered as the inner disturbance. V_{DC}^2 is the state variable and P_{DD} is the control input.

B. Inner Current Control Loop in d-q Reference Frame.

The power control loop is to deliver the given amount of real power to the main grid. The given real power reference P_{DMr} is outputted from the DC-bus voltage control. According to the real power reference, the *d*-axis current reference is computed (here the VSC is set in unit-power-factor operation) and hence the real power tracking problem is equivalent to current tracking problem in the *d-q* reference frame. The schematic diagram of the power control loop is shown in Fig. 2.

To simplify the design of the current controller, its order is expected to be reduced into a first-order system. Therefore, the parameters tuning law of the PI

controller is set to cancel the system pole by constructing a zero in the loop gain. Finally, the resultant power control loop can be expressed by the following transfer function as

$$G_C(s) = \frac{1}{\tau_i s + 1} \qquad (2)$$

where τ_i is the time constant which decides the bandwidth of the power control loop. τ_i is preferred to be small to achieve small phase lag whereas it has a minimum limitation because the bandwidth is limited by the switch frequency of power-electronic-based VSC. Based on τ_i, the PI controller's parameter can be selected as $k_{pi} = L/\tau_i$ and $k_{ii} = r/\tau_i$.
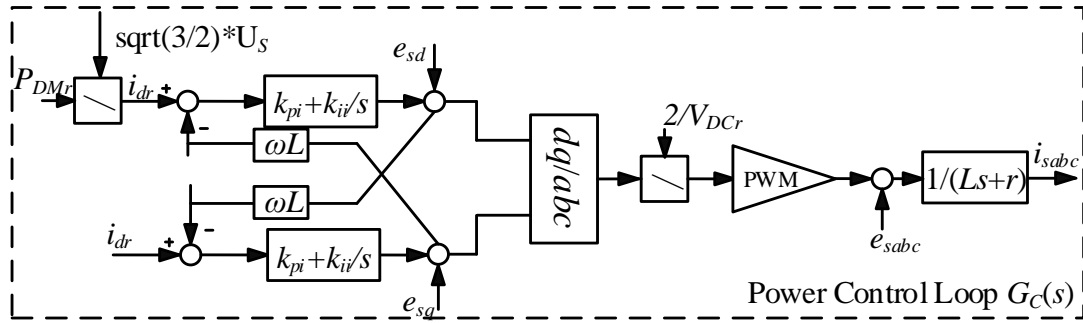

Fig. 2 Schematic diagram of the power control loop

C. PI-Based DC-Voltage Control Loop

Controlling V_{DC} can be achieved by controlling V_{DC}^2. The commonly used PI-based controller is an effective approach to regulate V_{DC}^2 as shown in Fig. 3. The DC-bus voltage control loop compares V_{DC}^2 with the reference signal V_{DCr}^2 and then process the error signal by a voltage compensator $K_{VC}(s)$ and a limiter and finally outputs the power reference signal P_{DMr} for the nested power control loop. Design of the voltage compensator is based on the knowledge of the closed-loop transfer function of the system to ensure enough phase margin. In general, the bandwidth of the outer DC-bus voltage controller is designed much lower than the real power controller in order to make the phase delay from $G_C(s)$ negligible. Based on this fact, it is considered that the assumption $G_C(s)=1+j0$ is reasonable in the design procedure of the DC-bus voltage control loop.
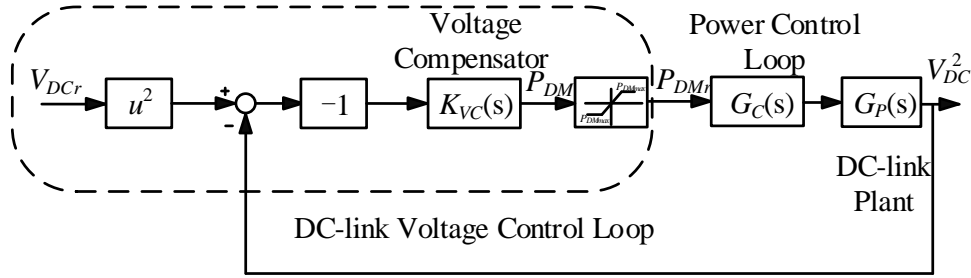
Fig. 3 Schematic diagram of the PI-based DC-voltage control.

As indicated at (1), P_{DD} and P_{loss} can affect V_{DC} in both transient and steady state. This negative impact can be removed in the steady state by including an integral term in the $K_{VC}(s)$. Since P_{DD} may be a time-varying variable due to continuous load variation, the mitigation of the negative impact in the transient state can only be achieved in a limited extent. To further mitigate the negative impact from exogenous disturbance P_{DD}, the feedforward compensation-based disturbance rejection control is added by measuring the exogenous disturbance P_{DD} as shown in Fig. 4. However, the feedforward compensation method requires costly sensor, which should be paid more attention to when the power level goes higher. Besides, internal disturbance P_{loss} is usually not measurable and may fail to be compensated with feedforward compensation-based disturbance rejection control. Hence, the negative impact from P_{loss} may still exist though it is very small.
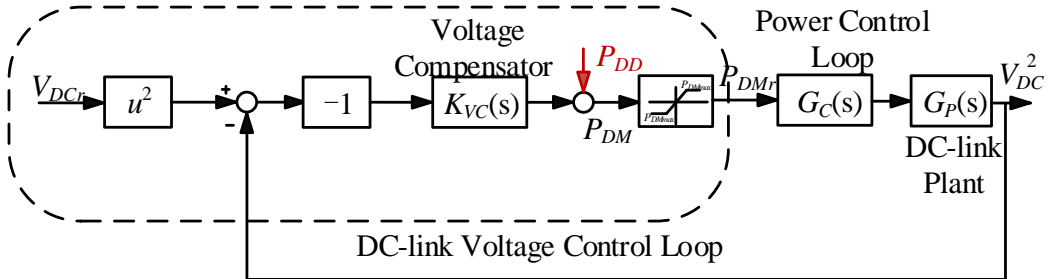

Fig. 4 Schematic diagram of the PI-based DC-voltage control with power-feedforward compensation.

D. ADRC-Based DC-Bus Voltage Control Loop with a CESO

It is known that the PI-based DC-voltage control approach needs detailed information of the model. Besides the feedforward compensation-based rejection control needs additional sensor and the inner disturbance P_{loss} may also be unavailable for feedforward compensation. To deal with these limitations, an extended observer is proposed to estimate the exogenous and inner disturbances in (1) instead of directly measuring them.

To introduce the extended state observer, an augmented state space formulation is derived based on (1) as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}}_{A} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \underbrace{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}}_{B} u + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{E} h \tag{3}$$

where x_1 equals to V_{DC}^2, x_2 equals to the sum of P_{DD} and P_{loss}, i.e., the lumped disturbances and uncertainties, and is also considered as an augmented state. b_0 is the coefficient of the control input. h is the derivative signal of the augmented state x_2.

According to the augmented state space formulation in (3), the extended state observer is established as

$$\begin{bmatrix} \dot{\hat{x}}_1 \\ \dot{\hat{x}}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}}_{A_o} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} + \underbrace{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}}_{B_o} u + \underbrace{\begin{bmatrix} l_1 \\ l_2 \end{bmatrix}}_{L} \left(y - \hat{x}_1 \right) \tag{4}$$

$$y = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{C} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \delta(t) \tag{5}$$

where $\hat{x}_1$ is estimated state of x_1, $\hat{x}_2$ is the estimated state of x_2, y is the measured output signal which consists of true signal x_1 and noise signal $\delta(t)$, l_1 and l_2 are the observer gains.

The bandwidth tuning method is used to select proper observer gains l_1 and l_2 to ensure the stability of the extended state observer. By subtracting (4) from (3) and combining (5), the estimated error dynamic can be derived as follows.

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} -l_1 & 1 \\ -l_2 & 0 \end{bmatrix}}_{A_d} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} + \underbrace{\begin{bmatrix} -l_1 \\ -l_2 \end{bmatrix} \delta(t) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h}_{\text{disturbance term}} \tag{6}$$

The characteristic polynomial of the coefficient matrix Ad is given by

$$\lambda(s) = s^2 + l_1 s + l_2 \tag{7}$$

If roots of (7) are forced to be located at $\lambda_0 = -\omega_0$, i.e., the bandwidth of the extended state observer is ω_0, then the observer gains l_1 and l_2 can be chosen as follow:

$$\begin{cases} l_1 = 2\omega_0 \\ l_2 = \omega_0^2 \end{cases} \tag{8}$$

The bandwidth tuning method is an effective and simple way to select proper observer gains meanwhile guarantee the stability of the extended state observer.

It is known that the larger the bandwidth is, i.e., the larger the observer gains are, the better tracking performance the extended state observer will achieve. The negative impact of the disturbance term in (6), however, will amplify as l_1 and l_2 increase.
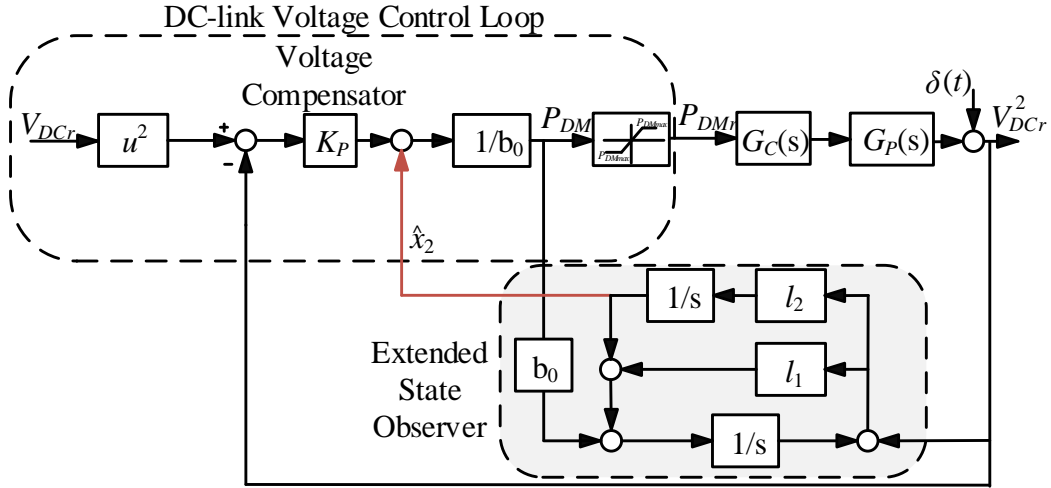

Fig. 5. Schematic diagram of the ADRC-based DC-voltage control with a conventional ESO

It is indicated in (6) that noise in the will not threat the convergency characteristic of the estimated error system though, it may impact the accuracy of the state variables' estimation Since the estimated state $\hat{x}_2$ is coupled into the control input which is the key process of the ADRC, the negative impact from the noise reflected on the output V_{DC}^2 will also aggravate.

E. ADRC-Based DC-Bus Voltage Control with an AGESO

To solve the trade-off between disturbance rejection and noise suppression, an adaptive gain is proposed based on the Kalman filter algorithm for the CESO. As the Kalman filter algorithm is generally implemented in digitally, the discrete form of the extended state observer is given by

$$\begin{bmatrix} \dot{\hat{x}}_1(k+1) \\ \dot{\hat{x}}_2(k+1) \end{bmatrix} = A_K \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} + B_K u + L_K \left[y(k) - \hat{x}_1(k) \right] \tag{9}$$

Where A_K, B_K, L_K is the discrete form of A, B, L.

Hence the discrete-time AGESO is given as follows.*Measurement update:*

$$\begin{cases} L_K(k) = P^-(k)C^T \left[C_d P^-(k)C^T + R \right] \\ \hat{x}(k) = \hat{x}^-(k) + L_K(k)\left[x_1(k) - \hat{x}_1(k) \right] \\ \quad P(k) = P^-(k) - L_K(k)CP^-(k) \end{cases} \tag{10}$$

Time update

$$\begin{cases} P^-(k+1) = A_K P(k)A^T + Q(k) \\ \hat{x}^-(k+1) = A\hat{x}(k) + B_K u(k) \end{cases} \tag{11}$$

Where $P^-(k)$, $L^-_K(k)$, $\hat{x}^-(k)$ denote the expected values computed by values on $(k-1)T$. $P(k)$, $L_K(k)$, $\hat{x}(k)$ denote the estimated value computed by the current expected valued. T is the sample period.

With $T \rightarrow 0$, the expression of the AGESO in continuous-time form can also be derived

The differential Riccati equation to compute the estimation-error covariance is given by

$$\begin{aligned} P(t) &= \lim_{T \to 0} \frac{P^-(k+1) - P^-(k)}{T} \\ &= -P(t)C^T R_c^{-1}(t)CP(t) + AP(t) + P(t)A^T + Q_C(t) \end{aligned} \tag{12}$$

The observer gains are given by

$$\begin{aligned} L(t) &= \lim_{T \to 0} \frac{P^{-1}(k)C^T \left[C_d P^{-1}(k)C^T + R \right]}{T} \\ &= P(t)C^T R_C^{-1}(t) \end{aligned} \tag{13}$$

The equation of the AGESO is given by

$$\dot{\hat{x}}(t) = A\hat{x}(t) + Bu(t) + L(t)\left[x_1(t) - \hat{x}_1(t) \right] \tag{14}$$

3.Simulation Verifications

To evaluate the performance of ADRC-based DC-bus voltage control strategy, a simulation is carried out in the MATLAB/Simulink environment according to Fig. 1. As this paper is focused on the DC-bus voltage's robustness of the grid-connected VSC in the DC microgrid, the dynamic of the DC microgrid is simplified as a dynamic power load as shown in Fig. 6. The main simulation parameters are listed in Table I.
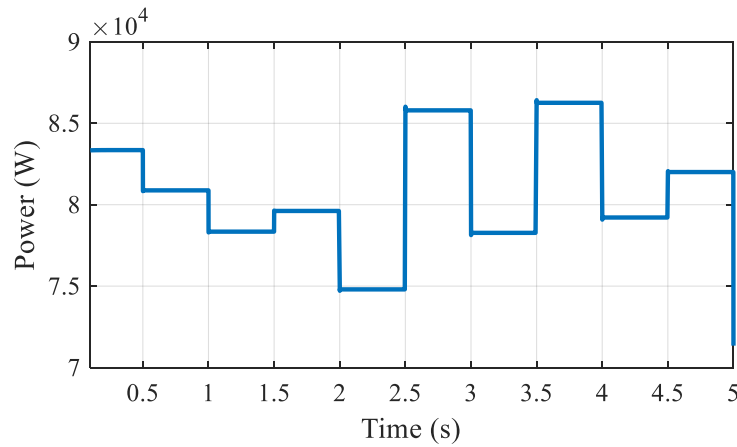
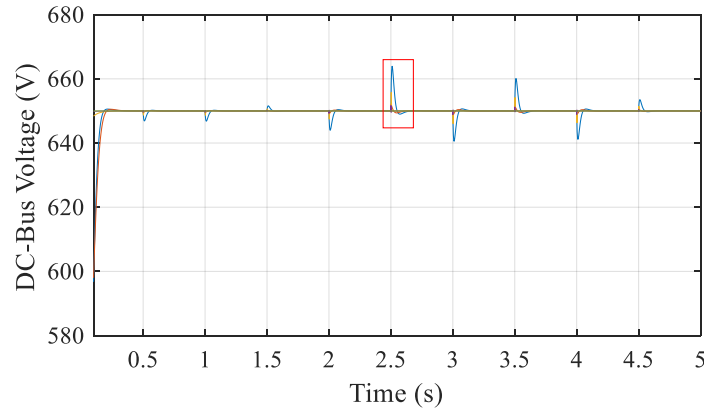Fig. 6 Simulated dynamic power demand of the DC microgrid.

Fig. 7 Responses of the DC-bus voltage under PI control, PI control with feedforward compensation and ADRC-based control with CESO.

The performance of the DC-link voltage control under the PI-based, the PI-based with feedforward compensation and ADRC-based DC-bus voltage control is compared. The bandwidth of the above DC-bus voltage controllers are set 700 rad/s for fair comparison. Under the dynamic power disturbance, different DC-bus voltage responses arise as shown in Fig. 7. To present a clear comparison among different control methods, the detail of the highlighted part in Fig. 7 is shown in Fig. 8 As seen, a decrease in power demand from the DC microgrid will introduce a DC-bus voltage rise for the grid-connected VSC at t=2.5s. The largest DC-bus voltage rise can be seen when it is controlled by the conventional PI control method. The feedforward compensation added for the PI controller can improve disturbance rejection capability because the magnitude of DC-bus voltage rise is decreased from 14V to 3V. It can also be seen that the ADRC-based control method can achieve satisfactory DC-bus voltage tracking

performance and disturbance rejection performance with CESO. It is also indicated that a bigger bandwidth will result in a better disturbance rejection capability.

Table I

SIMULATED SYSTEM PARAMETERS

System parameters	Values
U_S	380V
V_{DCr}	650V
C	4200μF
L	0.1mH
r	2e-3Ω
k_{pi}	0.5
k_{ii}	10

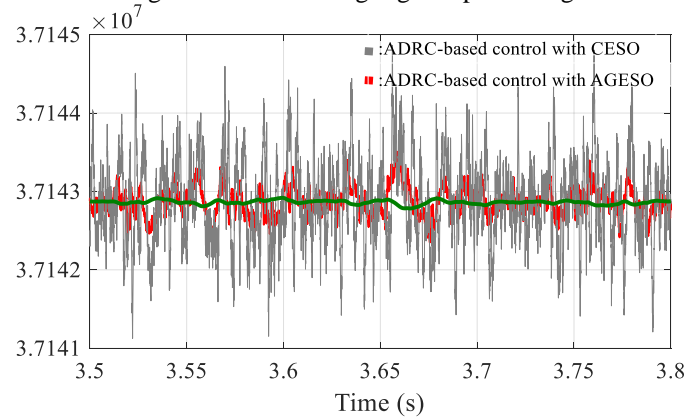Fig. 8 Detail of the highlighted part in Fig. 7.

Fig. 9 Estimated disturbances under ADRC-based control with CESO and AGESO in noisy environment.

As discussed in Section II-D, there is a trade-off between the disturbance rejection capability and noise immunity in the bandwidth-tuning-based CESO. To verify the effectiveness of the proposed AGESO which can automatically obtain the observer gains according to the Kalman filter-based algorithm, a series of comparative simulation experiments are carried out. To simulate the noise pollution in the output measurement, $\delta(t)$ is considered as the white random signal, the variance of which is set as 100. The bandwidth of the outer DC-bus voltage control loop is decreased to 20 rad/s to ensure a complete decoupling performance between the outer DC-bus voltage control loop and the extended state observer. Fig. 9 shows the estimated disturbance under the ADRC-based DC-bus voltage control with CESO and AGESO. It can be seen that estimated disturbance with CESO presents higher vibration than that with AGESO while both the approaches present almost the same level of disturbance rejection capability against the dynamic power disturbance as shown in Fig. 12. Fig. 13 shows that the estimated disturbances with CESO and AGESO are almost the same. Therefore, it is verified that the proposed AGESO can automatically find the better observer gains to improve the noise suppression performance and hence contribute to a better system performance when the noise signal exists in the output.
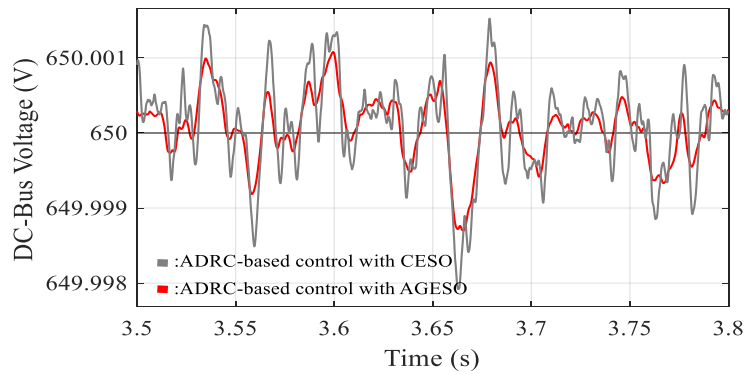

Fig. 10 Responses of the DC-bus voltage under ADRC-based control with CESO and AGESO in noisy environment.
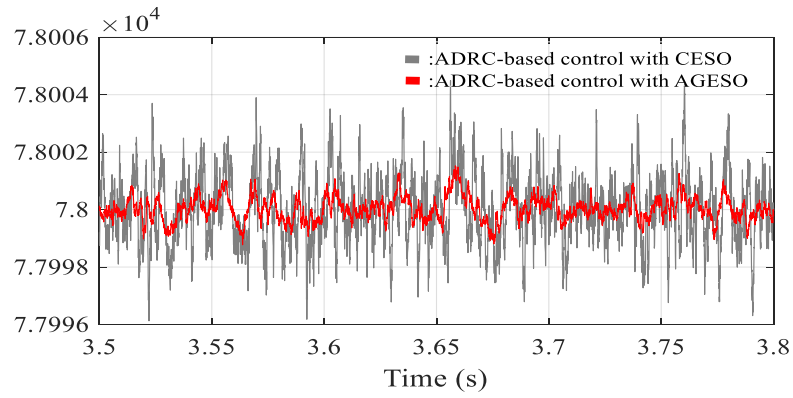
Fig. 11 Control inputs under ADRC-based control with CESO and AGESO in a noisy environment.
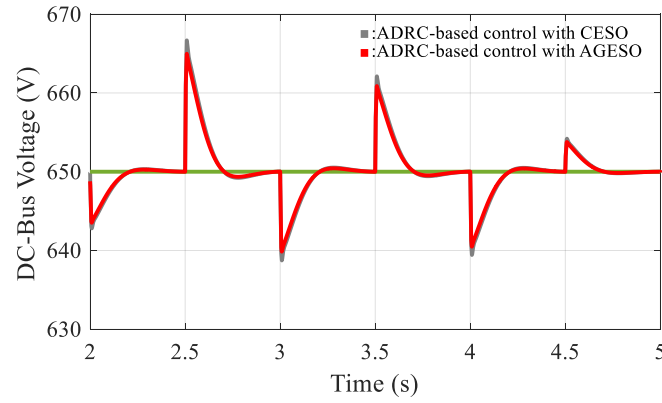

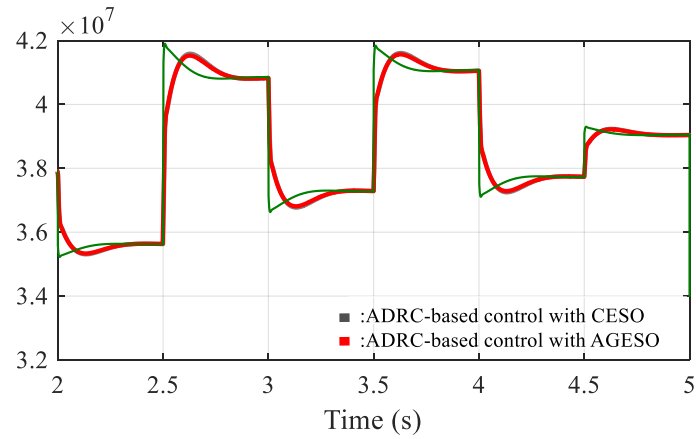Fig. 12 Responses of the DC-bus voltage under ADRC-based control with CESO and AGESO.

Fig. 13 Disturbance estimations under ADRC-based control with CESO and AGESO.

4. Conclusion

In this paper, the DC-side voltage robust control for hybrid AC/DC microgrid is researched and an ADRC-based DC-bus voltage control method is proposed for the grid-connected VSC in DC microgrid. Compared with the traditional power feedforward suppression method, this method can not only obviate the need of the additional sensor which is necessary for conventional PI-based control with feedforward compensation, but also be more independent from the model information. In addition, the ADRC is improved using an adaptive gain based ESO, which achieves better trade-off between disturbance rejection capability and measurement noise attenuation. Simulation results verify that :1) the proposed method features a higher level of disturbance rejection capability compared to traditional PI-based method with feedforward compensation; 2) the proposed method highlighted by AGESO shows better measurement noise attenuation ability compared to conventional method with CESO.

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