A NOVEL NEUTRAL POINT BALANCE STRATEGY FOR NPC INVERTER BASED ON SPWM

Bo GONG[1], Shanmei CHENG[2], Yi QIN[3]

In this paper, the neutral point voltage variation is analyzed based on neutral point current, and the relationship among neutral point voltage variation, voltage offset, the power factor, and the regulation angle is investigated in detail. A novel neutral point balance strategy for NPC inverter based on sinusoidal pulse width modulation (SPWM) is proposed. A voltage offset is added to the modulation waves to maintain the neutral point voltage balance. The neutral point voltage can be balanced by adjusting the voltage offset and regulation angle, which is easy to implement. Simulation results verify the effectiveness of the proposed strategy.

Keywords: three-level inverter, neutral point voltage, voltage offset, SPWM

1. Introduction

Recently, the neutral point clamped three-level inverter has found widely implemented in medium-voltage high-power applications, such as industrial drive, traction and power system, since it has the following advantages: lower voltage stress on switching devices, improved output waveforms, better electromagnetic compatibility [1-4]. Fig. 1 shows the NPC three-level inverter topology.

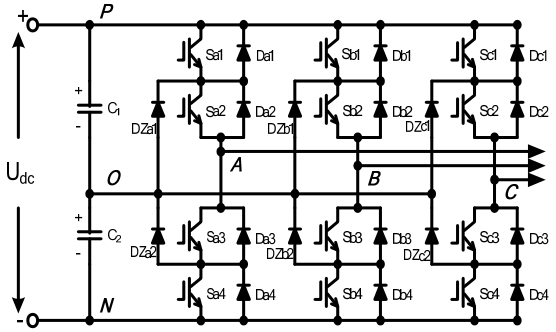


Fig. 1. Three-level NPC inverter structure diagram

[1] PhD student, Dept. of Control Science and Engineering, Huazhong University of Science and Technology, China, e-mail: oxinyi@gmail.com

[2] Prof., Dept. of Control Science and Engineering, Huazhong University of Science and Technology, China

[3] Prof., Dept. of Control Science and Engineering, Huazhong University of Science and Technology, China

However, the NPC three-level inverter has an inherent problem of the neutral point voltage balance. Under normal operation, the neutral point voltage is half of the DC voltage, the voltage reference point is the negative terminal of the DC-link in the system. The neutral point voltage unbalance involves nonuniform dc-link capacitors, operating conditions and load types. The unbalance of the neutral point voltage will increase the output voltage harmonics, damage the switching devices and dc-link capacitors. Therefore, the neutral point voltage balance has been extensively investigated and several control techniques have been developed [5-9]. Most of the control techniques are based on space vector pulse width modulation (SVPWM) method, and SPWM method. For SVPWM scheme, redundant states of the small vectors are employed to maintain the neutral point voltage balance [10-13], but the calculation of the dwell time and the vector switching sequence selection are really burdensome because of the large number of the switching states, and the relationship between neutral point voltage and various switching states is very complicated. For SPWM scheme, a zero sequence signal is added to the modulation waves to balance the neutral point voltage [14-18]. In [14], a real-time neutral point voltage control scheme based on zero sequence voltage injection without measuring the power factor angle was proposed. The neutral point voltage can be controlled precisely. However, the mentioned method requires much information of system parameters, such as the three phase reference voltages, output currents, capacitor voltages, and values of the dc-link capacitors. Therefore, it is not conducive to real-time implementation because of its complexity.

This paper presents a comprehensive analysis of the neutral point voltage variation based on neutral point current, a neutral point voltage balance control strategy based on SPWM is proposed, it only requires detecting the capacitor voltages, so it is simple and easy to realize. For the new strategy, a voltage offset is added to modulation wave, the neutral point voltage variation is correlative with the voltage offset, regulation angle, power factor angle, and load current value, and the neutral point voltage can be balanced by adjusting the voltage offset and regulation angle with different power factors. Simulation results show that the strategies have good capability for neutral point voltage balance.

2. Neutral point balancing analysis of SPWM scheme

There are many modulation schemes to generate PWM signals. The SPWM modulation scheme is the most widely used method, because it can be easily implemented with digital techniques and extended to use in higher level converter topologies. The multilevel SPWM modulation scheme is based on a comparison of a sinusoidal reference waveform with several vertically shifted carrier waveforms. The SPWM scheme for there-level inverter is shown in Fig. 2,

during a PWM period, if the modulation wave is greater than the upper carrier wave, switch Sa1 is on and Sa3 is off. In contrast, if the modulation wave is greater than the lower carrier wave, switch Sa2 is on and Sa4 is off. There are three output states of phase voltage. When Sa1 and Sa2 are on, Sa3 and Sa4 are off, the output state is "P", the phase voltage $U_{AO} = U_{dc}/2$. Output state "O" signifies that Sa2 and Sa3 are on, Sa1and Sa4 are off, $U_{AO} = 0$. When Sa3 and Sa4 are on, Sa1, Sa2 are off, the output state is "N" and $U_{AO} = -U_{dc}/2$.

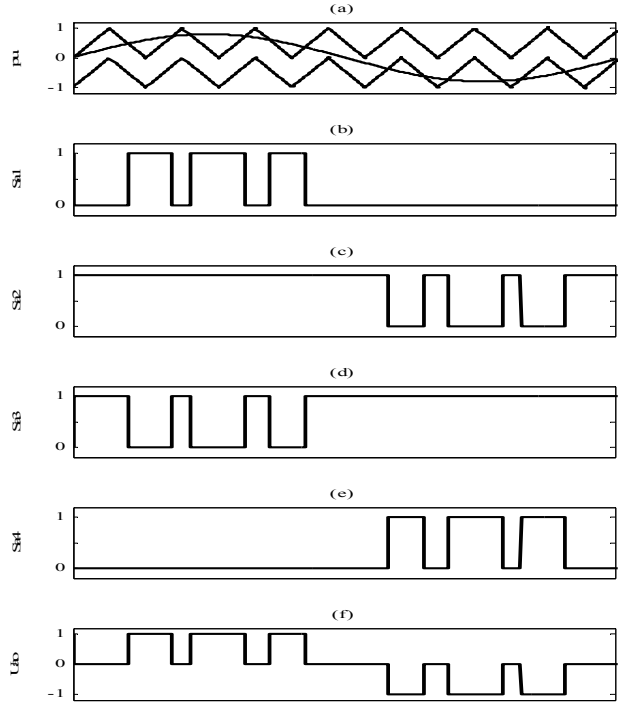


Fig. 2. (a) SPWM scheme for three-level NPC inverter, (b)-(e) the gate signals for switches Sa1, Sa2, Sa3, and Sa4, (f) output phase voltage

The three phase reference voltages are expressed by following expressions, where m is the modulation index, $0 \le m \le 1$.

$$\begin{cases} u_a = m\sin\omega t \\ u_b = m\sin(\omega t - \frac{2}{3}\pi) \\ u_c = m\sin(\omega t - \frac{4}{3}\pi) \end{cases} \tag{1}$$

The output currents are assumed as sinusoidal:

$$\begin{cases} i_a = I_m \sin(\omega t - \varphi) \\ i_b = I_m \sin(\omega t - \frac{2}{3}\pi - \varphi) \\ i_c = I_m \sin(\omega t - \frac{4}{3}\pi - \varphi) \end{cases} \tag{2}$$

where I_m is the current amplitude, φ is the power factor angle, and ω is the fundamental angular frequency.

The carrier frequency is assumed to be sufficiently high compared with the output frequency, whereas the reference voltages and phase currents are assumed constant in a PWM period.

The average neutral point current during a PWM period is

$$i_o = i_a d_{ao} + i_b d_{bo} + i_c d_{co} \tag{3}$$

where d_{jo} (j=a, b, c) is the time ratio of the "O" state in each PWM period. As shown in Fig. 3, when $u_j \geq 0$, if $u_{tri1} > u_j$, the output state is "O" and $t_{jo} = (1-u_j)\times T$. When $u_j < 0$, if $u_{tri2} < u_j$, the output state is "O" and $t_{jo} = (1+u_j)\times T$, where utri1 is the upper carrier; u_{tri2} is the lower carrier for three-level SPWM algorithm, t_{jo} is the dwelling time of the "O" state, and the PWM period is T, hence, the time ratio of the "O" state is shown by the following expression:

$$d_{jo} = \begin{cases} 1-u_j & (u_j \geq 0) \\ 1+u_j & (u_j < 0) \end{cases} \tag{4}$$

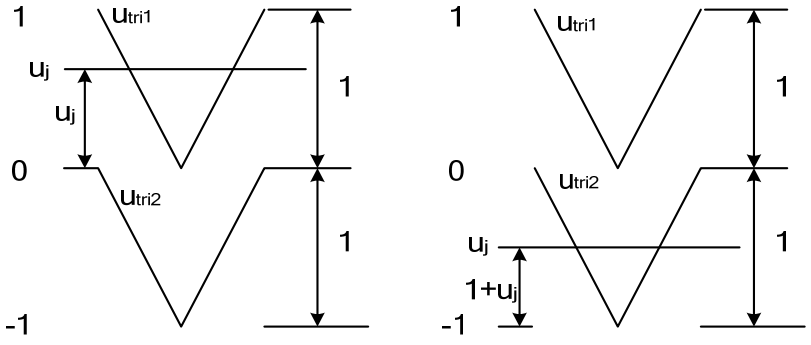


Fig. 3. The time ratio of the "O" state

The relationship between the neutral point current i_o and voltage unbalance dU_c is

$$dU_c = U_{c1} - U_{c2} = \frac{i_o}{C} = \frac{i_a d_{ao} + i_b d_{bo} + i_c d_{co}}{C} \tag{5}$$

When any phase is clamping to the neutral point, the current flows out or into the neutral point, which results in a rippling of the capacitor voltages and the neutral point unbalance.

3. Neutral point balance control based on SPWM

In this paper, a voltage offset is add to the adjusting phase u_k (k is a, b or c) to maintain the neutral point voltage balance. The adjusting phase u_k is the phase whose absolute value is the largest of three phases which is given by the following:

$$u_k = \begin{cases} \min\{u_j\} & \max\{u_j\} < abs(\min\{u_j\}) \\ \max\{u_j\} & \max\{u_j\} > abs(\min\{u_j\}) \end{cases} \quad j = a,b,c \tag{6}$$

where $\min\{\}$ is the function to get the minimum of the three phases, and $\max\{\}$ is the function to get the maximum of the three phases.

The adjusting phase is set to be:

$$u_k^{'} = u_k + \Delta u \tag{7}$$

where Δu is the voltage offset.

The modulation waveforms for neutral point voltage balance control strategy when $\Delta u>0$ are shown in Fig. 4. The modulation waveform of phase A can be expressed as:

$$u_a^{'} = \begin{cases} u_a & (-\pi/2+\Delta\theta) \le \omega t \le (\pi/2-\Delta\theta) \, or \, (\pi/2+\Delta\theta) \le \omega t \le (3\times\pi/2-\Delta\theta) \\ u_a+\Delta u & (\pi/2-\Delta\theta) < \omega t < (\pi/2+\Delta\theta) \, or \, (3\times\pi/2-\Delta\theta) < \omega t < (3\times\pi/2+\Delta\theta) \end{cases} \tag{8}$$

where $\Delta\theta$ is the regulation angle, $0 \le \Delta\theta \le \pi/2$.

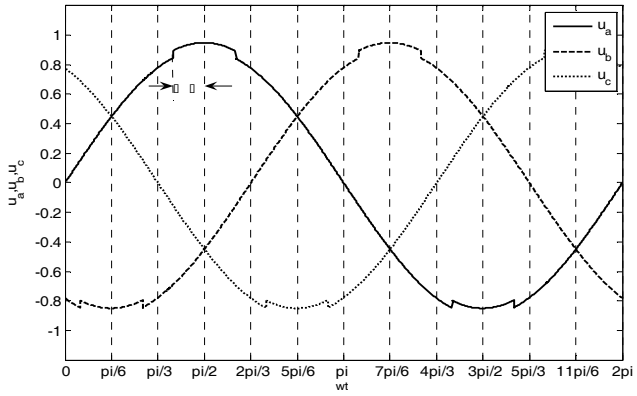


Fig. 4. Modulation waveforms for the proposed control strategy when $\Delta u>0$

For the proposed strategy, d_{jo} and dU_c can be expressed as:

$$d_{jo}^{'} = \begin{cases} 1-u_j^{'} & (u_j^{'} \ge 0) \\ 1+u_j^{'} & (u_j^{'} < 0) \end{cases} \tag{9}$$

$$dU_c = \int_0^{2\pi} \frac{i_a d'_{ao} + i_b d'_{bo} + i_c d'_{co}}{C} d(\omega t) \tag{10}$$

Let dU_{cj} (j=a, b, c) be the change in the neutral point voltage caused by each phase. The expression of dU_{ca} is

$$\begin{aligned} dU_{ca} = \int_0^{2\pi} \frac{i_a d'_{ao}}{C} d(\omega t) &= \int_0^{\pi} \frac{i_a \times (1-u_j)}{C} d(\omega t) - \int_{\frac{\pi}{2}-\Delta\theta}^{\frac{\pi}{2}+\Delta\theta} \frac{i_a \times \Delta u}{C} d(\omega t) \\ &+ \int_{\pi}^{2\pi} \frac{i_a \times (1+u_j)}{C} d(\omega t) + \int_{\frac{3\pi}{2}-\Delta\theta}^{\frac{3\pi}{2}+\Delta\theta} \frac{i_a \times \Delta u}{C} d(\omega t) \\ &= -\frac{4 \times I_m \times \Delta u \times \sin\Delta\theta \times \cos\varphi}{C} \end{aligned} \tag{11}$$

Proven by the same methods, dU_{cb} and dU_{cc} are shown by the following expression:

$$dU_{cb} = dU_{cc} = -\frac{4 \times I_m \times \Delta u \times \sin\Delta\theta \times \cos\varphi}{C} \tag{12}$$

The total change of the neutral point voltage is

$$dU_c = -\frac{12 \times I_m \times \Delta u \times \sin\Delta\theta \times \cos\varphi}{C} \tag{13}$$

The relationship among dU_c, Δu and φ is shown in Fig. 5, and the relationship among dU_c, Δu and $\Delta\theta$ is shown in Fig. 6. Obviously, $\sin\Delta\theta \geq 0$ when $0 \leq \Delta\theta \leq \pi/2$. The system is in motoring mode when φ is in $(-\pi/2, \pi/2)$, and system is in regenerative mode when φ is in $(\pi/2, 3\pi/2)$. Therefore, in motoring mode, when $\Delta u > 0$, $dU_c < 0$ and neutral point voltage will increase. In contrast, when $\Delta u < 0$, $dU_c > 0$ and neutral point voltage will decrease. In regenerative mode, when $\Delta u < 0$, $dU_c < 0$ and neutral point voltage will increase and when $\Delta u > 0$, $dU_c > 0$ neutral point voltage will decrease.

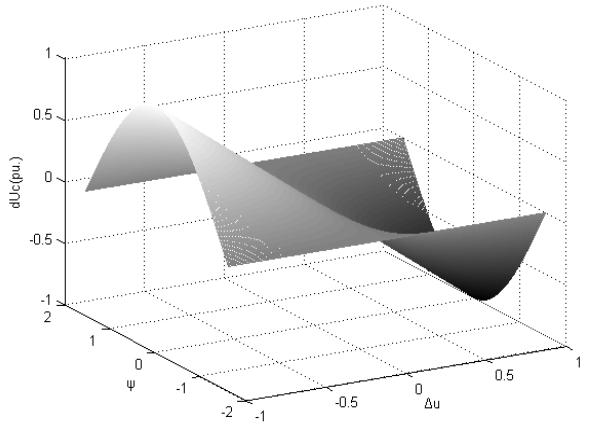


Fig. 5. Relationship among dU_c, Δu and φ

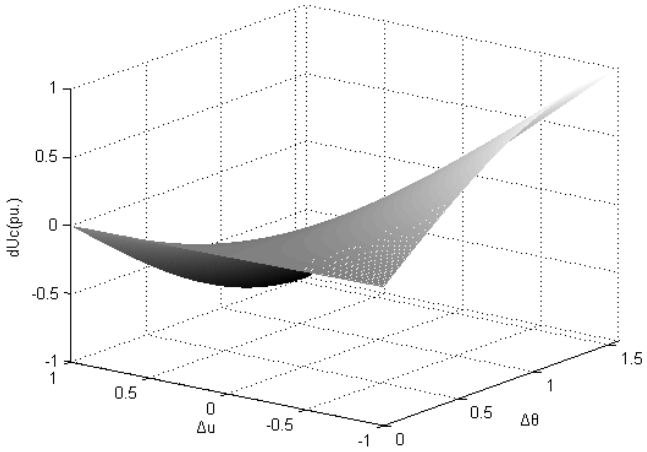


Fig. 6. Relationship among dU_c, Δu and Δθ

As shown in Fig. 7 and Fig. 8, the change of the neutral point voltage is proportional to the absolute value of Δu, when the power factor angle φ and $\Delta\theta$ keep invariant. And the change of the neutral point voltage is proportional to $\Delta\theta$, when the power factor angle φ and Δu keep invariant. Hence, maintaining the neutral point balance by adding the offset to modulation wave is available, and the adjusting strength can be controlled by Δu and $\Delta\theta$.

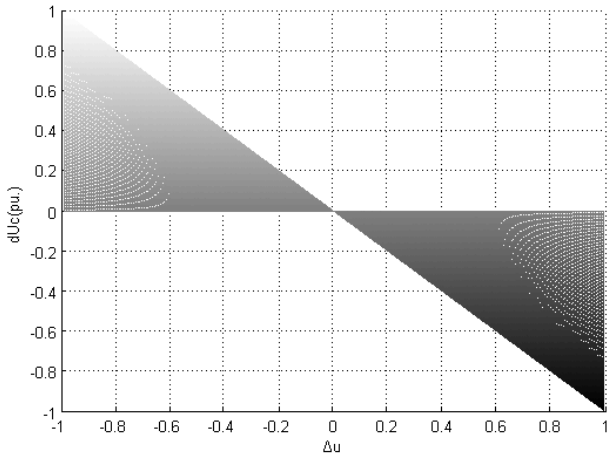


Fig. 7. Relationship between dU_c and Δu

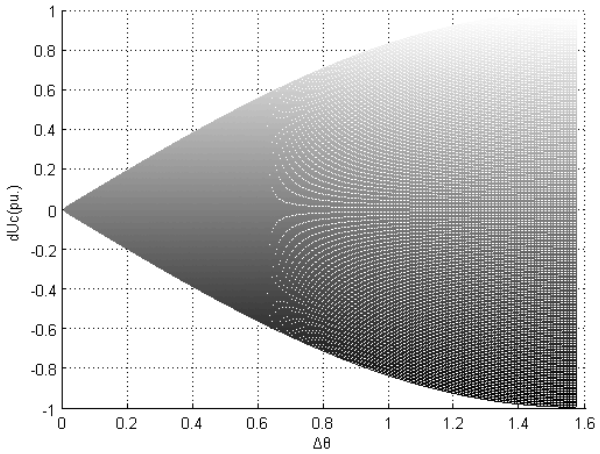


Fig. 8. Relationship between dU_c and $\Delta\theta$

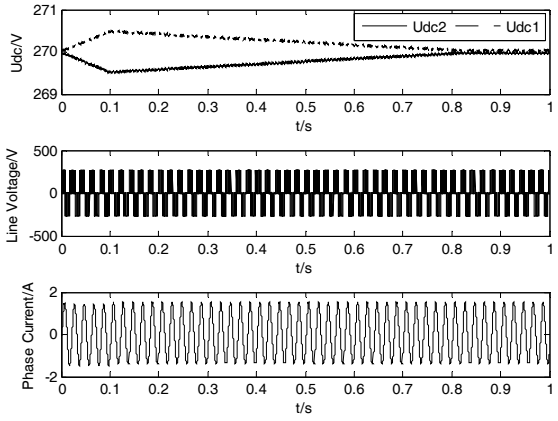
For high-voltage power conversion systems, the switching frequency is low, and the output currents contain high harmonic contents. The relationship between the total change of the neutral point voltage dU_c and harmonic components can be analyzed using the above method. It can be proved that when the even order harmonic is active, dU_c is zero, and dU_c is very small when the odd order harmonic is active. And the higher order harmonics can be filtered. Therefore, the output currents can be assumed as sinusoidal to analyze the change of the neutral point voltage.

4. Simulation results

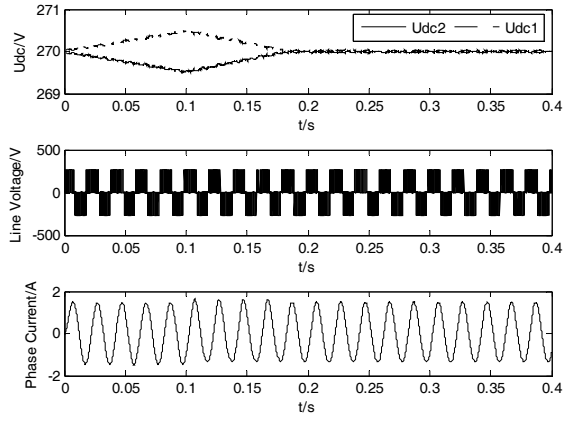
The validness of the control strategy is verified through simulations on the three-level NPC inverter using Matlab simulink package. In the closed-loop control, DC-link voltage is set to 540V, the initial voltage values of the two DC-link capacitors are 270V, and the switching frequency is 1 KHz. A resistor is placed parallel with C_2 to make the neutral point unbalance, R=2000Ω. The voltage values shift of the two DC-link capacitors occurs when the system is working, at t=0.1s the control of the neutral point voltage is applied.

The neutral point voltage control results, output line voltages and phase currents are shown in Fig. 9, and Fig. 10. Resistance-inductance load is used in the system, for Fig. 9, R=60Ω and L=33mH. The system is simulated with different modulation indices, voltage offsets, regulation angles, and power factors. Fig. 9 (a) ~ (d) show the control results when modulation index m is 0.4, and Fig. 9 (e) ~ (h) show the control results when modulation index m is 0.9. After employing the proposed neutral point voltage control strategy, the deviation of the two capacitor voltages is suppressed, neutral point voltage is quickly controlled to

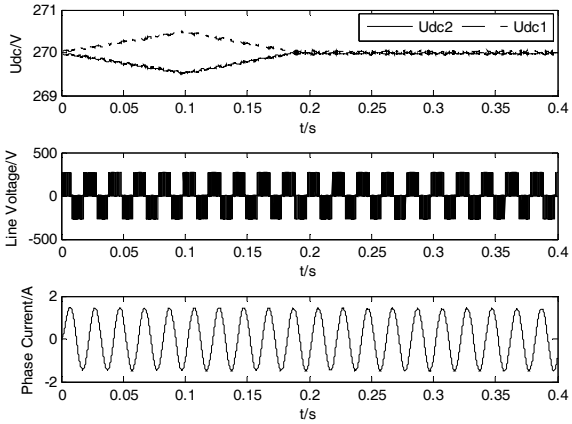
balance with excellent control precision, and the line voltages and phase currents change little. The results in Fig. 9 (a), (e) are obtained when the system is operated with $\Delta u=0.05$ and $\Delta\theta=\pi/3$, the results in Fig. 9 (b), (f) are obtained when the system is operated with $\Delta u=0.1$ and $\Delta\theta=\pi/3$, the results in Fig. 9 (c), (g) are obtained when the system is operated with $\Delta u=0.05$ and $\Delta\theta=\pi/2$, the results in Fig. 9 (d), (h) are obtained when the system is operated with $\Delta u=0.1$ and $\Delta\theta=\pi/2$. Fig. 9 (a) and (b) show the neutral point voltage balance control results, when the modulation indices, regulation angles and power factors are the same. It can be noticed that the larger the value of voltage offset is, the stronger the regulating capacity of the neutral point voltage is, as demonstrated by equation (13). Fig. 9 (a) and (c) demonstrate the neutral point voltage balance control results, when the modulation indices, voltage offset and power factors are the same. It can be observed that regulating capacity of the neutral point voltage is markedly strengthened with the increase of the regulation angle, which is in complete accordance with the theory. The same conclusions can also be drawn by comparing Fig. 9(e), Fig. 9(f), Fig. 9(g) and Fig. 9(h). In Fig. 9(a), the modulation index is 0.4, and in Fig. 9(e), the modulation index is 0.9. Therefore, the output phase current value is bigger with the same load. Obviously, the neutral point voltage adjusting is more quickly in Fig. 9(e), which is consistent with equation (13).



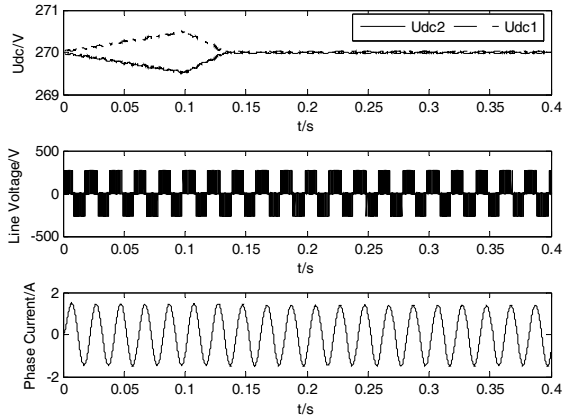
(a) m=0.4, $\Delta u=0.05$, $\Delta\theta=\pi/3$



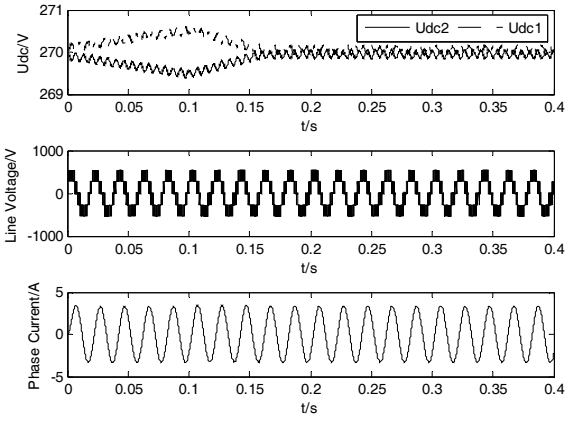
(b) m=0.4, Δu=0.1, Δθ=π/3



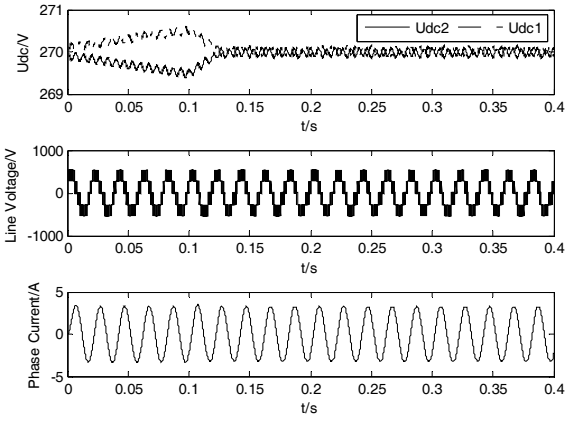
(c) m=0.4, Δu=0.05, Δθ=π/2



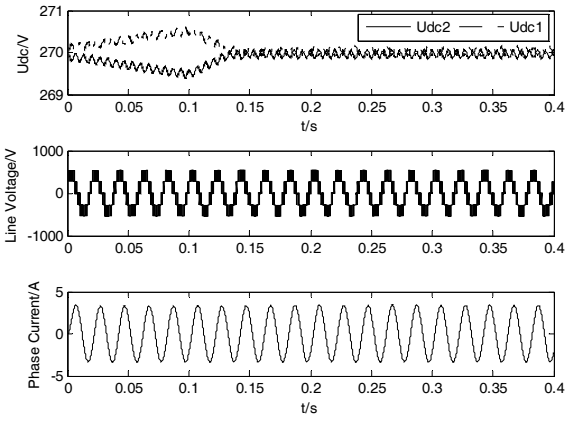
(d) m=0.4, Δu=0.1, Δθ=π/2



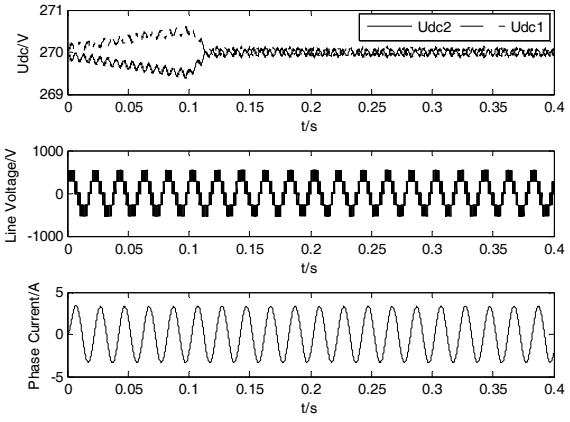
(e) m=0.9, Δu=0.05, Δθ=π/3



(f) m=0.9, Δu=0.1, Δθ=π/3

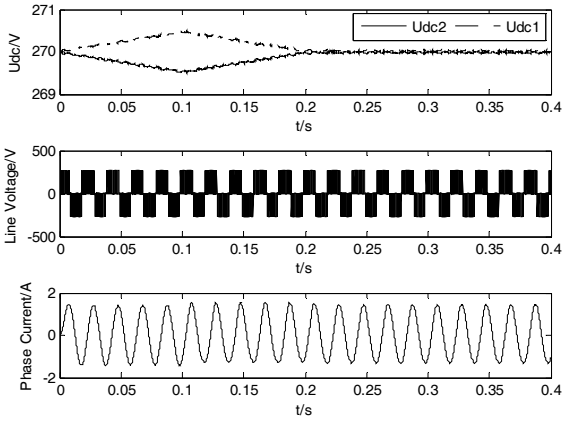


(g) m=0.9, Δu=0.05, Δθ=π/2

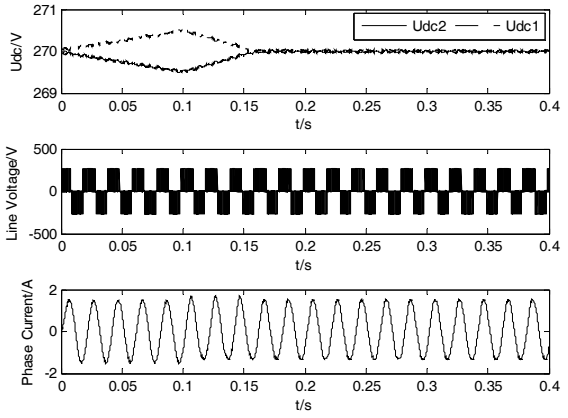


(h) m=0.9, Δu=0.1, Δθ=π/2

Fig. 9. Control results using neutral point control strategy



(a) m=0.4, Δu=0.1, Δθ=π/3 L=60mH



(b) m=0.4, Δu=0.1, Δθ=π/3 L=10mH

Fig. 10. Control results with different power factors

Fig. 10 shows the relationship between the neutral point voltage regulating capacity of the proposed scheme and power factor, when modulation index is 0.4, voltage offset is 0.1, and regulation angle is $\pi/3$. In Fig. 10 (a), the resistance is 60Ω, and inductance is 60mH of resistance-inductance load, the neutral point voltage regulation time is 0.12s. In Fig. 10 (a), the resistance is 60Ω, and inductance is 10mH of resistance-inductance load, the neutral point voltage regulation time is 0.06s. And as shown in Fig. 9 (b), the neutral point voltage regulation time is 0.08s, when the resistance is 60Ω, and inductance is 33mH of resistance-inductance load. The power factor will become higher when the inductance decreases, and the resistance keeps invariant. It can be seen that regulating capacity of the neutral point voltage is markedly strengthened by increasing the power factor with the other parameters consistent, which is consistent with the conclusions of the theoretical analysis. The proposed strategy can get rapid dynamic response and present good performance on neutral point voltage balance with different power factors.

5. Conclusions

In this paper, a neutral point voltage balance control strategy based on SPWM for three-level inverters is proposed, it requires few parameters of the system, so it is simple and easy to realize. This strategy maintains the neutral point voltage balance by adding a voltage offset to the modulation waves. The causes of the neutral point unbalance are studied in detail, and the neutral point voltage variation is correlative with the voltage offset, regulation angle, power factor angle, and load current value. The new simple and effective strategies for neutral point voltage control are verified through simulation. Simulation results show that the proposed strategy presents good performance in wide modulation range, and achieves good control effect on neutral point voltage balance with different power factors.

REFERENCES

[1]. *Z. G. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefanovic, J. M. Leuthen, and S. Gataric*, "Voltage Balancing Control of Diode-Clamped Multilevel Rectifier/Inverter Systems" , IEEE Transactions on Industry Applications, vol. 41, no. 6, November/December 2005, pp. 1698-1706.

[2]. *N. Celanovic, D. Boroyevich*, "A Comprehensive Study of Neutral-point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters" , IEEE Transactions on Power Electronics, vol. 15, no. 2, March 2000, pp. 242-249.

[3]. *I. Pereira, A. Martins*, "Neutral-Point Voltage Balancing in Three-Phase NPC Converters Using Multicarrier PWM Control" , Proceedings of International Conference on Power Engineering, Energy and Electrical Drives, 2009.

[4]. *B. P. McGrath, D. G. Holmes*, "Multicarrier PWM Strategies for Multilevel Inverters" , IEEE Transactions on Industrial Electronics, vol. 49, no. 4, August, 2002, pp. 858-867.

[5]. *H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming*, "Medium-Voltage Multilevel Converters-State of the Art, Challenges, and Requirements in Industrial Applications," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, August, 2010, pp. 2581-2595.

[6]. *M. Marchesoni, P. Tenca*, "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages", IEEE Transactions on Industrial Electronics, vol. 49, no. 4, August, 2002, pp. 752-765.

[7]. *F. Z. Peng*, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", IEEE Transactions on Industry Applications, vol. 37, no. 2, March/April, 2001, pp. 611-618.

[8]. *D. H. Lee, S. R. Lee and F. C. Lee*, "An Analysis of Midpoint Balance for the Neutral-Point-Clamped Three-Level VSI", Proceedings of IEEE Power Electronics Specialists Conference, 1998.

[9]. *M. Chang-Su, K. Tae-Jin, K. Dae-Wook, and H. Dong-Seok*, "A Simple Control Strategy for Balancing the DC-link Voltage of Neutral-Point-Clamped Inverter at Low Modulation Index", Proceedings of IEEE 29th Annual Conference of Industrial Electronics Society, 2003.

[10]. *P. J. Patel, R. A. Patel, V. Patel, and P. N. Tekwani*, "Implementation of Self Balancing Space Vector Switching Modulator for Three-Level Inverter", Proceedings of 3rd International Conference on Industrial and Information Systems, 2008.

[11]. *K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume*, "A Novel Neutral Point Potential Stabilization Technique Using the Information of Output Current Polarities and Voltage Vector", IEEE Transactions on Industry Applications, vol.38, no.6, November/December 2002, pp. 1572-1580.

[12]. *L. M. Tolbert, T. G. Habetler,* "Novel Multilevel Inverter Carrier-Based PWM Method", IEEE Transactions on Industry Applications, vol.35, no.5, September /October 1999, pp. 1908-1107.

[13]. *S. Busquets-Monge, S. Alepuz, J. Rocabert and J. Bordonau*, "Pulse Width Modulations for the Comprehensive Capacitor Voltage Balance of N-Level Three-Leg Diode-Clamped Converters", IEEE Transactions on Power Electronics, vol. 24, no. 5, May 2009, pp. 1364-1375.

[14]. *S. Qiang, L. Wenhua, Y. Qingguang, and W. Zhonghong*, "A Neutral-Point Potential Balancing Algorithm for Three-Level NPC Inverters Using Analytically Injected Zero-Sequence Voltage", Proceedings of IEEE 8th Annual Conference on Applied Power Electronics, 2003.

[15]. *S. Ogasawara, H. Akagi,* "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters", IEEE Industry Applications Society Meeting, 1993.

[16]. *L. Yongdong, W. Chenchen*, "Analysis and Calculation of Zero-Sequence Voltage Considering Neutral-Point Potential Balancing in Three-Level NPC Converters", IEEE Transactions on Industrial Electronics, vol. 57, no. 7, July 2010, pp. 2262-2271.

[17]. *A. Bendre, G. Venkataramanan, D. Rosene and V. Srinivasan*, "Modeling and Design of A Neutral-Point Voltage Regulator for A Three-Level Diode-Clamped Inverter Using Multiple-carrier Modulation", IEEE Transactions on Industrial Electronics, vol.53, no.3, June 2006, pp. 718-726.

[18]. *R. M. Tallam, R. Naik, and T. A. Nondahl*, "A Carrier-Based PWM Scheme for Neutral-Point Voltage Balancing in Three-Level Inverters," IEEE Transactions on Industry Applications, vol.41, no.6, November/December 2005, pp. 1734-1743.