U.P.B. Sci. Bull., Series A, Vol. 68, No. 3, 2006

REDUCTION OF THE ACQUISITION TIME FOR CMOS TIME-RESOLVED PHOTON EMISSION BY OPTIMIZED IR DETECTION

R. ISPASOIU, T. CRAWFORD, B. JOHNSTON, C. SHAW, S. KASAPI, J. GOERTZ, O. RINAUDO, P. OUIMET*

Pe bza optimizarii detectorului fotodioda cu avalansa din sistemul EmiScope™ utilizat pentru rezolvarea temporala a fotonilor, am realizat reducerea cu un factor mai mare de 2.5 a timpului de achizitie a semnalului emis în infrarosu de un tranzisttor CMOS. Efectul nedorit al pulsuirlor de zgomot generate de fotodioda la durate aleatorii fata de semnalul detectat a fost redus prin utilizarea întârzierii controlate a ferestrei temporale de detectie.

We have achieved a greater than 2.5x improvement in the acquisition time figure of merit of an EmiScope™ Time Resolved photon Emission (TRE)-based probe system, by optimization of the detector dark-count rate, photon detection efficiency, and timing jitter. The effects of detector after-pulsing were reduced by use of an optimized hold-off time.

Introduction

Time-resolved emission (TRE) has become an industry-standard for non-invasive back-side probing of ICs for debug and advanced failure analysis [1,2]. The continuing shrinkage of CMOS transistor size and lowering V_{DD} pose an increasing challenge to TRE systems because of lowering photon emission rates from transistors [3]. In order to keep pace with the corresponding trend in reducing CMOS photon emission, continuous improvements in photon-detection performance are required. Here we report a 2.5x improvement in acquisition time by optimizing the tradeoffs among the factors affecting detector performance. We are demonstrating the detector performance improvement with data from two test devices: a Credence test chip with 180nm gate length and a recent generation Freescale Semiconductor test device with 65nm gate length.

One practical figure of merit for assessing the measurability of the CMOS photon emission is the acquisition time to achieve a desired signal-to-noise (SNR). In order to compare the relative improvement in the acquisition time we are using the time-to-detection (T_{det}) figure of merit [4] that is associated [1]with the

* Research Scientist, Ph.D, Research Scientist, Ph.D, Research Scientist, Ph.D, Credence Systems Corp. – DCG, 1299 Orleans Dr., Sunnyvale, CA 94089, USA , Research Scientist, Ph.D , Research

acquisition time. In conditions when the signal is noise limited, T_{det} can be expressed as:

$$T_{\det} = \sigma^2 T_{loop} \frac{DCR \cdot TJ}{(PDE)^2} \tag{1}$$

where s is the confidence level in detecting a signal photon out of the noise, T_{loop} is the trigger loop length, DCR is the detector dark count rate, TJ is the single-photon detection timing jitter, and PDE is the photon detection efficiency.

1. Experimental setup, results and discussion

For the purpose of illustrating the way how the TRE setup works, in Fig.1 we schematically represent the time pattern associated with the operation of the IR photon detector, which for our system is an avalanche photodiode (APD) run in Geiger mode [4]. In this mode, it can achieve PDE ≥ 50%, TJ ≈ 52ps, and DCR ≤ 25,000 counts/second (cps). The reduction of T_{det} by the compression of T_{loop} has a significant effect on acquisition time reduction and has been discussed elsewhere [5]. In this work we are reporting on the reduction of the acquisition time by a factor of 2.5 (see Fig.2) by the optimization of the detector operation – characterized by the parameters DCR, TJ and PDE.

The overall PDE of the EmiScope™ system depends on the optical throughput of photons from the device under test (DUT) to the detector. Previously, the optical path in this photon-counting system included an optical switch. The switch allowed the user to insert a light source into the optical path in order to precisely place the illumination spot on the DUT area targeted for photon collection. However, the switch introduced extra loss into the photon-collection path as well. Here we have achieved a boost of at least 30% in the optical throughput by employing the light emission properties of the detector photodiode. Any photodiode can operate as an LED under forward bias [6]. By exploiting this property we no longer require an external light source; since the forward biased APD itself illuminates the area from which photons will be collected, the optical switch is obviated.

Scientist, Ph.D, Research Scientist, Ph.D, Freescale Semiconductor, 6501 William Cannon Dr., Austin, TX 78735, USA

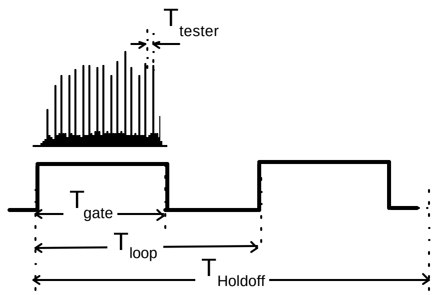

Fig. 1: The time pattern governing the operation of the IR photon detector. The detector is energized for a duration T_{gate} when it can sense the photons emitted by the CMOS transistor with a periodicity T_{tester}

In Fig.2 we show photon emission histograms recorded with different detector settings on a 180nm CMOS process device operating at a bias voltage of 1.0V (upper diagram) and compare it to the corresponding measured T_{det} values (lower diagram). The gray bars reflect the performance of a detector without the LED mode option, operating at the nominal specs of TJ ≈ 52ps and DCR ≤ 25.000 cps. The black and white bars represent the performance of the LED-mode detector in low DCR and low TJ (52ps) operation modes, respectively. Note that we achieve about 2.5x improvement in T_{det} in low-DCR mode, when the detector operates at DCR ≈ 15,000 cps, TJ ≈ 65 ps and PDE ≥ 45%; in the low-jitter mode the acquisition time is ~1.7x longer but the time resolution is optimized corresponding to TJ ≈ 52ps.

Other external factors can affect the DCR performance, stemming from the after-pulsing properties of the detector [7]. For example, when T_{loop} < 50µs and T_{gate} > 500ns, the DCR increases due to APD after-pulsing; the after-pulsing becomes more significant at smaller values of T_{loop}.

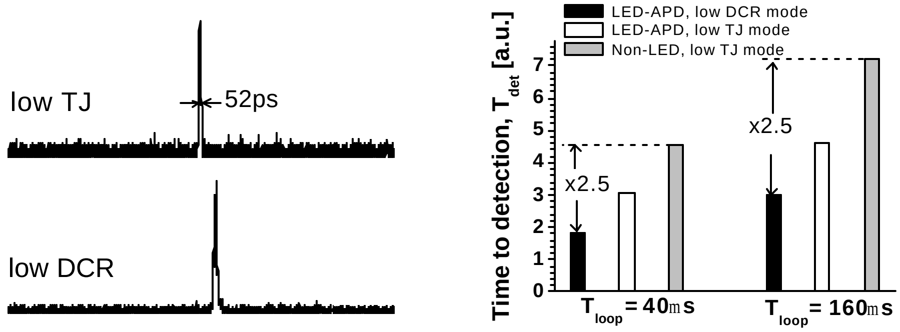

Fig. 2: Left: Comparison between emission histograms from a 180nm CMOS process, taken at low TJ and low DCR operation modes. Right: The summary of the corresponding improvement in the T_{det} figure of merit between low DCR and low TJ operation, at two T_{loop} settings for photon emission acquisition from a 180 nm CMOS.

The common work-around for this problem has been the use of a hold-off mode in which the detector is kept un-energized for a duration $T_{Holdoff}$ after each detection event [7]. $T_{Holdoff}$ is longer than the natural decay of the after-pulsing process (typically tens of microseconds at the APD operating temperature). As shown in Fig. 3.a), by using hold-off on the order of 100µs we recover the baseline DCR, essentially eliminating after-pulsing. It is worth noting that without hold-off, much of the benefit of loop compression as indicated by eqn.(1) would be lost due to the concomitant increase in DCR.

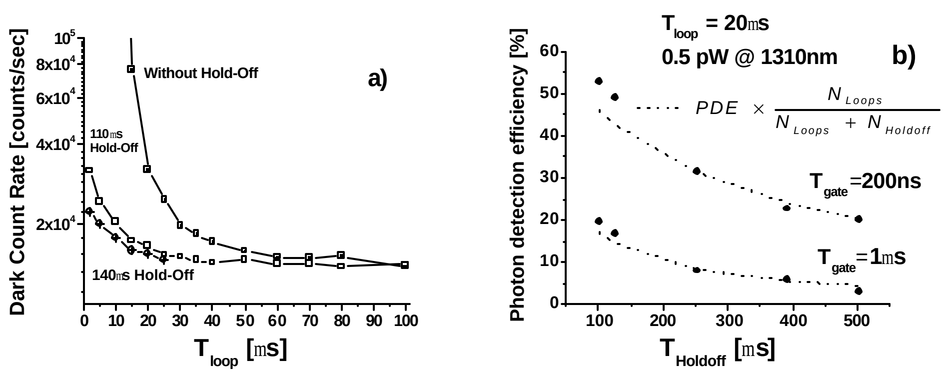

Fig. 3: a) The variation of the dark count rate with T_{loop} and the effect of hold-off in the reduction of DCR at short loops; b) The decrease of the effective detection efficiency with $T_{Holdoff}$ and T_{gate} when T_{Loop} is shorter than 50ms.

Another trade-off to using hold-off is that in cases when the CMOS emission signal is very strong (resulting in a high probability of detection per gating period) there is a significant probability that a photon will arrive during holdoff, leading to a reduction in the effective PDE. This can be made intuitively clear by considering that the detector remains off for some of the loops when it would otherwise be energized.

This is illustrated in Fig.3.b) which shows the variation of PDE with $T_{Holdoff}$ for T_{gate} set at 200ns and 1μs when T_{loop} was set at 20μs. The data was taken with an input light signal of 0.5pW at 1310nm (i.e. ~$3.3x10^6$ photons per second) which is significantly stronger than the typical emission from a 90nm (or smaller) CMOS circuit. The above mentioned decrease of PDE with $T_{Holdoff}$ is fit by a phenomenological equation involving a free parameter - N_{Loops} – the number of loops of detector operation until a photon is detected, and $N_{Holdoff}$ – the number of loops within a given hold-off time.

The understanding of these results allows us to adjust $T_{Holdoff}$ to the optimum duration for the specific emission characteristics of any CMOS, in order to ultimately minimize T_{det}. Practically speaking, the effect of holdoff on PDE is minimal because photon emission from CMOS ICs is very weak.

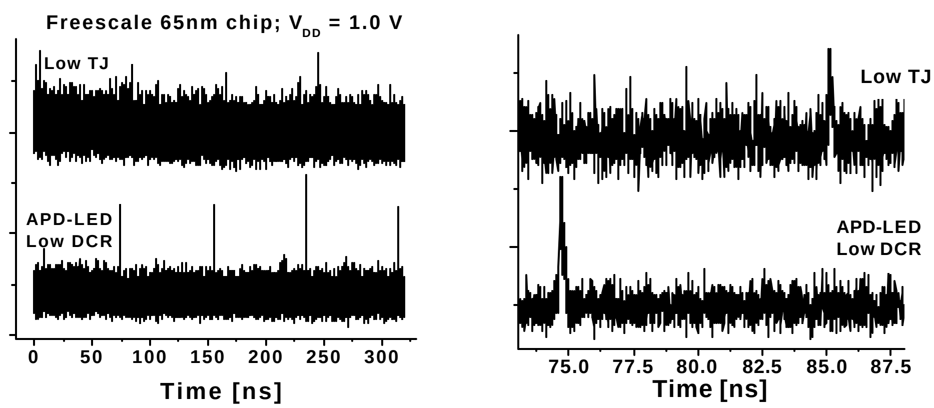

Fig. 4. TRE histograms from a Freescale 65nm CMOS biased at 1.0V. The detector operation conditions are indicated. The data acquisition time was 10min in both cases. Left: general view of the histograms; Right: zoom in on the emission peaks.

In Fig.4 we illustrate the detection time improvement with data from a current EmiScope™ field application. The DUT was a 65nm CMOS, from Freescale Semiconductor, biased at 1.0V and operating at a loop length of 42.25μs. In each diagram, two time-domain histograms are shown. The top histogram was taken in the low TJ mode while the lower histogram was taken in the reduced DCR setting for the system configuration allowing APD operation in

LED mode for DUT illumination. Due to these settings the lower trace unambiguously exhibits a reduced background noise as well as a stronger signal strength. The improvement in T_{det} was by more than a factor of 2.5.

From an EmiScope^{TM} user's point of view, it is worth emphasizing that we were able to acquire a well defined photon emission histogram, without the need of data averaging, from a 65nm CMOS in only 10 minutes. Work is under way to optimize the detector performance at lower temperatures, with a proven reduction of DCR to 8,000 cps corresponding to a PDE of more than 60%. This will allow an even more dramatic reduction of the data acquisition time in time-resolved photon emission for CMOS activity debug.

Conclusions

In conclusion, we have demonstrated an improvement in the acquisition time figure of merit, T_{det}, by a factor of greater than 2.5, by optimization of detector dark-count rate, photon detection efficiency, and timing jitter. Improvements to PDE were achieved by increasing the optical throughput of the system; TJ and DCR were optimized by bias conditions; the effects of after-pulsing were reduced by use of an optimized hold-off time. This reduction in acquisition time enables successful TRE probing of integrated circuits at 65nm and below.

Acknowledgements

We are grateful to Jim Vickers for inventing the EmiScope^{TM} and for continued help in keeping its performance up to speed.

REFERENCES

1. *D. Bodoh et al.*, "Defect Localization Using Time-Resolved Photon Emission on SOI Devices that Fail Scan Tests", Proc. ISTFA 2002, p. 655.
2. *P. Ouimet et al.*, "Analysis of 0.13um CMOS Technology Using Time Resolved Light Emission" Proc. ISTFA 2004, p. 203.
3. *S. Polonsky*, "Time-resolved emission spectroscopy of silicon integrated circuits", American Physical Society News, October 2005; online: http://www.aps.org/apsnews/1005/100515.cfm.
4. *J.S. Vickers et al.,* "Time-resolved photon-counting system based on a Geiger-mode InGaAs/InP APD and a solid immersion lens", Proc. IEEE LEOS 2003, vol.2, p. 600.
5. *R. Wampler et al.*, "Dramatic Reduction in Optical Probing Time Via Compression of ATPG-Generated Test Loops", submitted to ITC 2006.
6. *S. M. Sze*, "Physics of semiconductor devices", Wiley, New York (1981).
7. *R. Ispasoiu et al.*, "Time-resolved photon counting with Geiger mode avalanche photodiodes for CMOS activity debug", Single-Photon Workshop-2005, Teddington, UK.